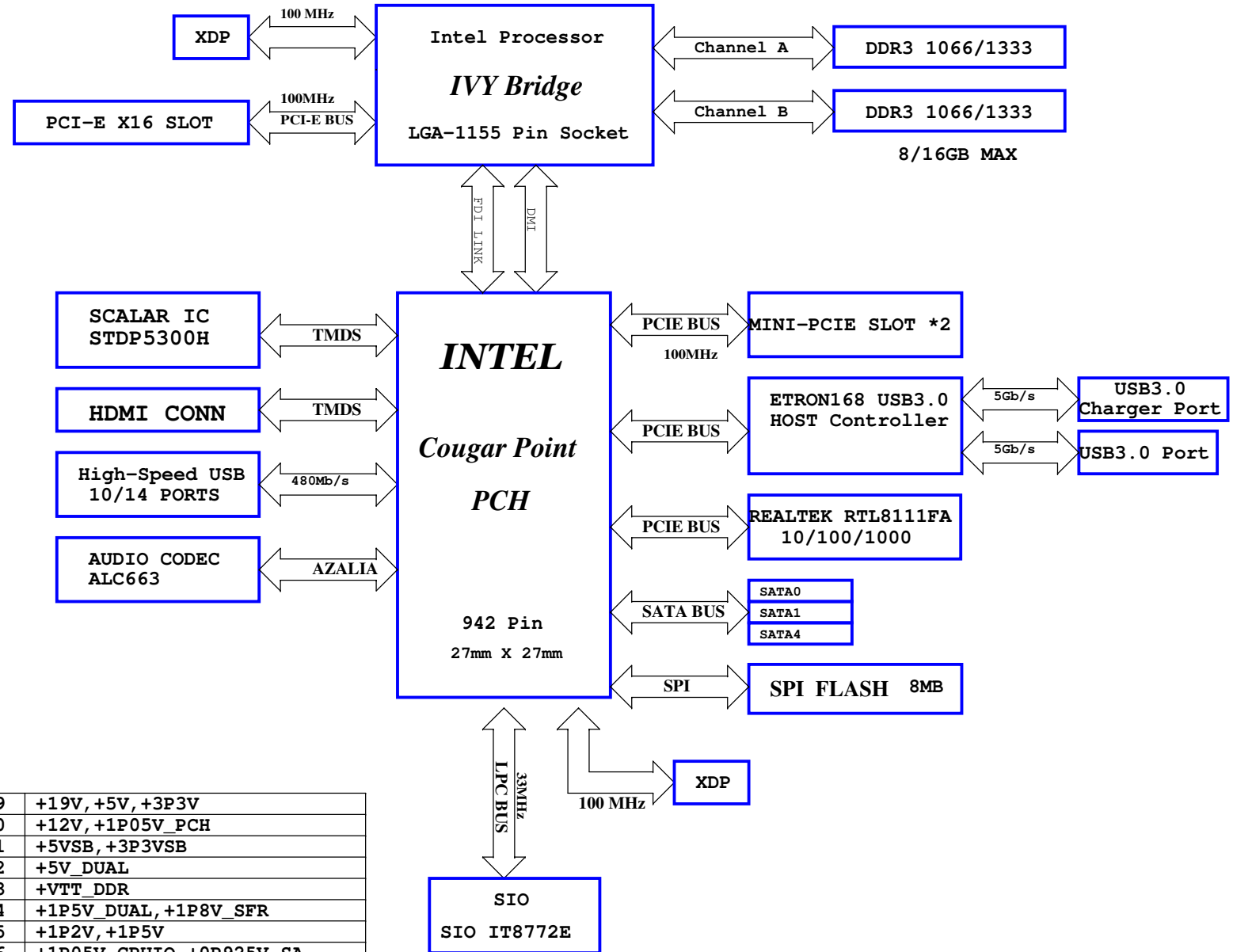


IPISB-AG

Revision: 1.06

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER SEQUENCE
03~08	INTEL CPU SOCKET1155(1~6)
09	PLTRST CPU#
10~11	DDR3 CHANNEL A&B
12	DDR3 TERMINATION A&B
13	TEMP SENSOR
14~22	INTEL PCH(1~9)
23	PCH_DPWROK & SLP_SUS
24	RSMRST# / PCIE_RST#
25	SM BUS & SPI ROM
26	PCI EXPRESS X16 SLOT
27	MINI-PCIE SLOT
28	MINI-PCIE SLOT
29	REALTEK RTL8111FA CONTROLLER
30	RJ45 CONNECTOR
31	REAR USB2.0 PORT
32	USB 3.0 CONTROLLER
33	USB POWER
34	SIDE USB3.0 PORT
35	SIDE USB2.0 PORT
36	USB PORT CONTROL
37	USB HEADER
38	USB Charger SLG55583
39	+5VA FOR CHARGE
40	REALTEK ALC663 CODEC
41	AUDIO AMP
42	AUDIO CONNECTOR
43	AUDIO SW
44	SUPER I/O IT8772E
45	FRONT PANEL CIRCUIT
46	FAN CIRCUIT
47	INTEGRATED VGA PORT
48	IR / SPKR
49	RTC/COMS/SCREW
50	DEBUG HEADER
51~52	SCALAR STDP5300H
53	I2S AUDIO DAC
54	LVDS CONNECTOR
55	DVI MUX
56	HDMI MUX
57	DVI CONNECTOR
58	HDMI-IN CONNECTOR
59	HDMI-OUT CONNECTOR
60	
61	SATA CONNECTOR
62	CARD READER RTS5209-GR
63	CARD READER CONNECTOR
64	+19V OCP - SYS_IN
65	VCORE CONTROLLER
66	VCORE DRIVER 1-2
67	VCORE DRIVER 2-2
68	AXG DRIVER

69	+19V,+5V,+3P3V
70	+12V,+1P05V_PCH
71	+5VSB,+3P3VSB
72	+5V_DUAL
73	+VTT_DDR
74	+1P5V_DUAL,+1P8V_SFR
75	+1P2V,+1P5V
76	+1P05V_CPUIO,+0P925V_SA
77	+1P05V_CPUIO CAP
78	DISCHARGE
79	CURRENT SENSE
80	CPU XDP DEBUG CONNECTOR
81	PCH XDP DEBUG CONNECTOR
82	EMI CAP



PEGATRON DT-MB RESTRICTED SECRET

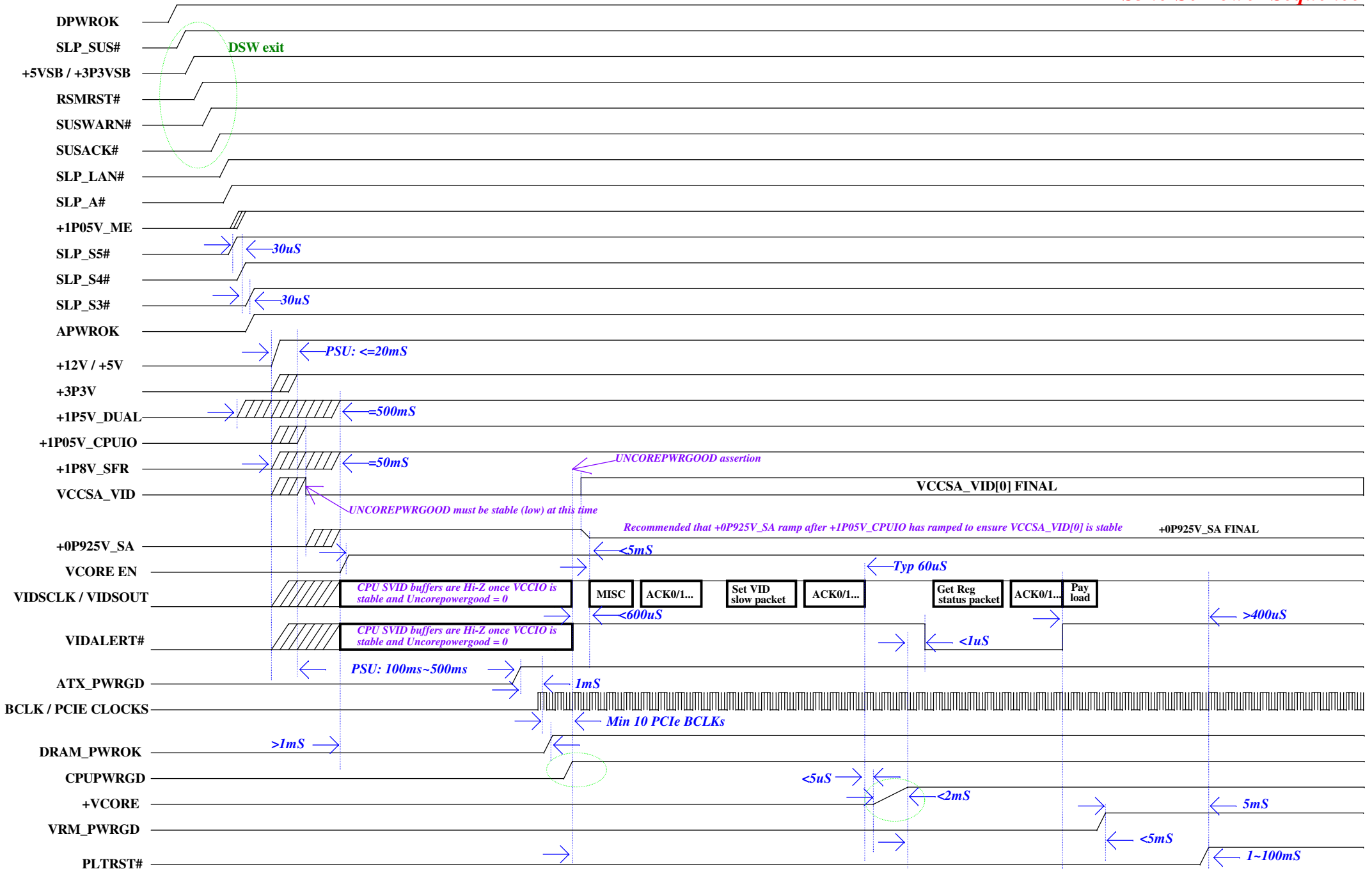
PEGATRON Title : **BLOCK DIAGRAM**

Pegatron Corp. Engineer: **ShunJing_Yang**

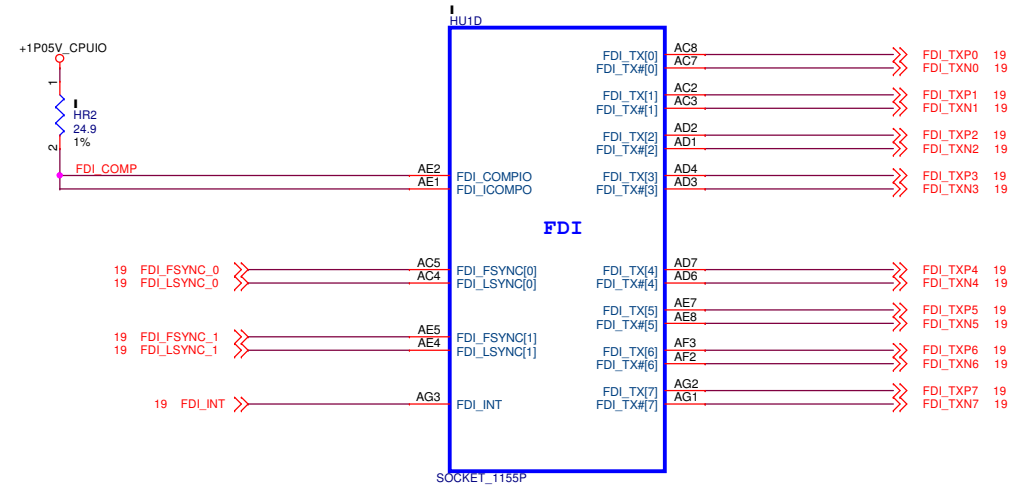
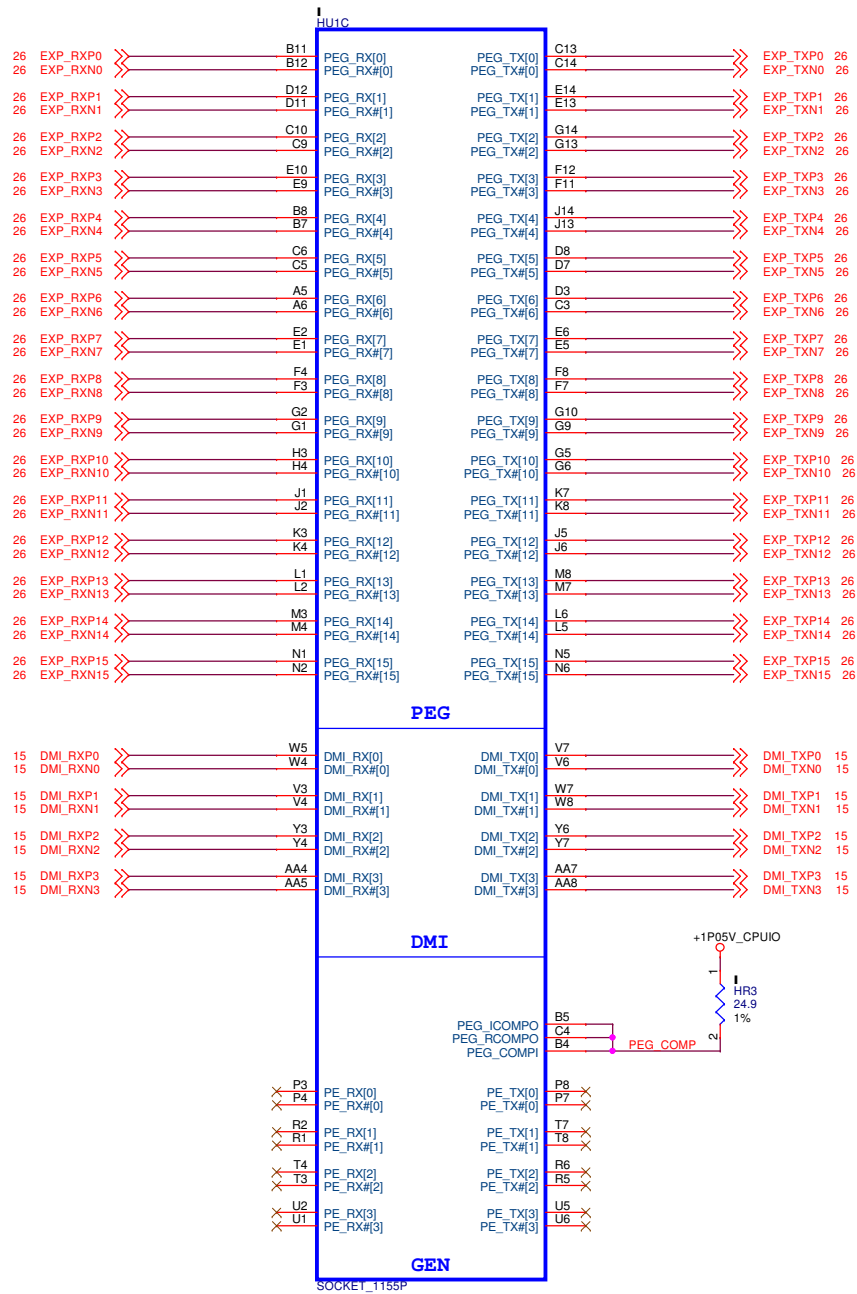
Size A3 Project Name **IPISB-AG** Rev 1.06

Date: Tuesday, February 21, 2012 Sheet 1 of 82

S5 to S0 Power Sequence



Date: **Tuesday, February 21, 2012** Sheet **3** of **82**



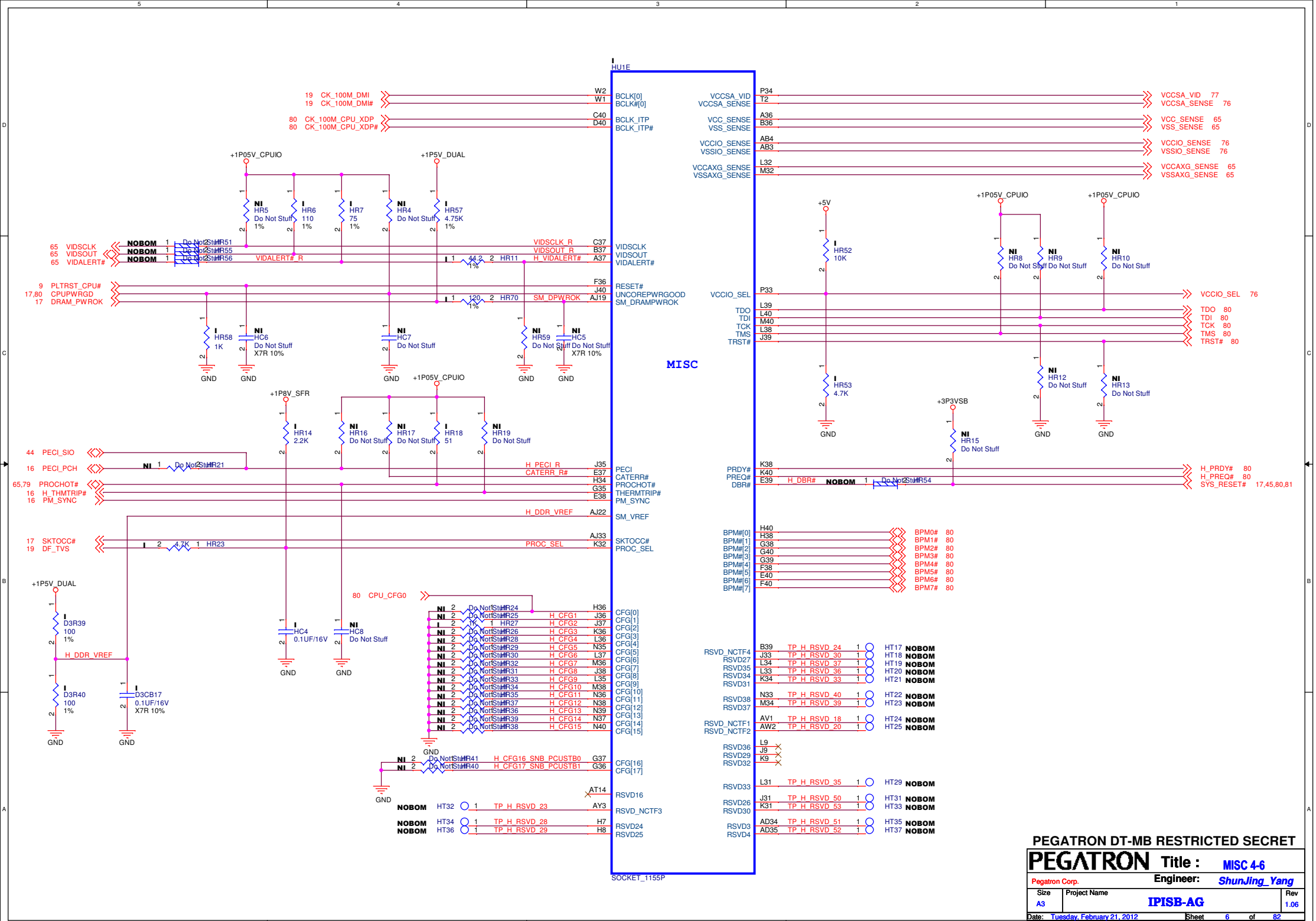
PEGATRON DT-MB RESTRICTED SECRET

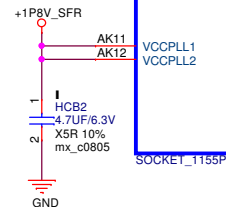
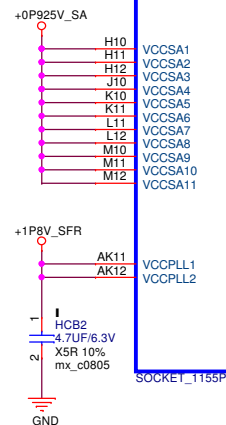
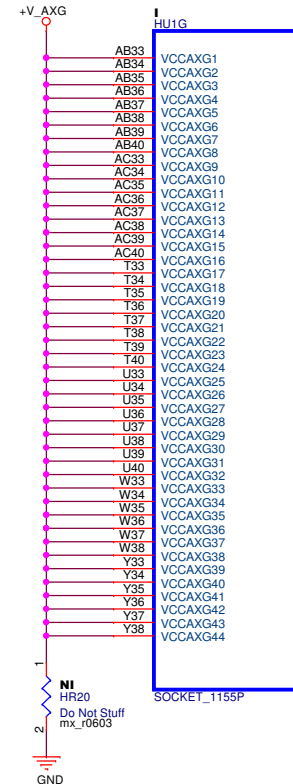
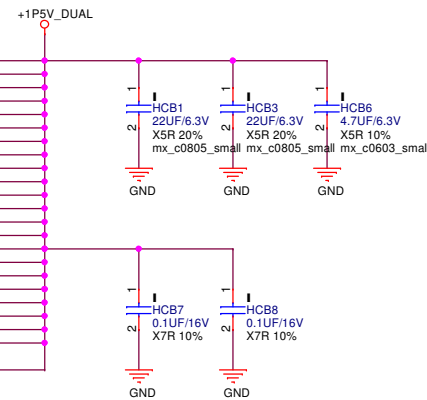
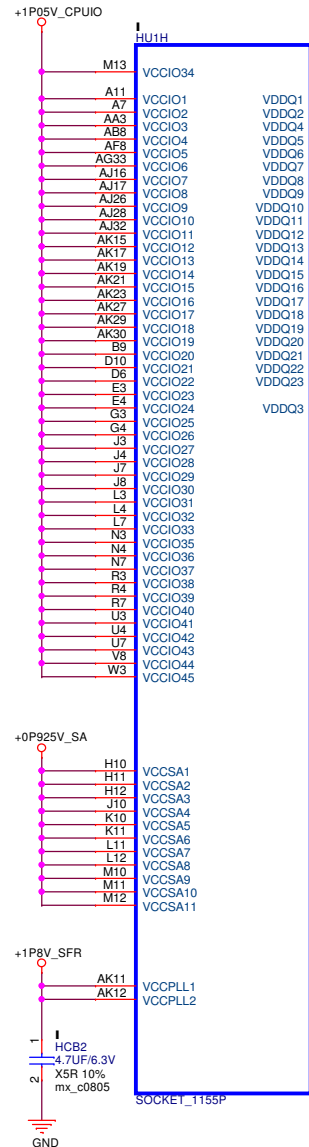
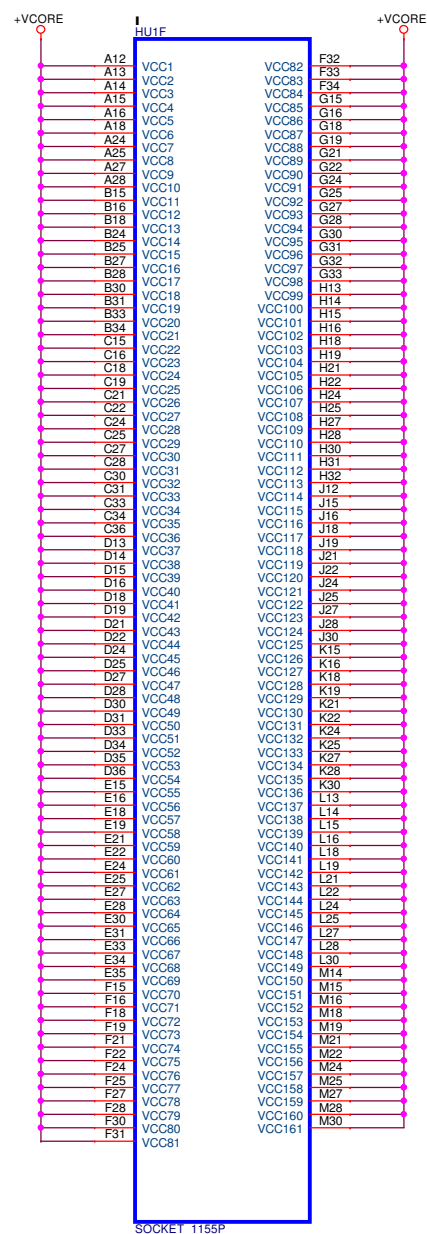
PEGATRON Title : **PCIe/DMI/FDI 3-6**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3 Project Name **IPISB-AG** Rev 1.06

Date: Tuesday, February 21, 2012 Sheet 5 of 82





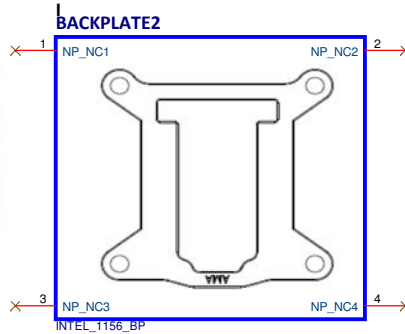
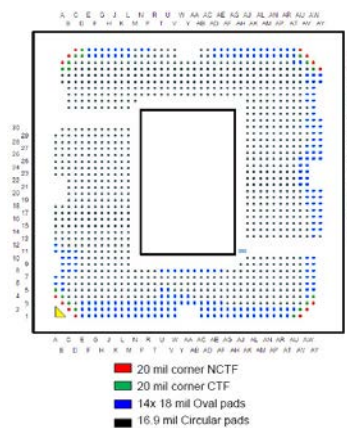
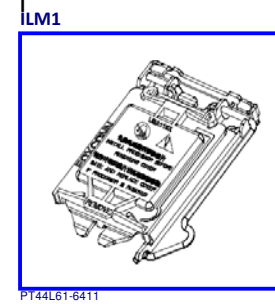
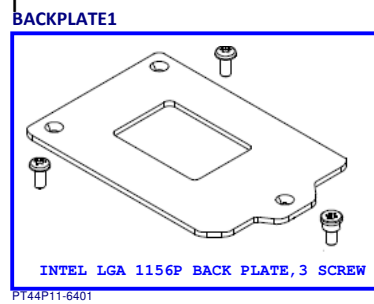
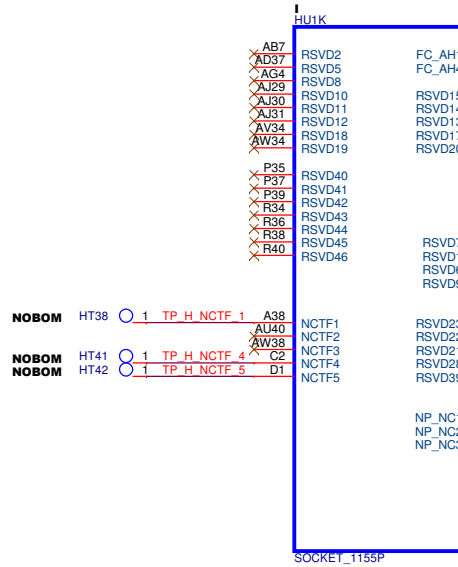
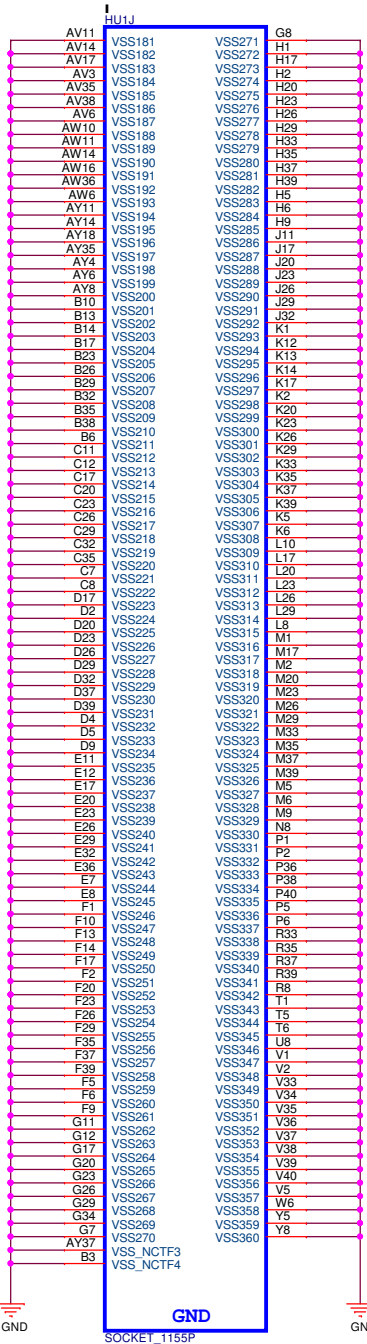
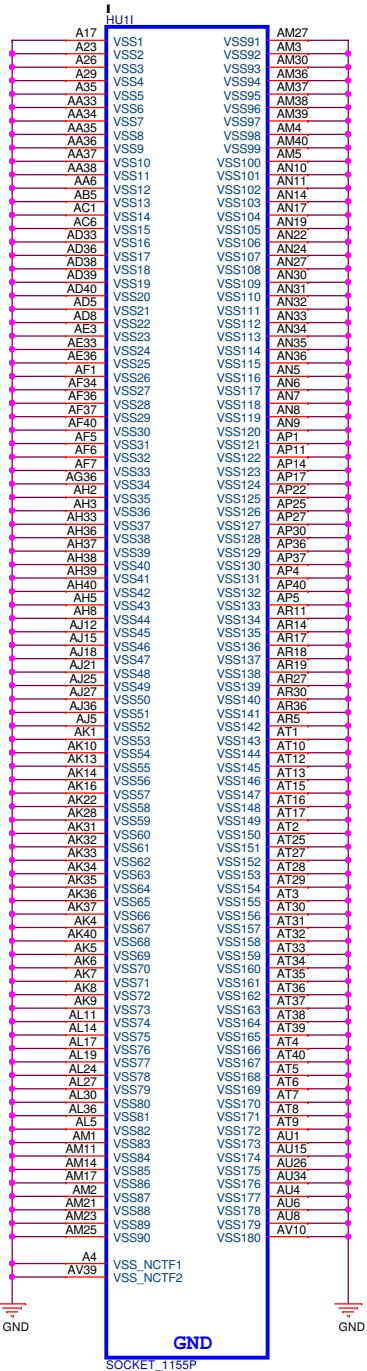
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCC 5 - 6

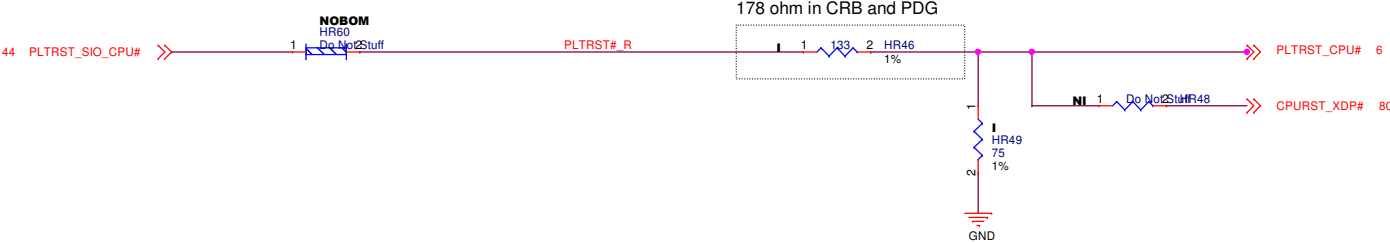
Pegatron Corp. Engineer: ShunJing_Yang

Size	Project Name	Rev
A3	IPISB-AG	1.06

Date: Tuesday, February 21, 2012 Sheet 7 of 82



PLTRST_CPU#



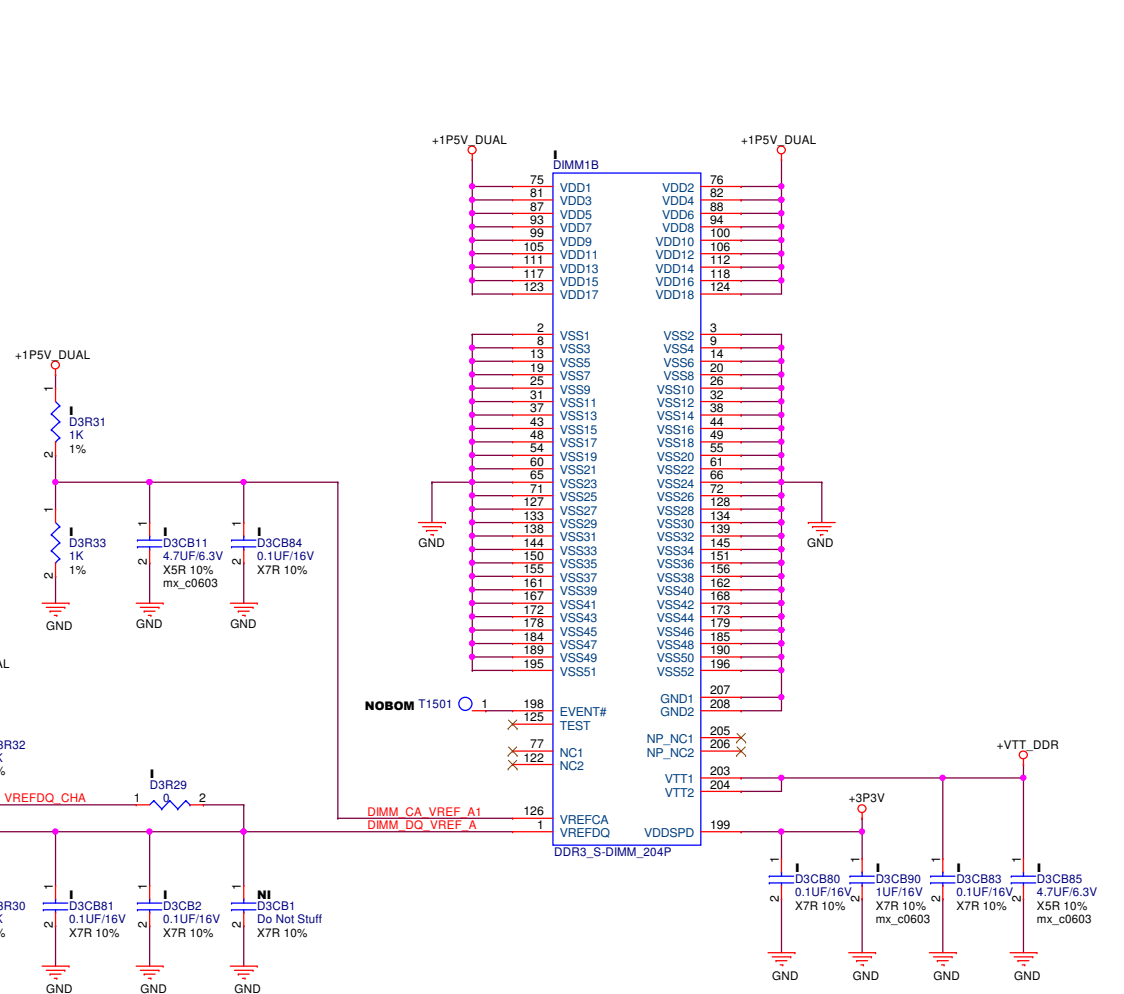
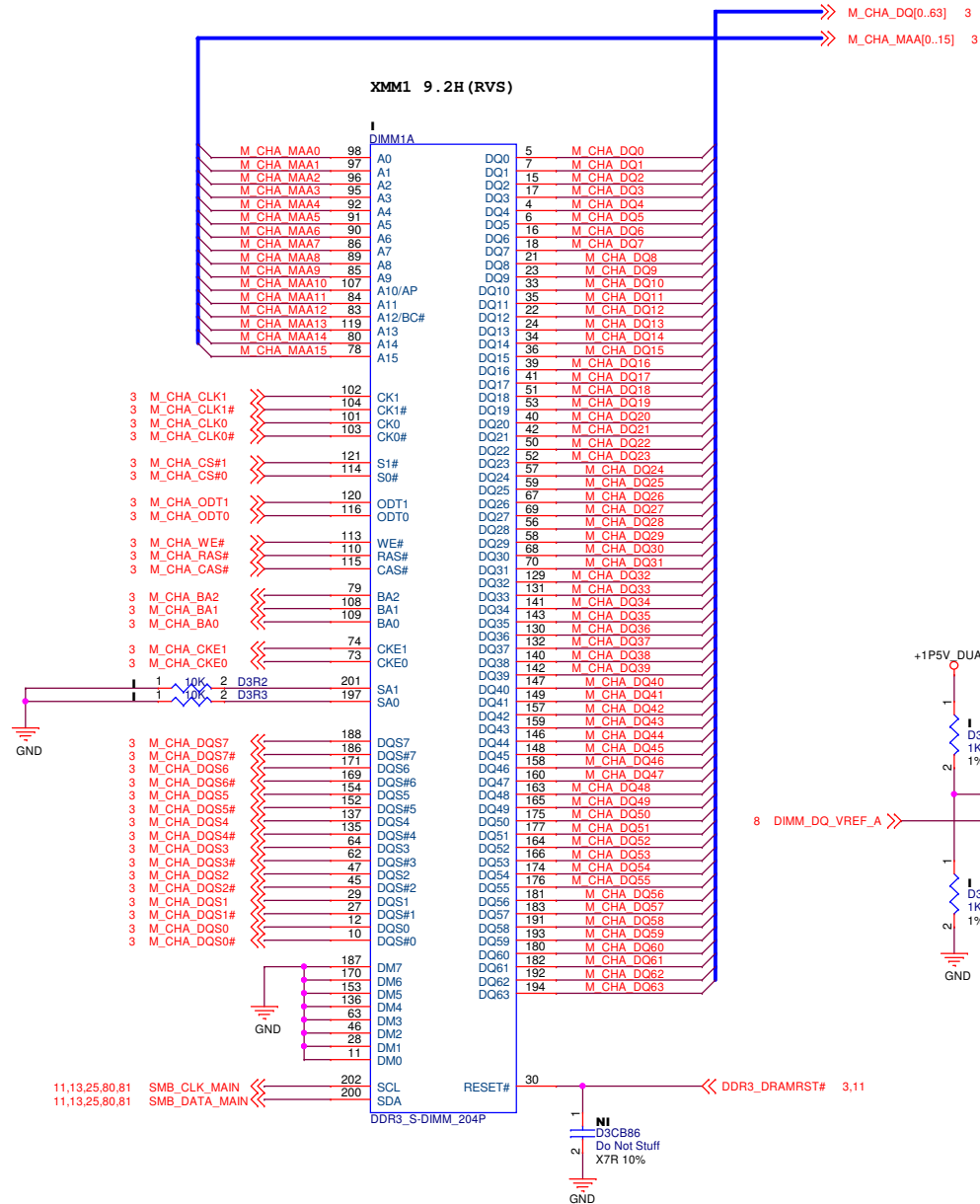
PEGATRON DT-MB RESTRICTED SECRET

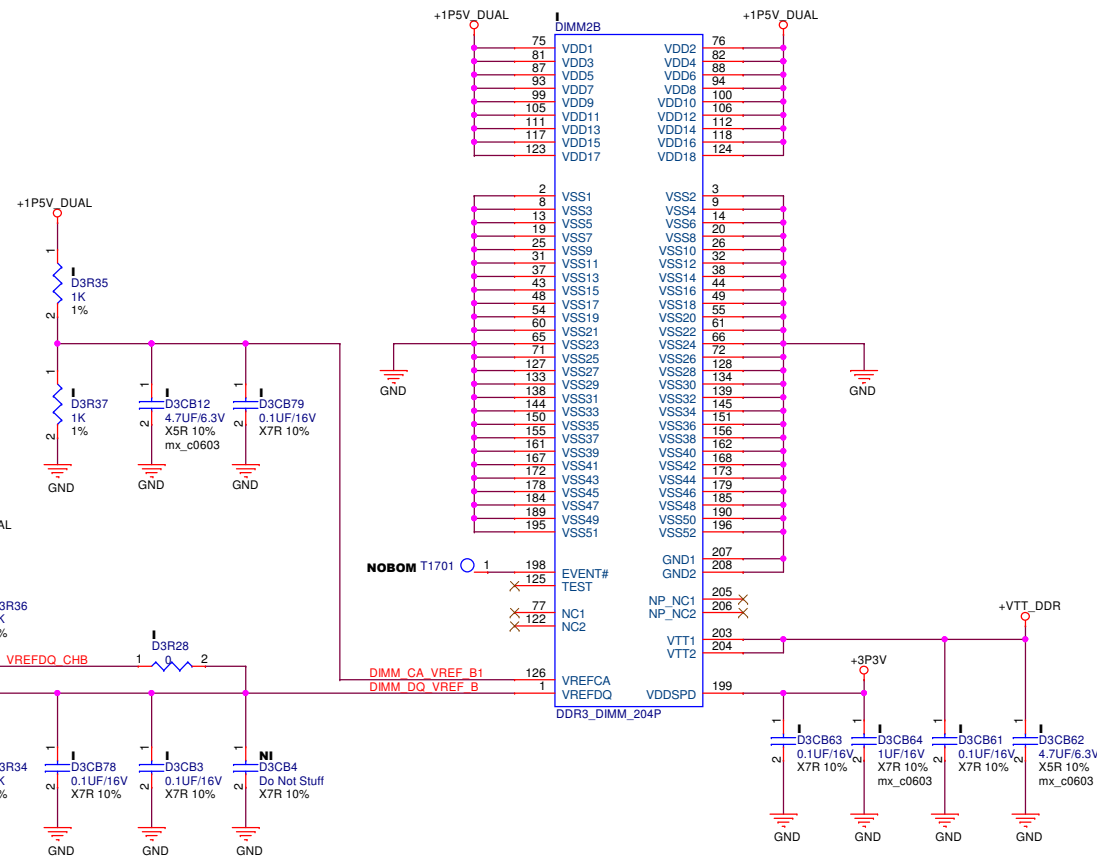
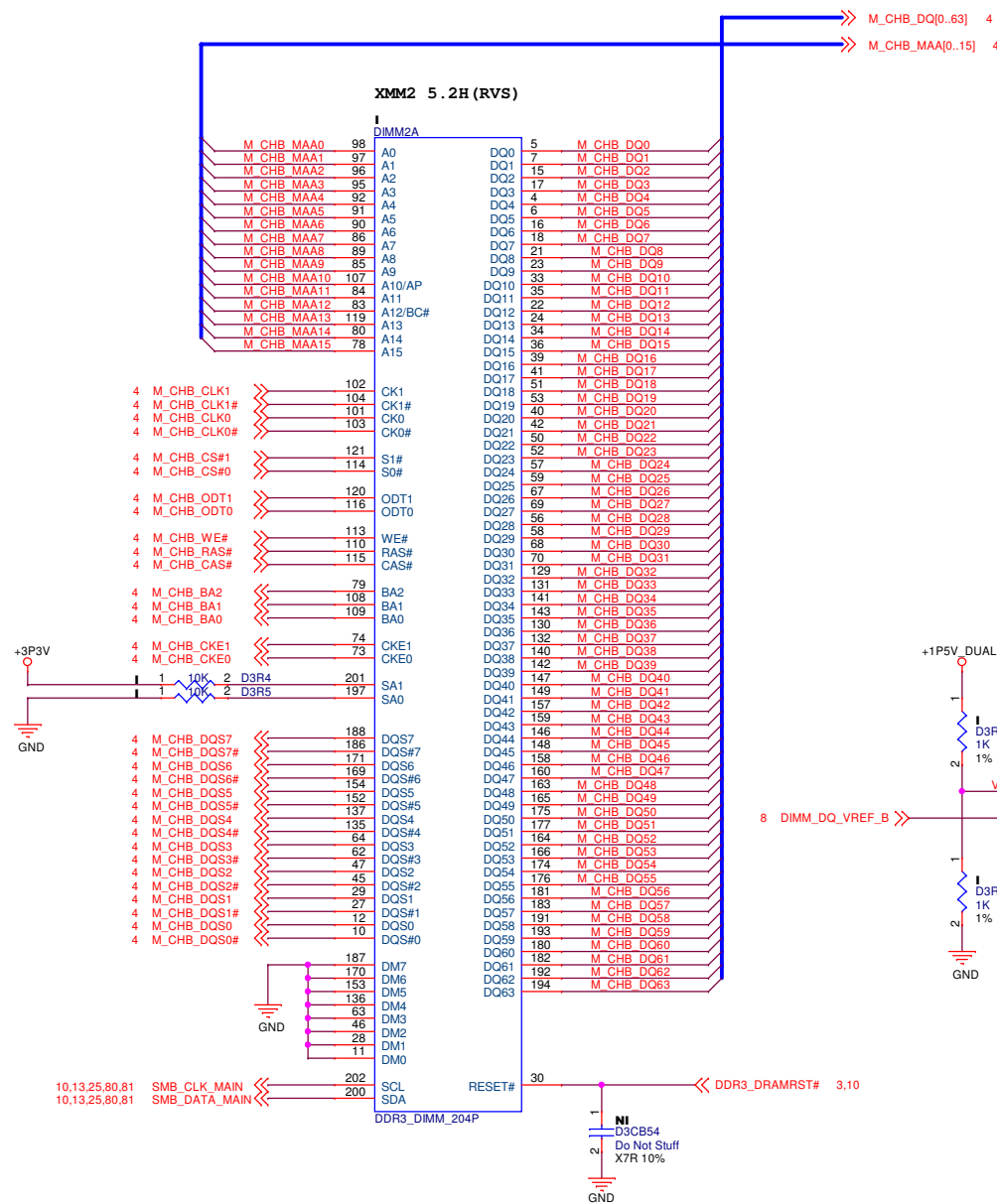
PEGATRON Title : **PLTRST_CPU#**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **9** of **82**





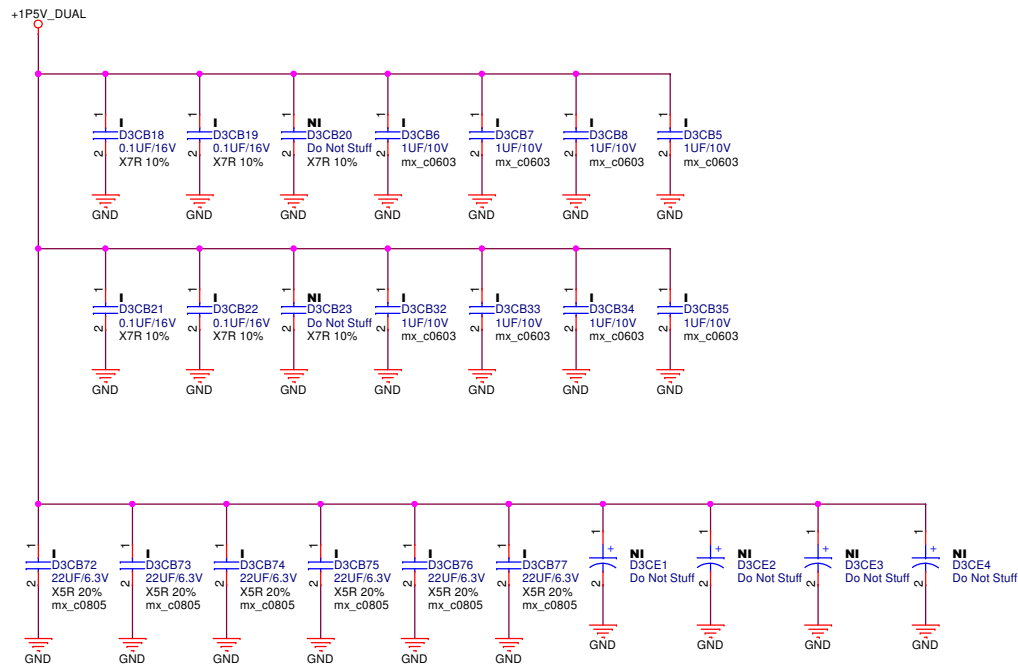
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **DDR3 CHANNEL B**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size **A3** Project Name **IPISB-AG** Rev **1.06**

Date: **Tuesday, February 21, 2012** Sheet **11** of **82**



PEGATRON DT-MB RESTRICTED SECRET

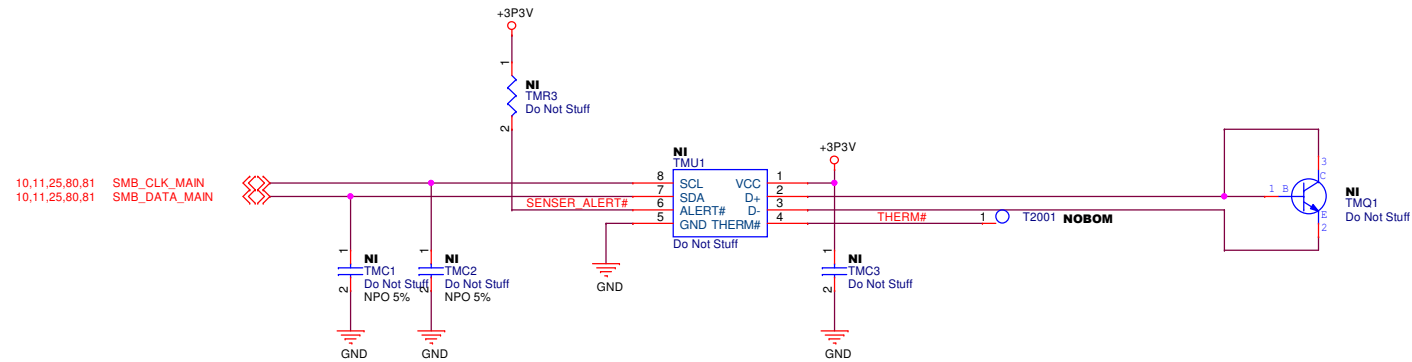
PEGATRON Title : **DDR3 TERMINATION**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **12** of **82**

20120204 PEGATRON DT-MB RESTRICTED SECRET

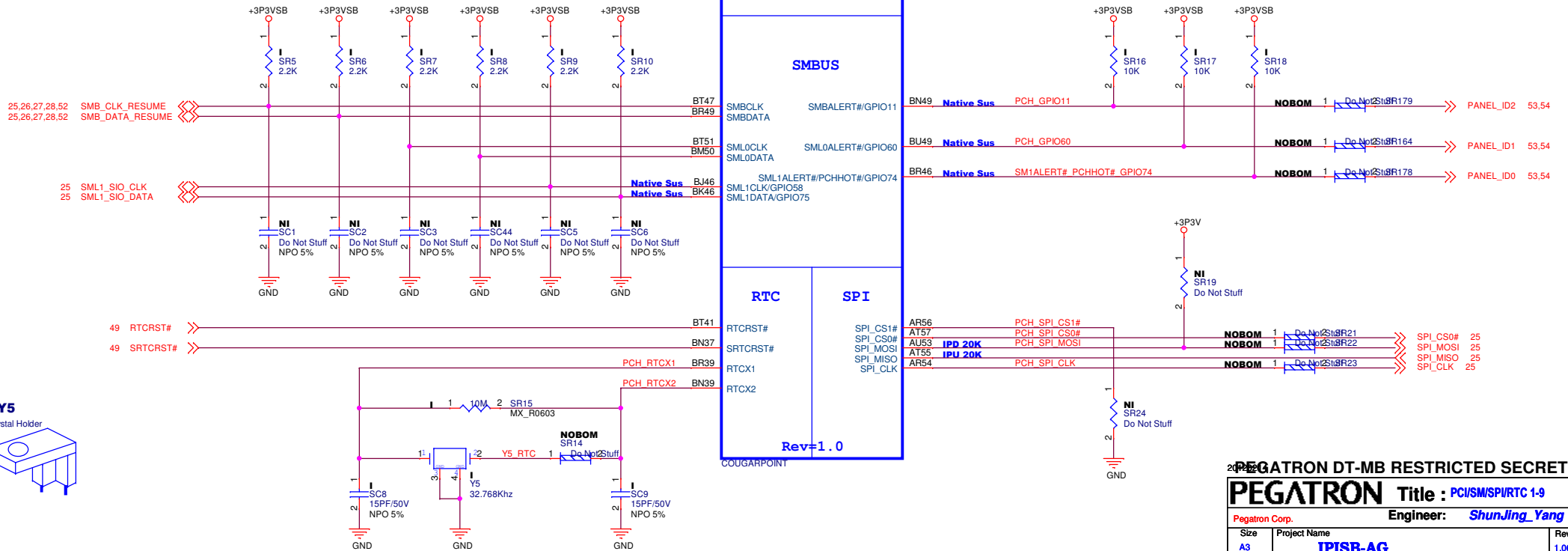
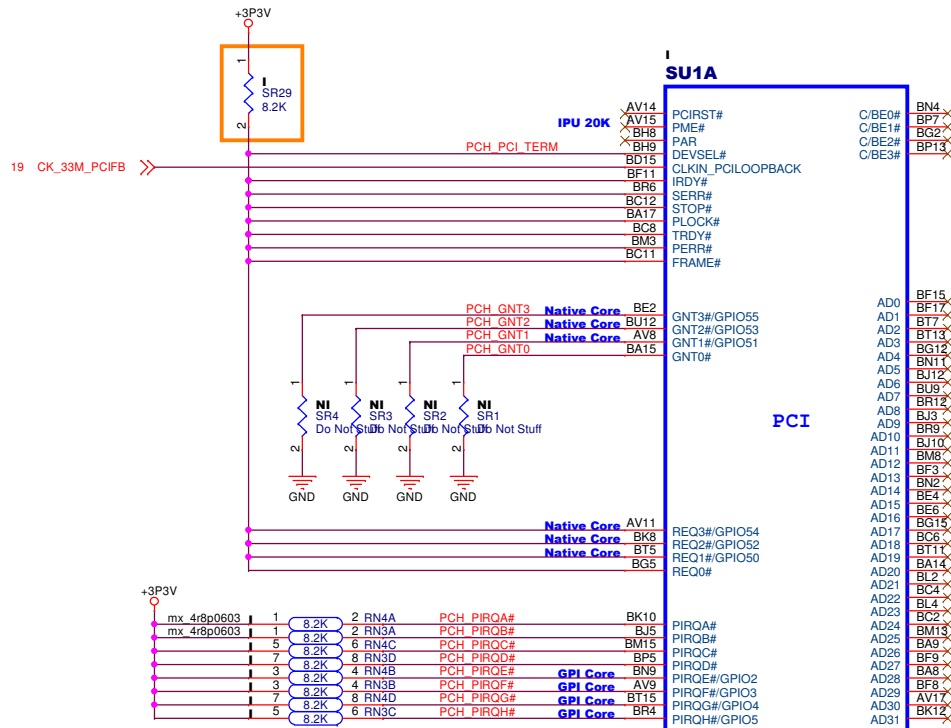


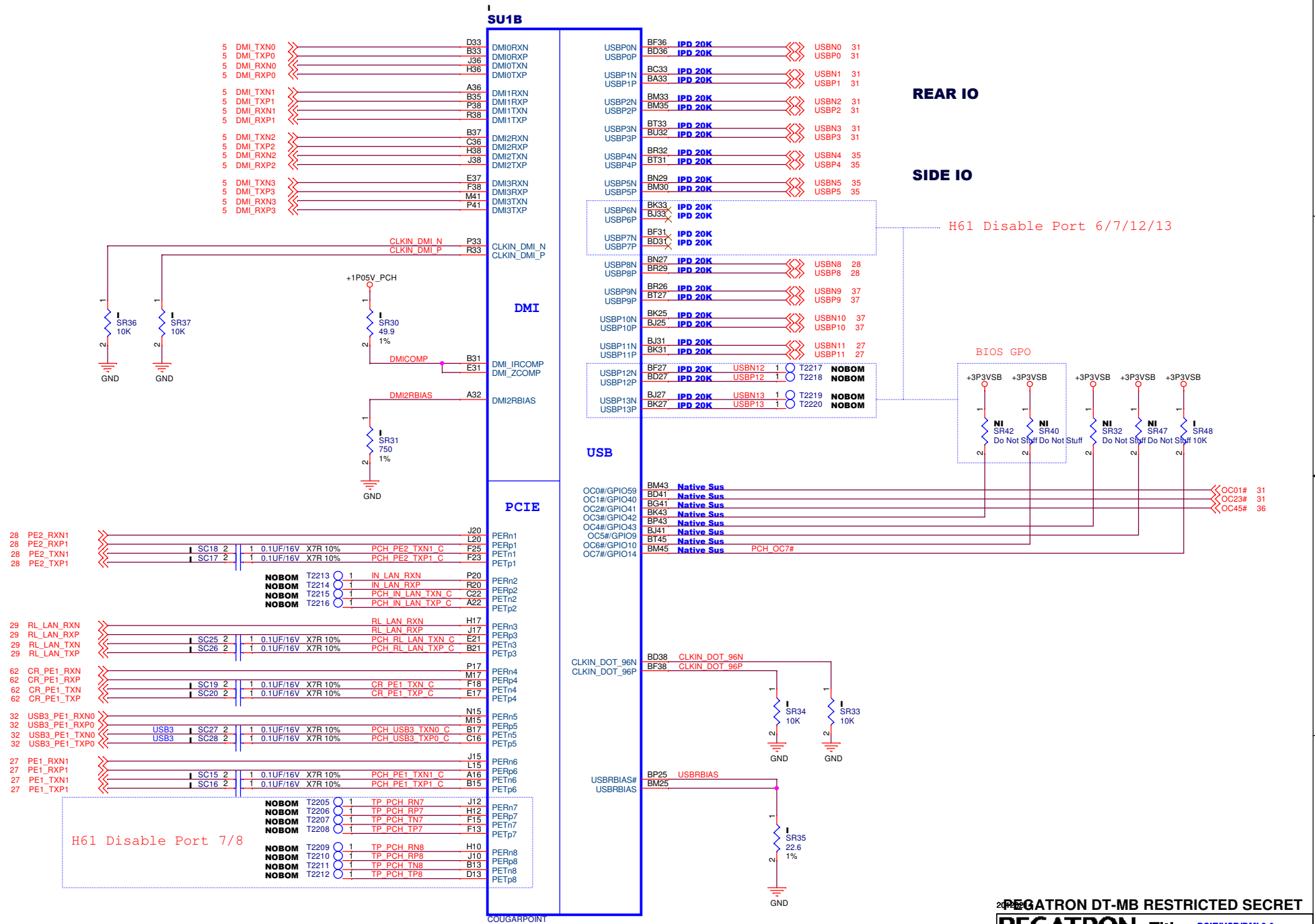
PEGATRON Title : **TEMP SENSOR**

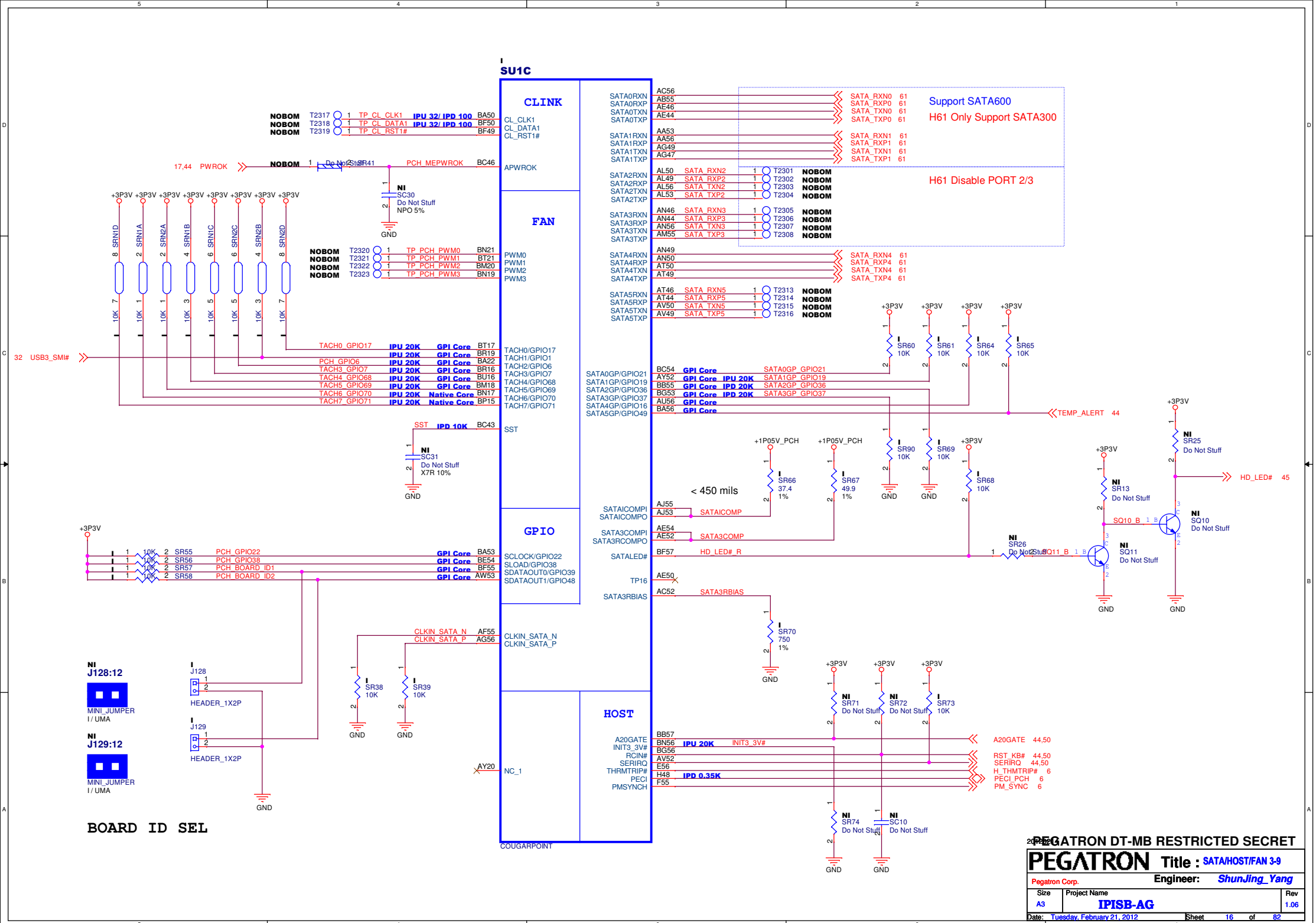
Pegatron Corp. **Engineer:** *ShunJing_Yang*

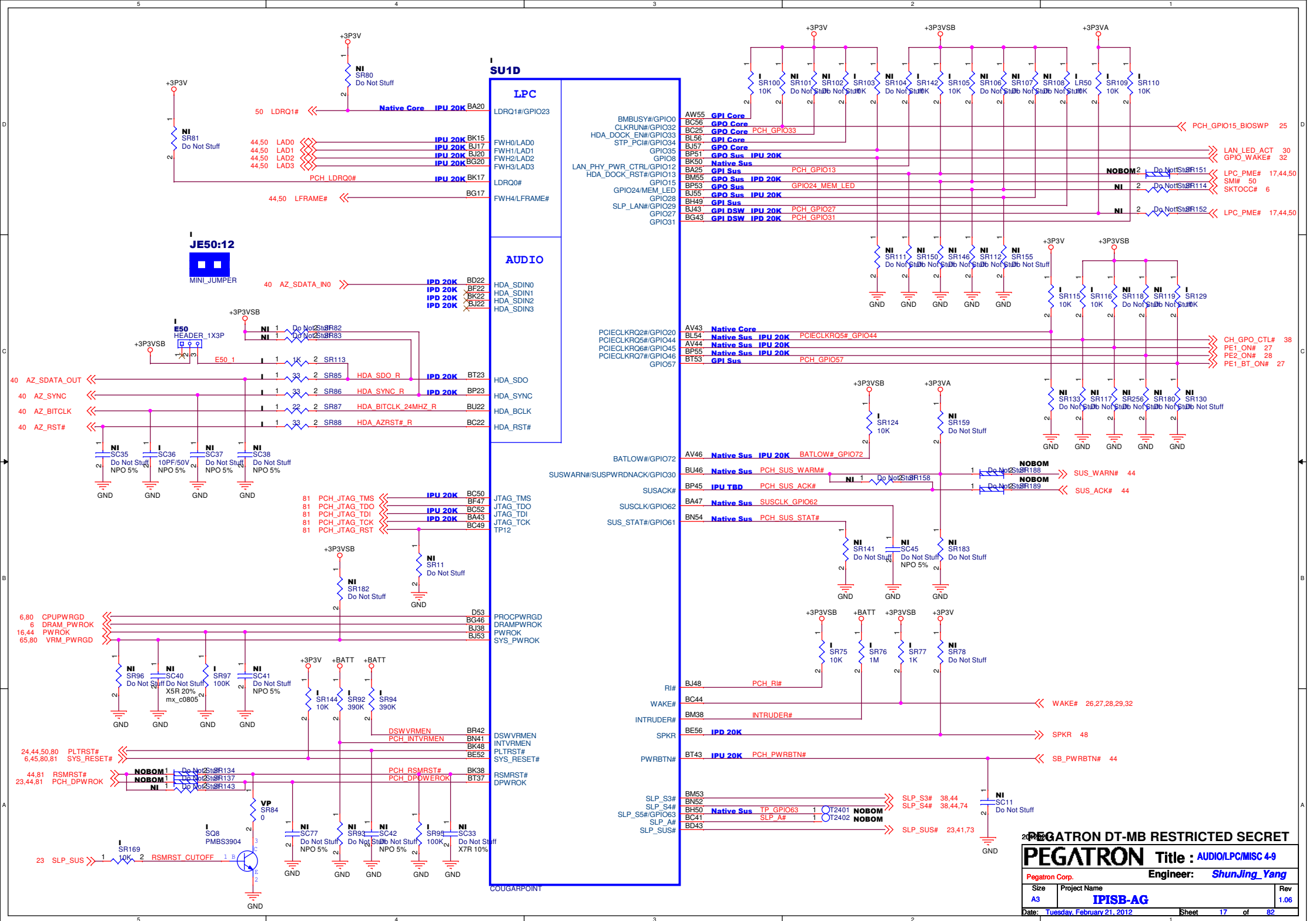
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

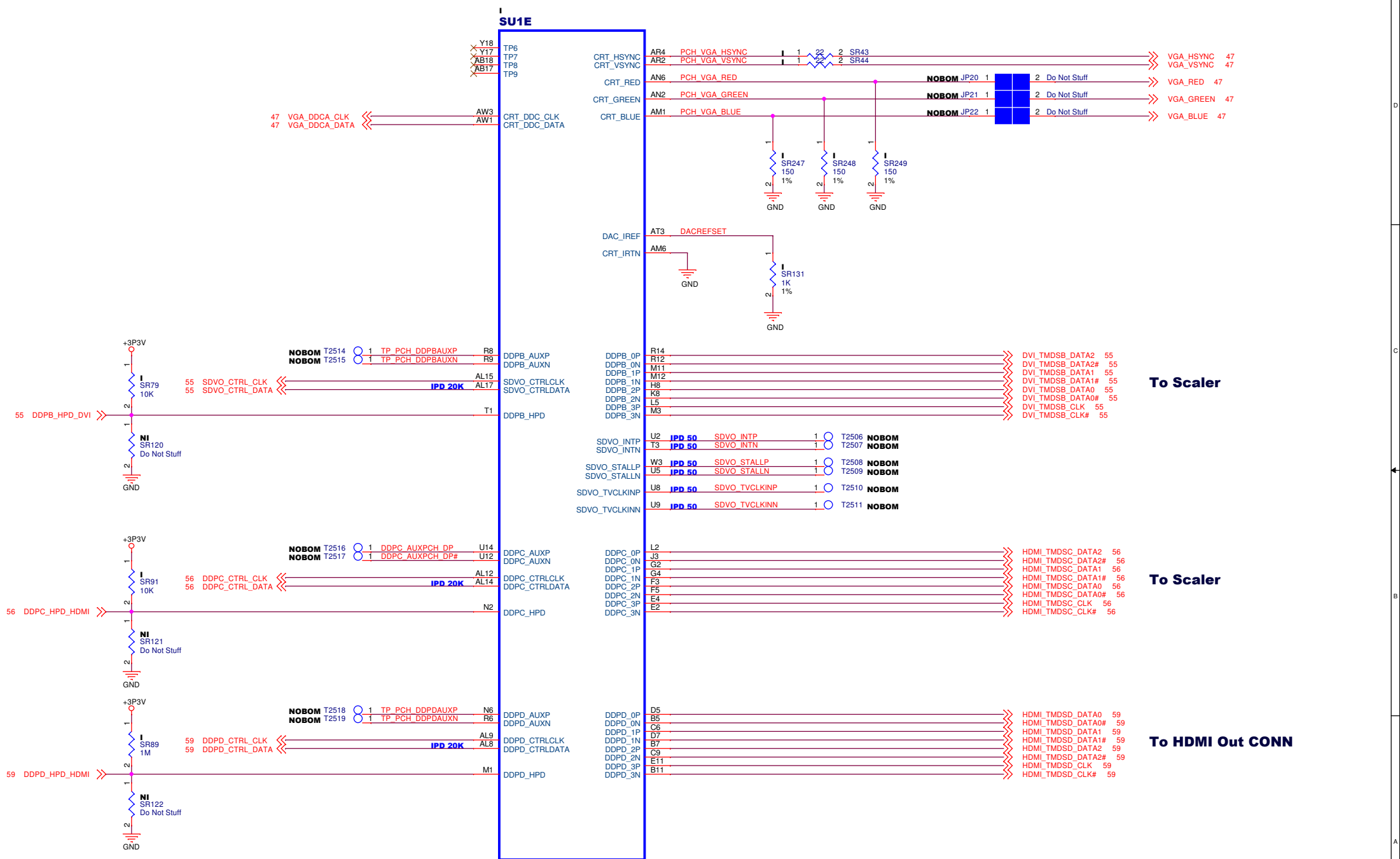
Date: Tuesday, February 21, 2012 Sheet 13 of 82

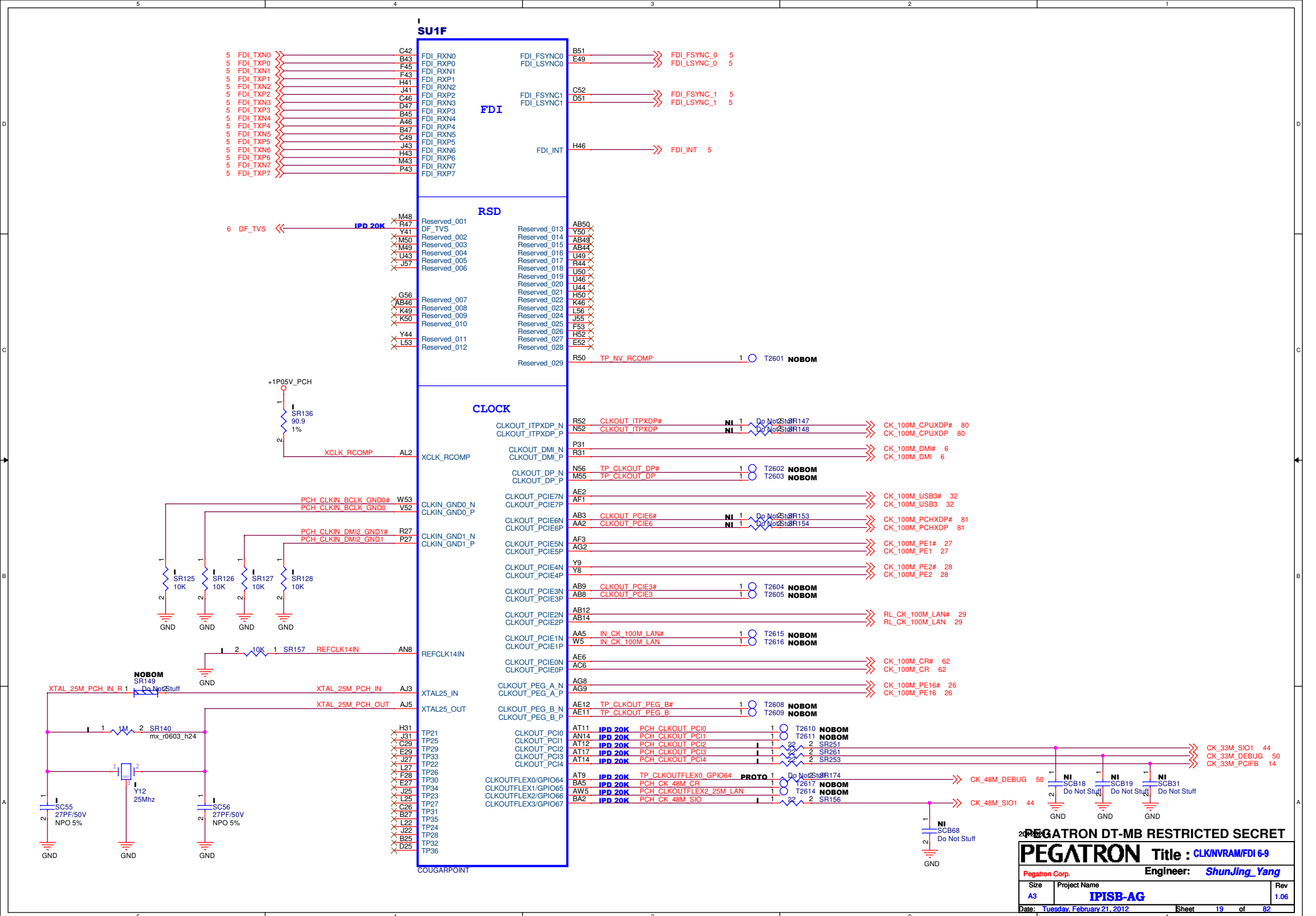


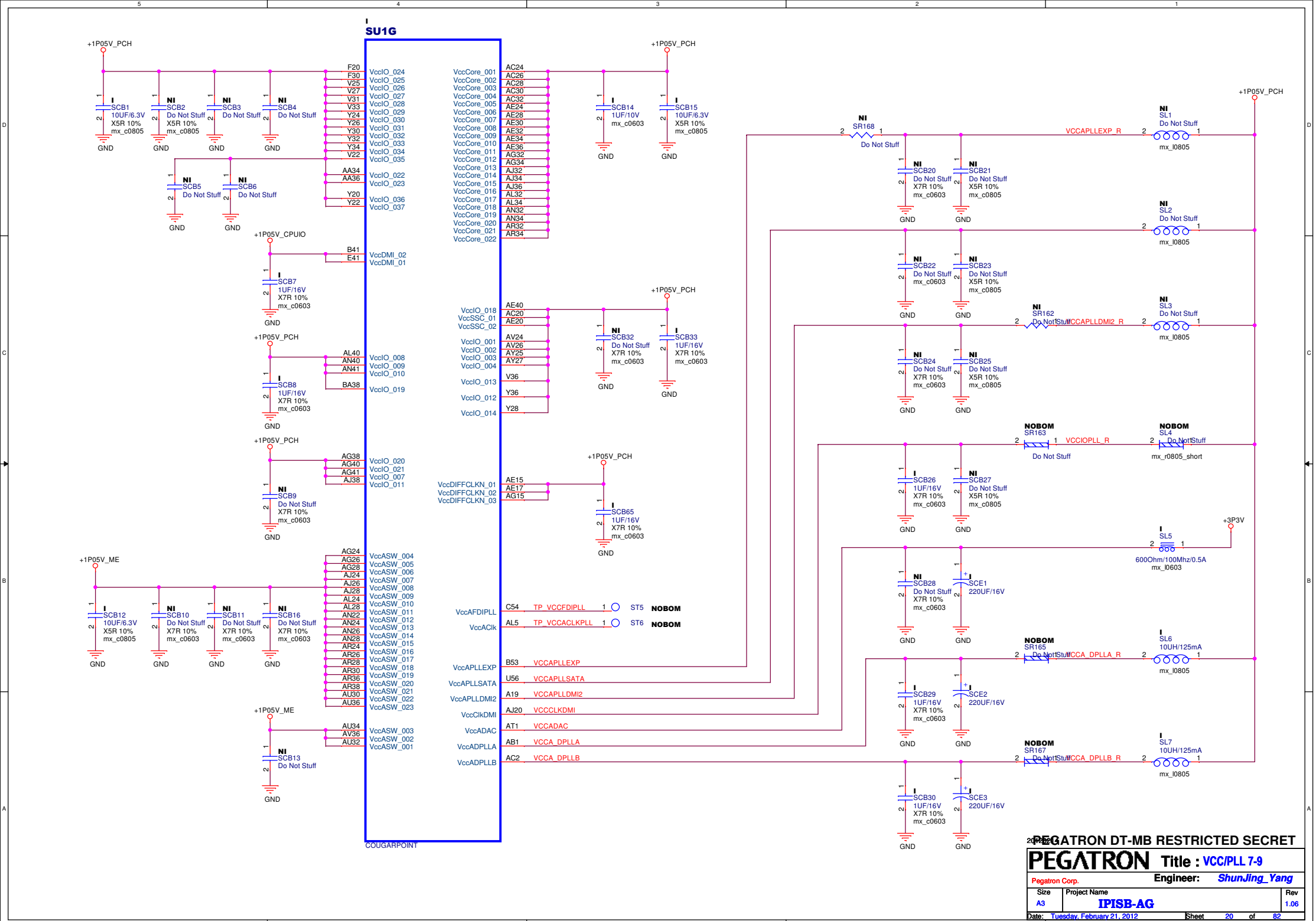


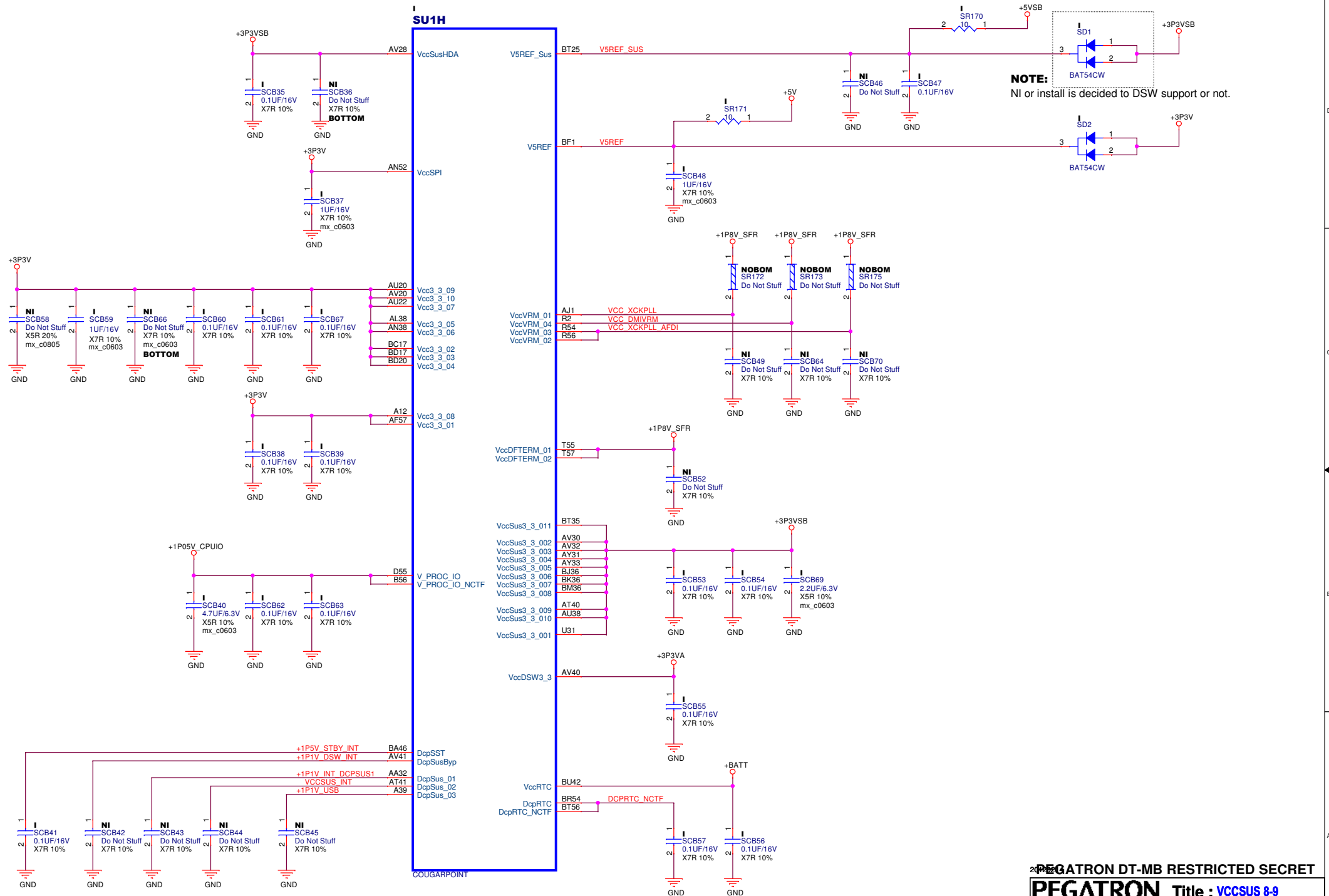




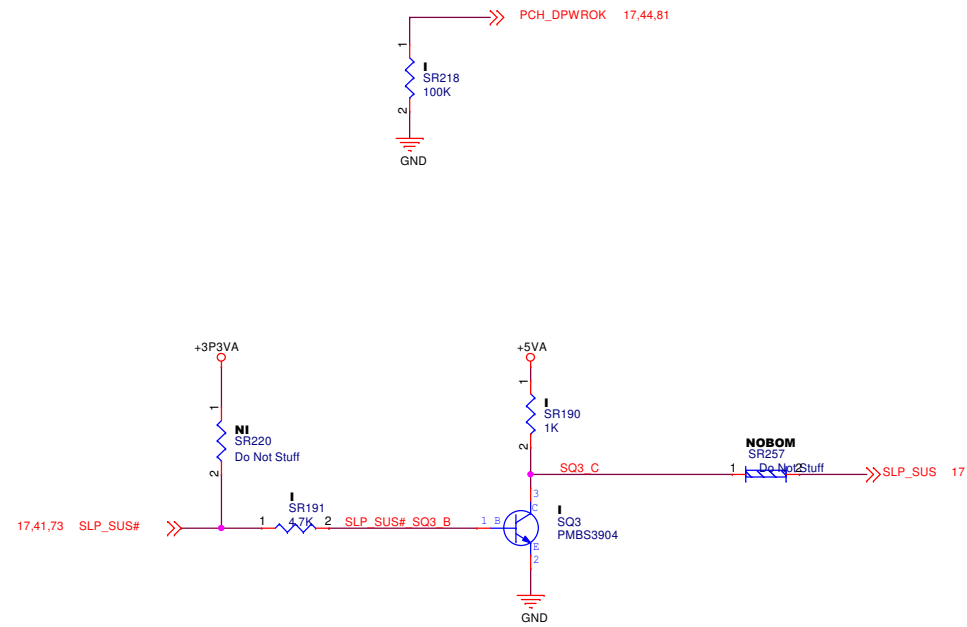








PEGATRON DT-MB RESTRICTED SECRET



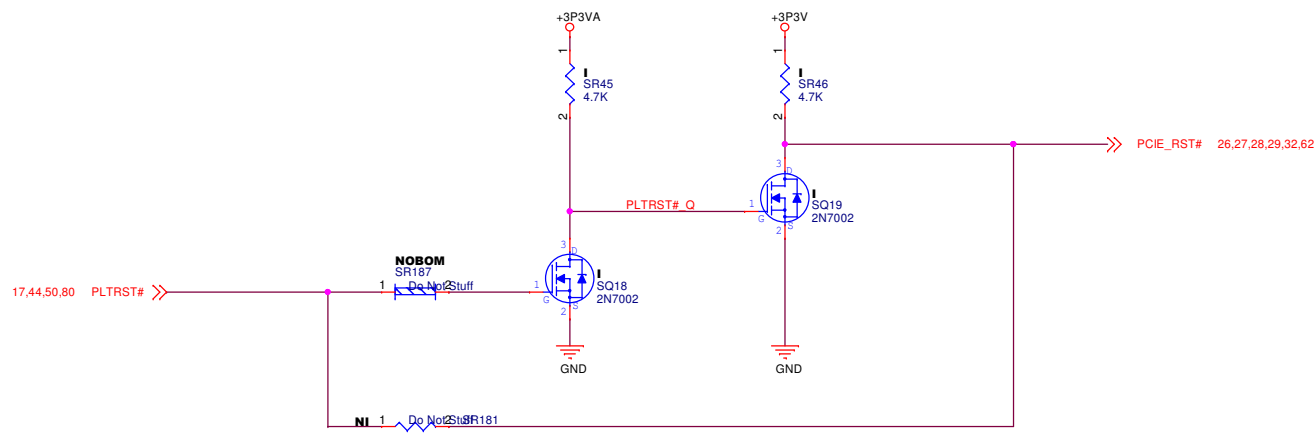
PEGATRON Title : PCH_DPWROK & SLP_SUS

Pegatron Corp. Engineer: ShunJing_Yang

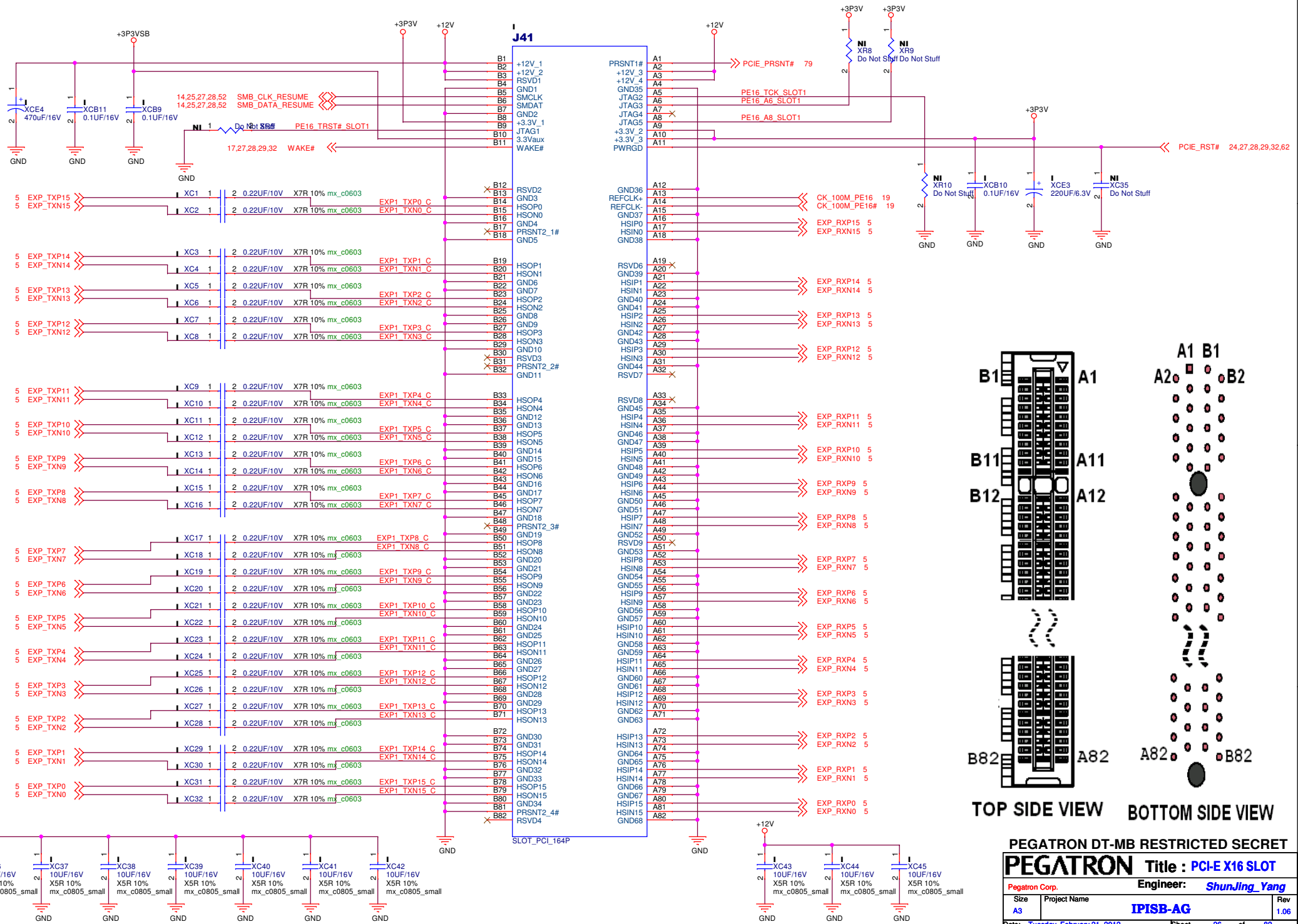
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **23** of **82**

RSMRST CIRCUIT



PCI EXPRESS X16 Graphics Card Slot



PEGATRON DT-MB RESTRICTED SECRET

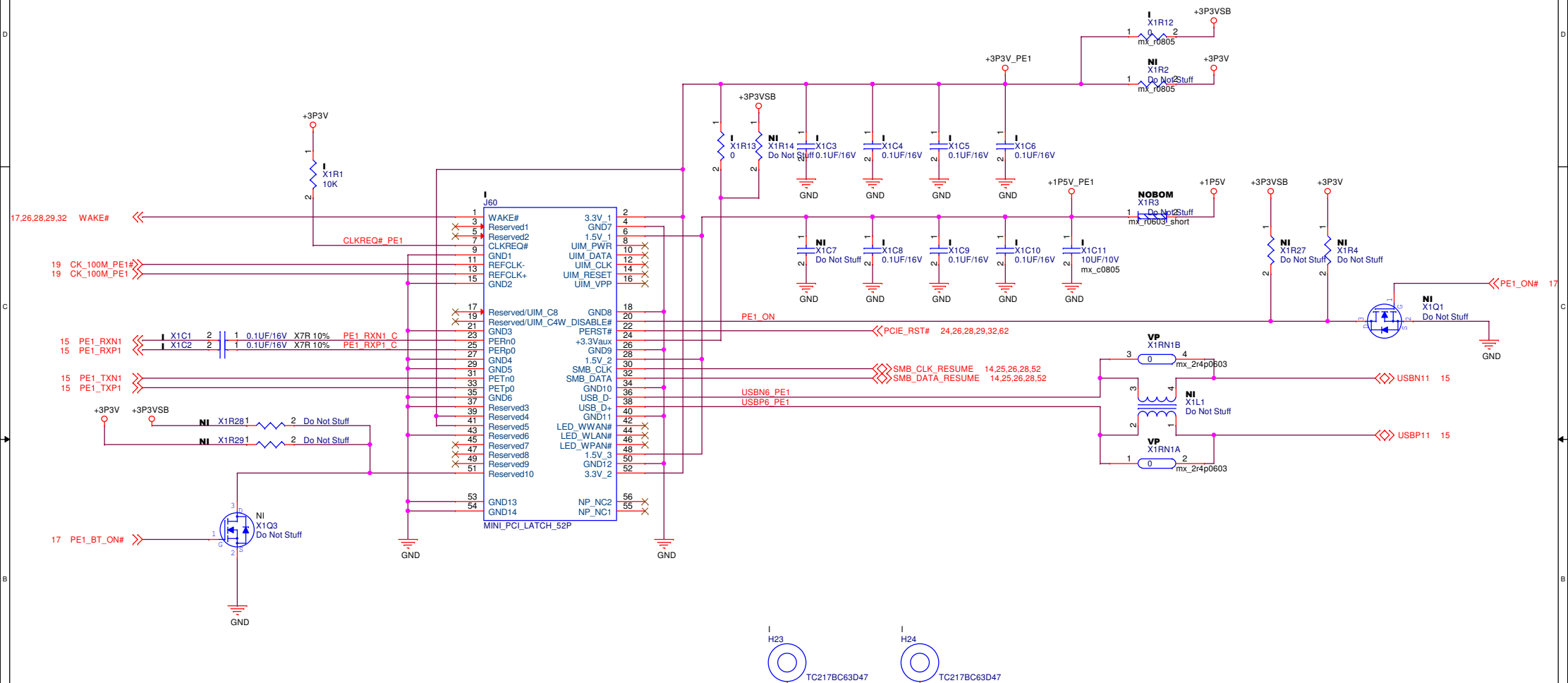
PEGATRON Title : PCI-E X16 SLOT

Engineer: *ShunJing Yang*

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: Tuesday, February 21, 2012 Sheet 26 of 82

Mini-PCIE Slot (Half Card) for Wifi



PEGATRON DT-MB RESTRICTED SECRET

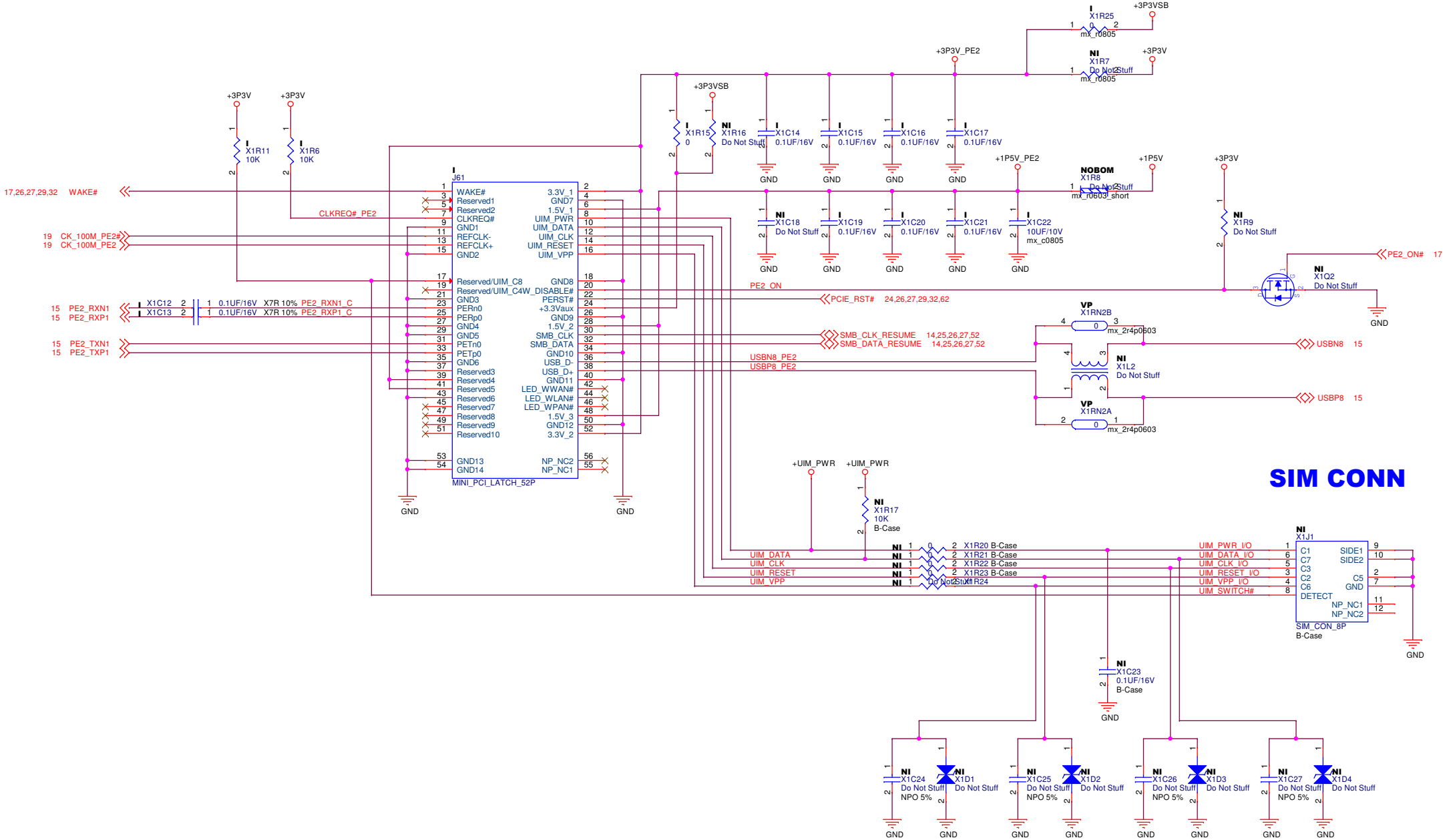
PEGATRON Title : **MINI-PCIE SLOT-1**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **27** of **82**

Mini-PCIE Slot (Full Card)



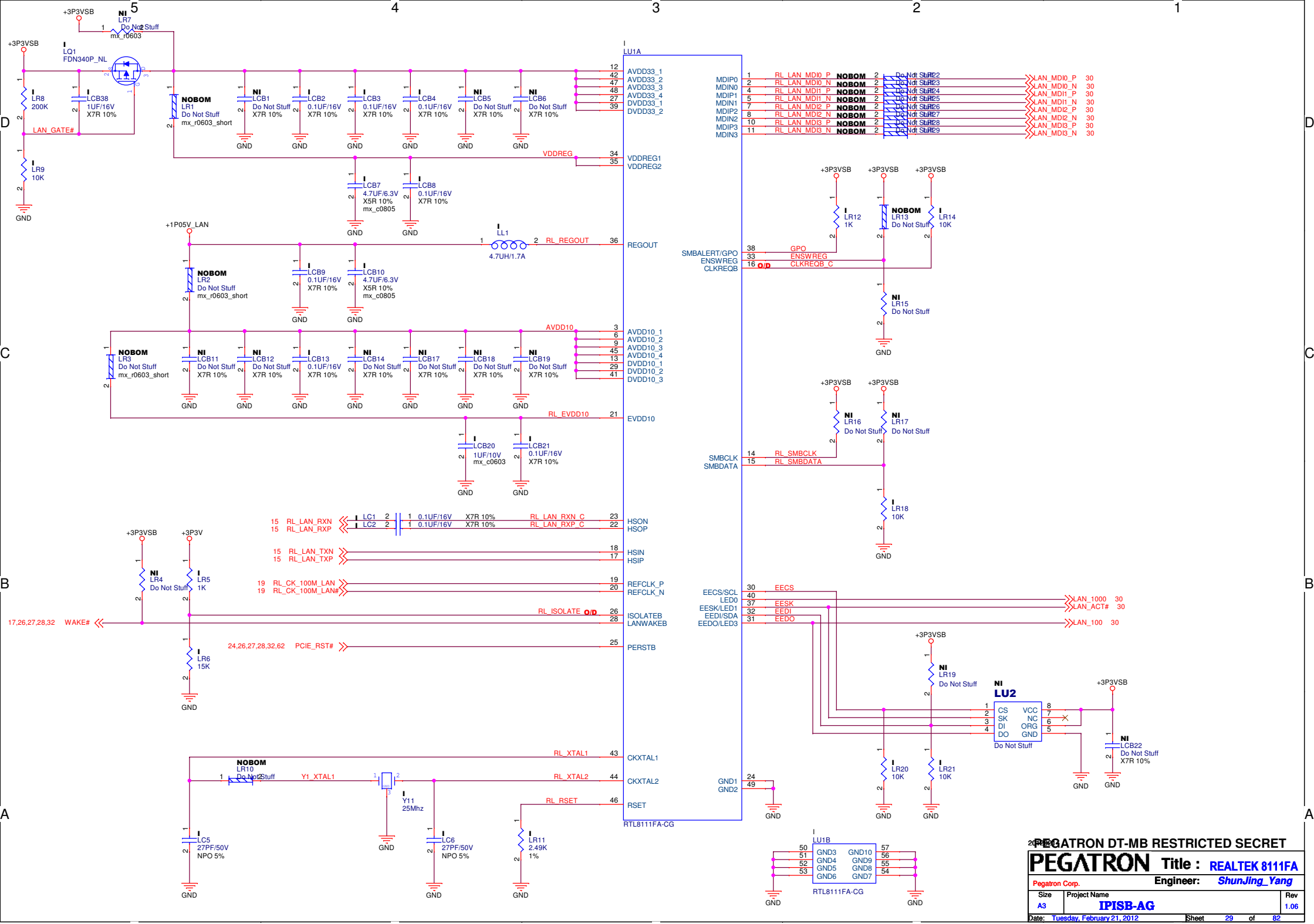
PEGATRON DT-MB RESTRICTED SECRET

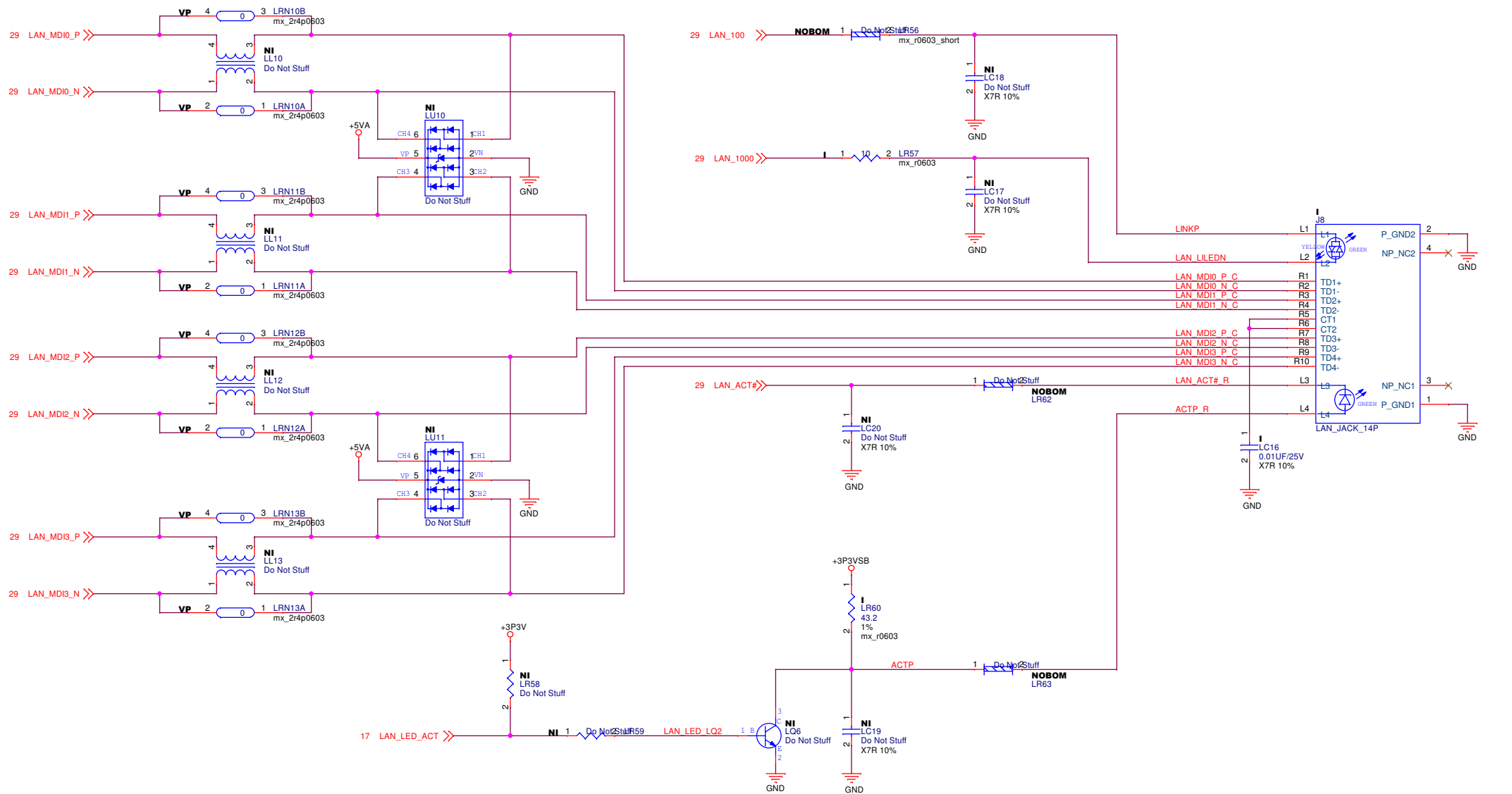
PEGATRON Title : MINI-PCIE SLOT-2

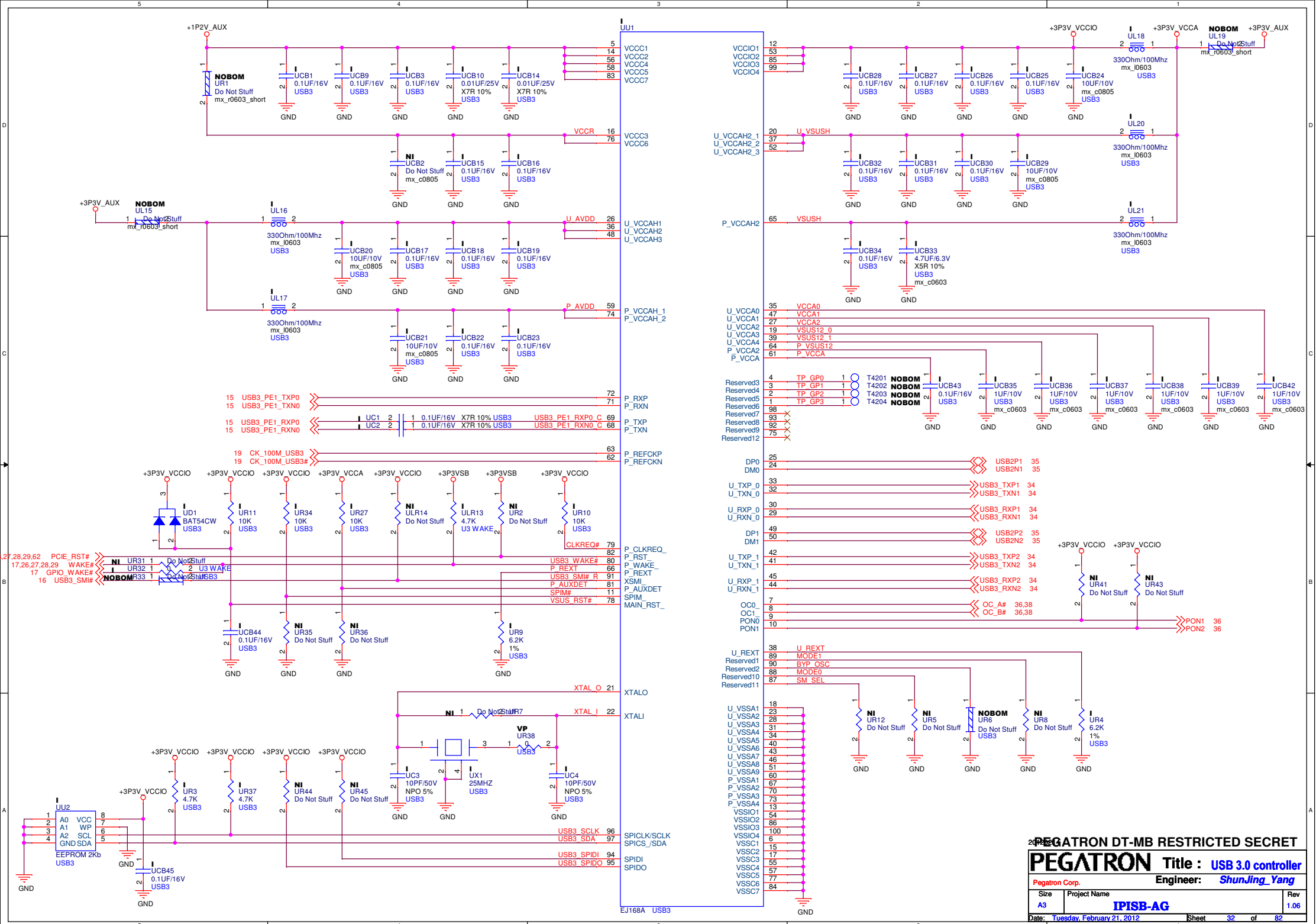
Pegatron Corp. Engineer: ShunJing_Yang

Size A3 Project Name IPISB-AG Rev 1.06

Date: Tuesday, February 21, 2012 Sheet 28 of 82

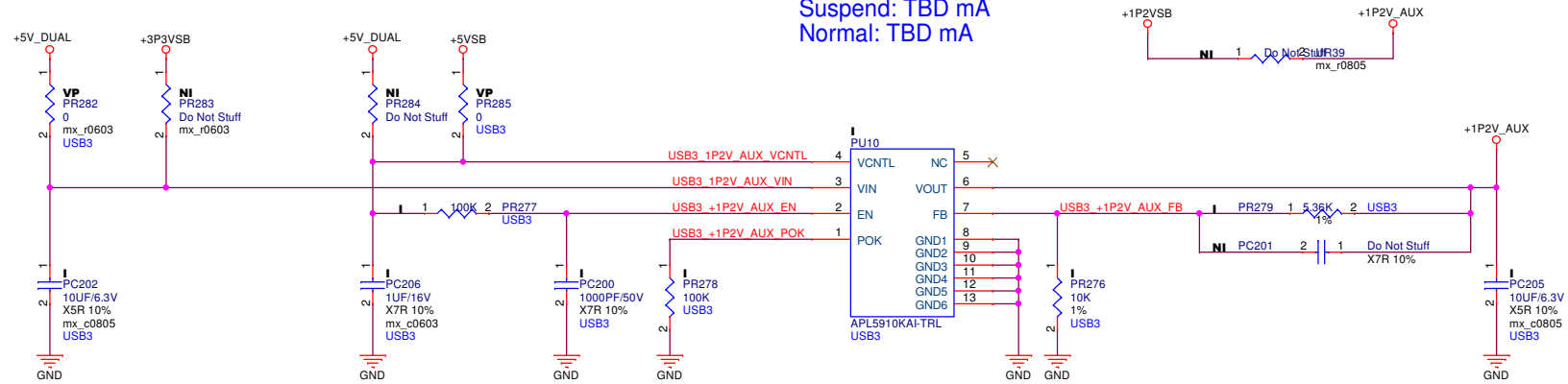






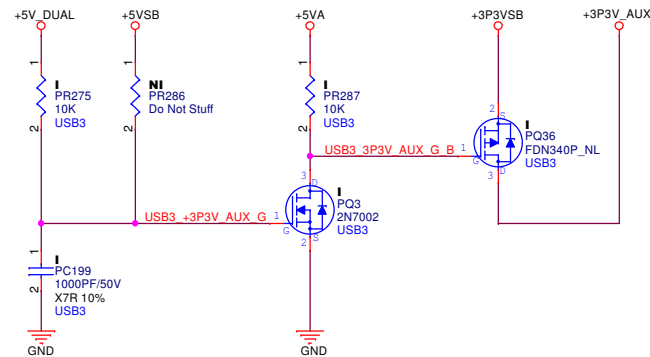
+1P2V_AUX

Suspend: TBD mA
Normal: TBD mA



+3P3V_AUX

Suspend: TBD mA
Normal: TBD mA



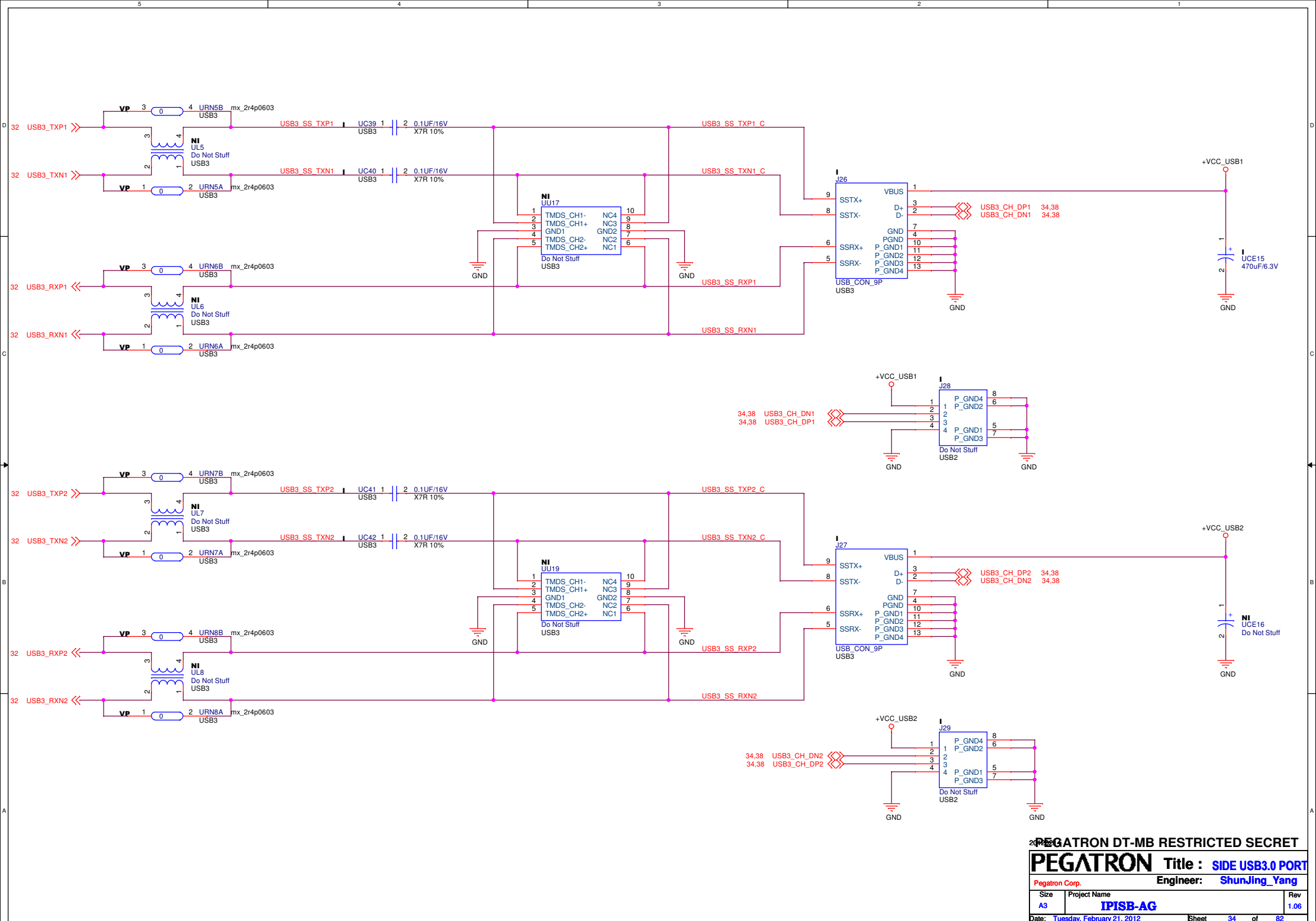
PEGATRON DT-MB RESTRICTED SECRET

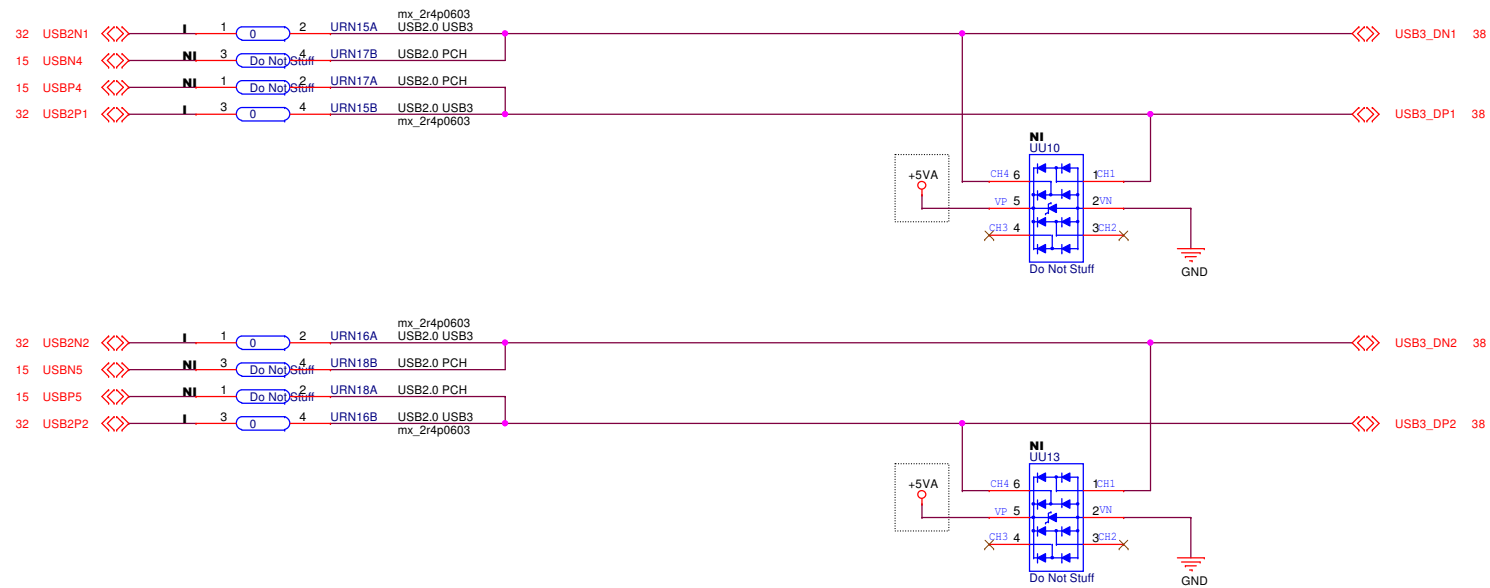
PEGATRON Title : **USB POWER**

Pegatron Corp. Engineer: **ShunJing_Yang**

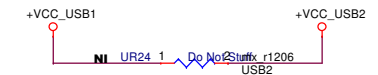
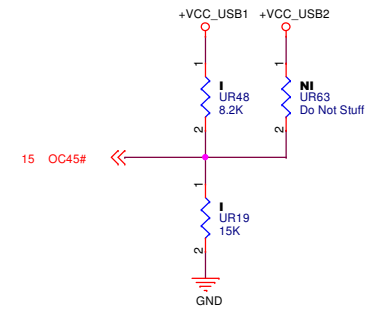
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **33** of **82**

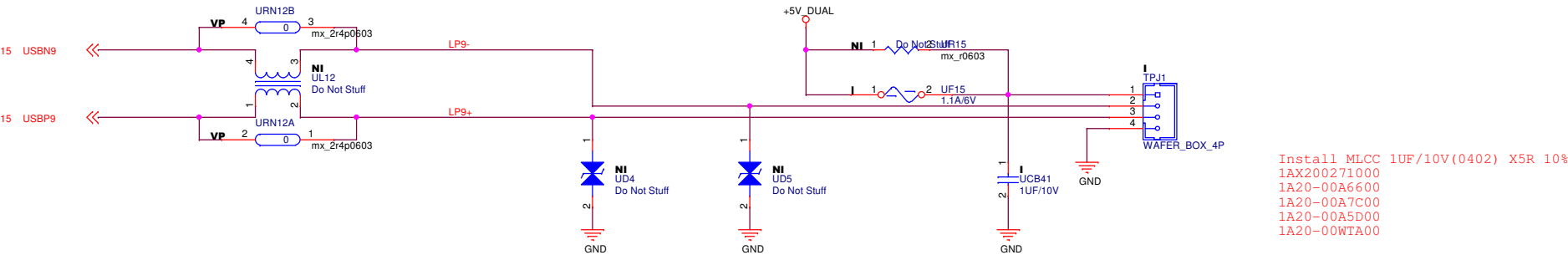




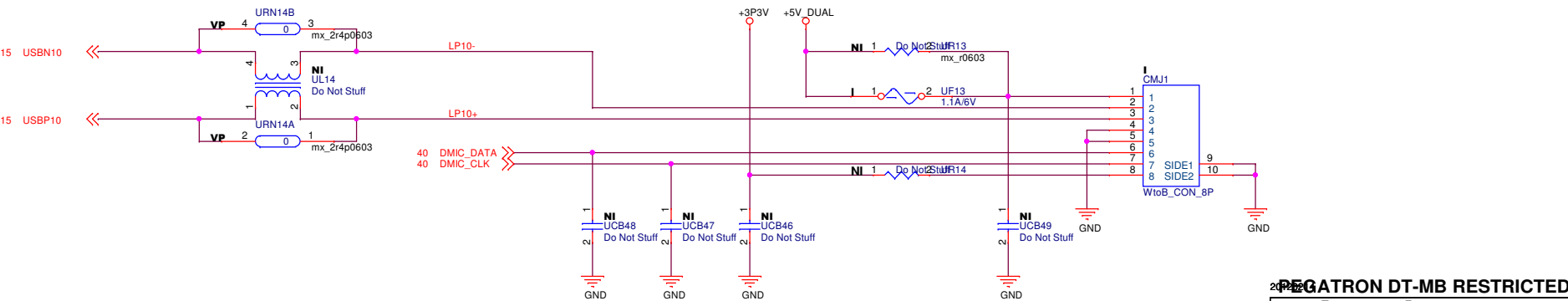
The schematic diagram illustrates the power supply section of the NI-6009 module. It shows the connection of various power rails to the module's internal components. Key components include resistors UR20, UR40, UR21, and capacitors UF3, UF1, UC37, and UU11. The diagram also shows the connection of the module's pins 32, 38, and 39 to the power supply rails.



Touch Panel connector



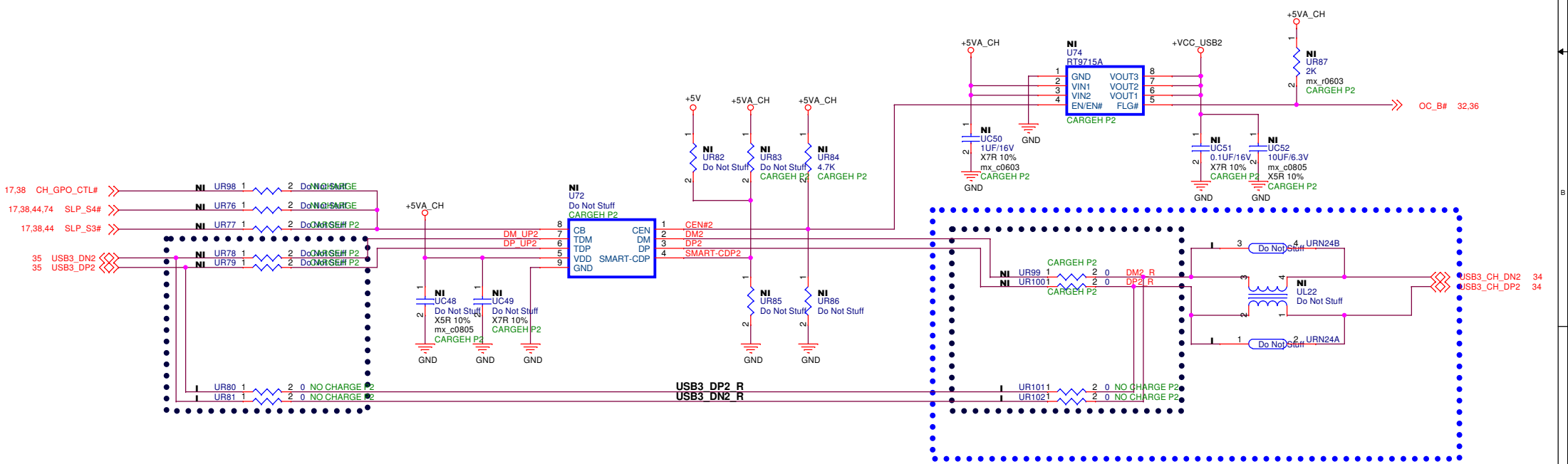
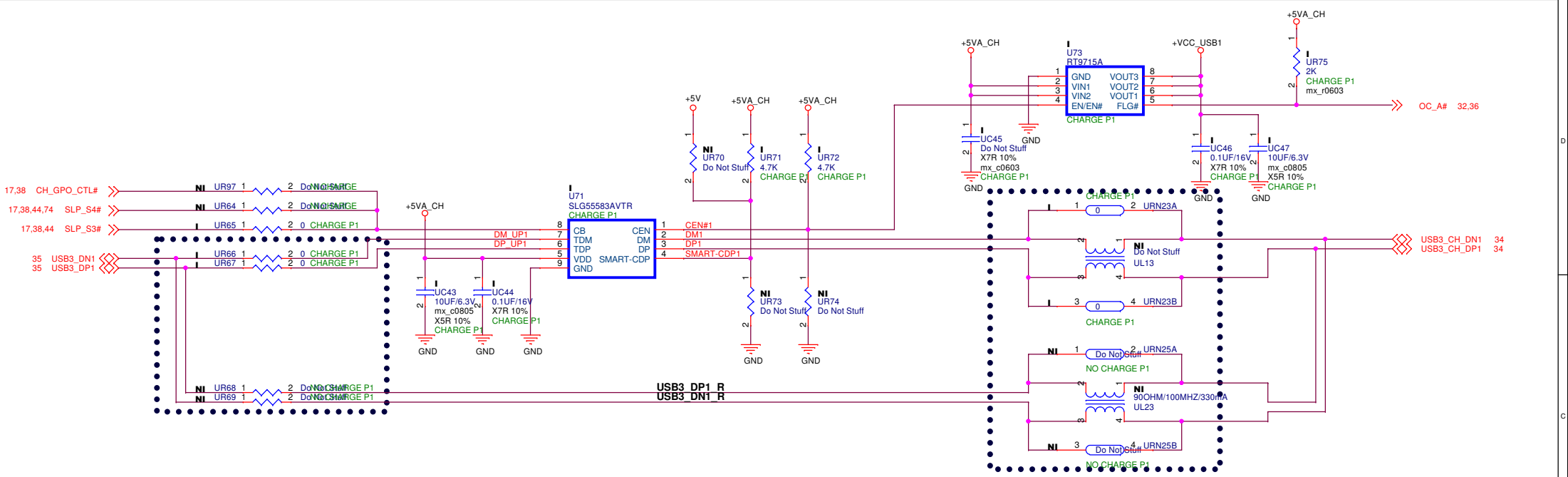
Camera Module connector

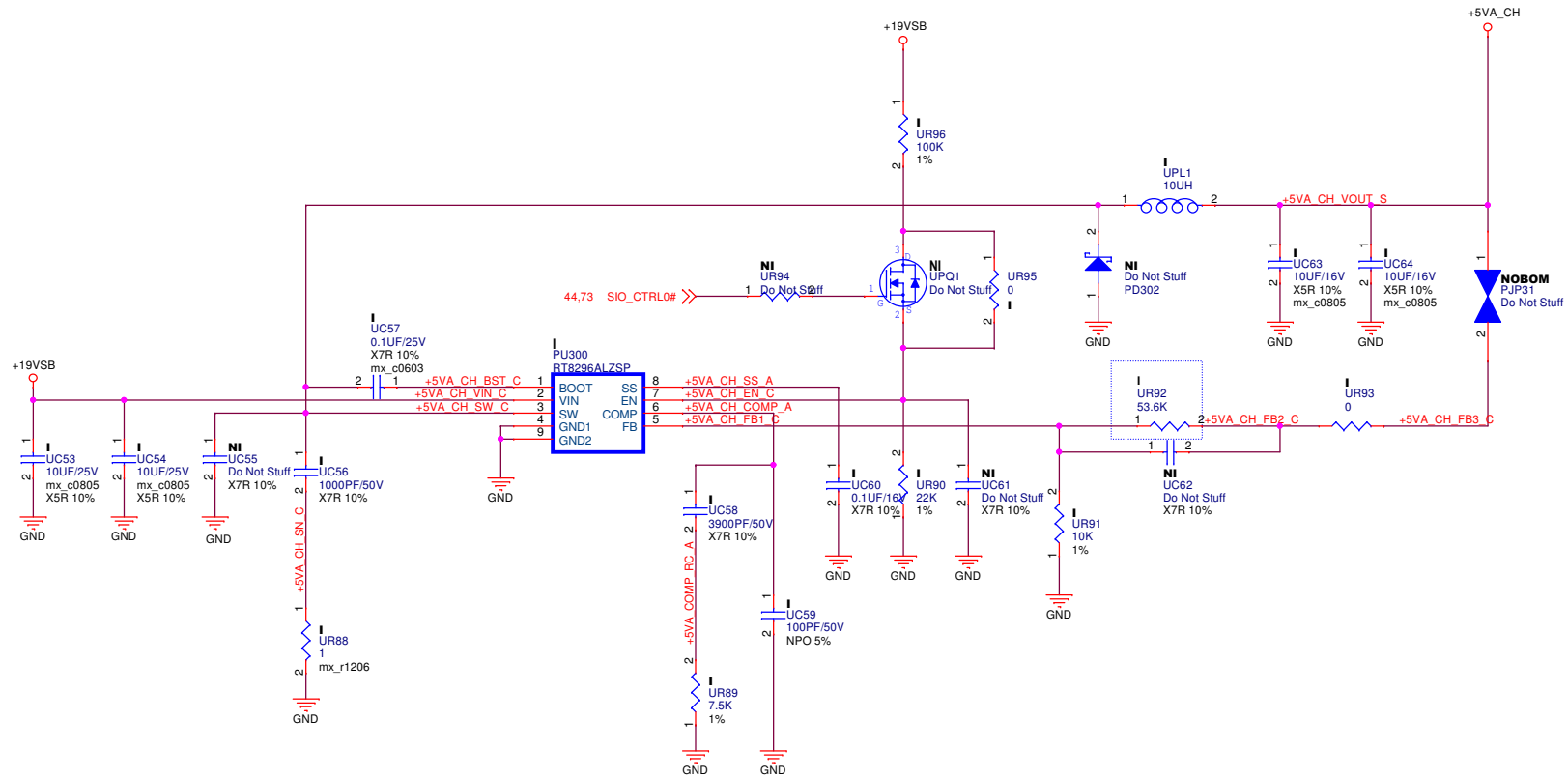


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB HEADER
Pegatron Corp. Engineer: ShunJing_Yang

Size	Project Name	Rev
A3	IPISB-AG	1.06
Date: Tuesday, February 21, 2012 Sheet 37 of 82		

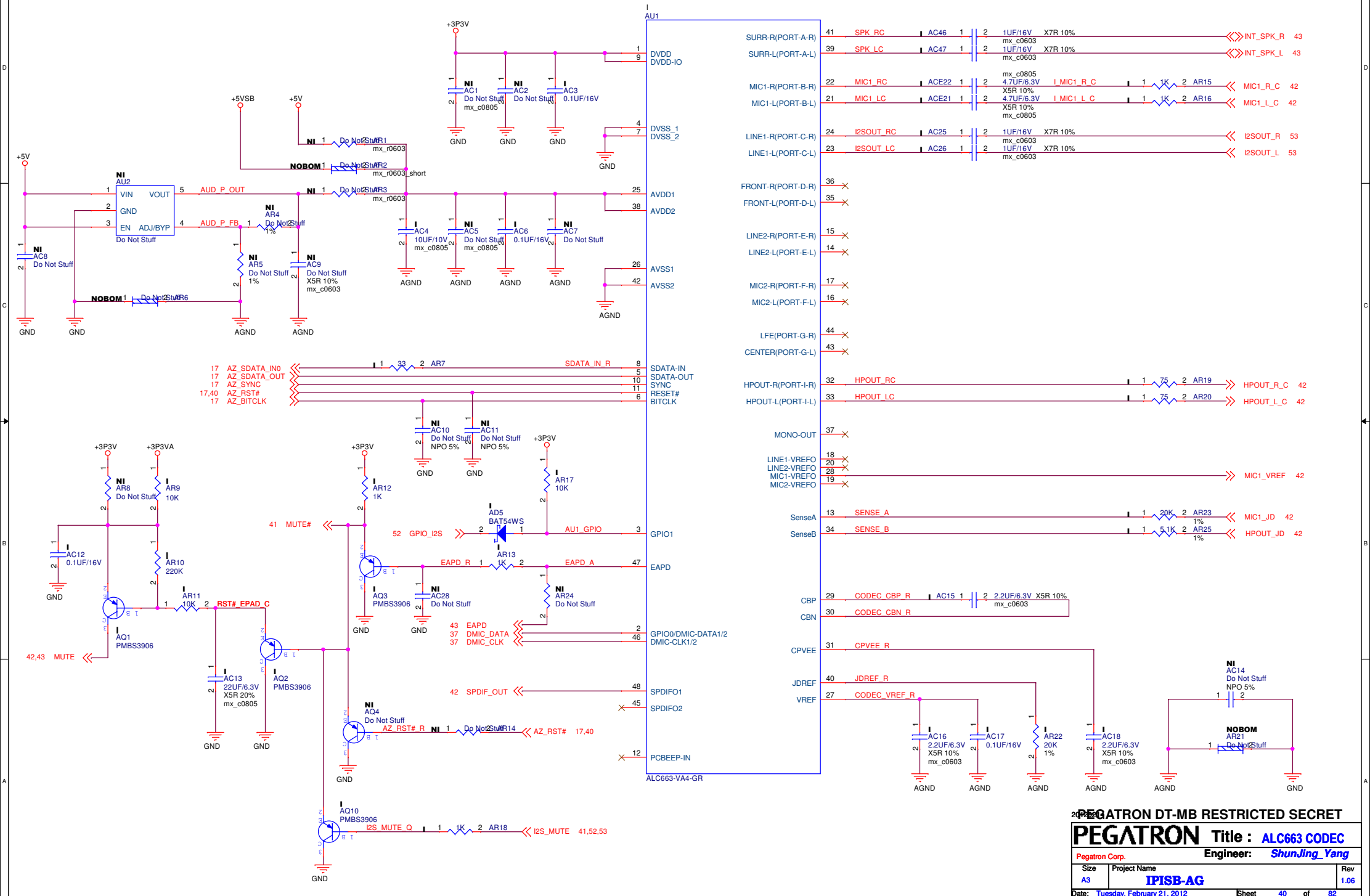


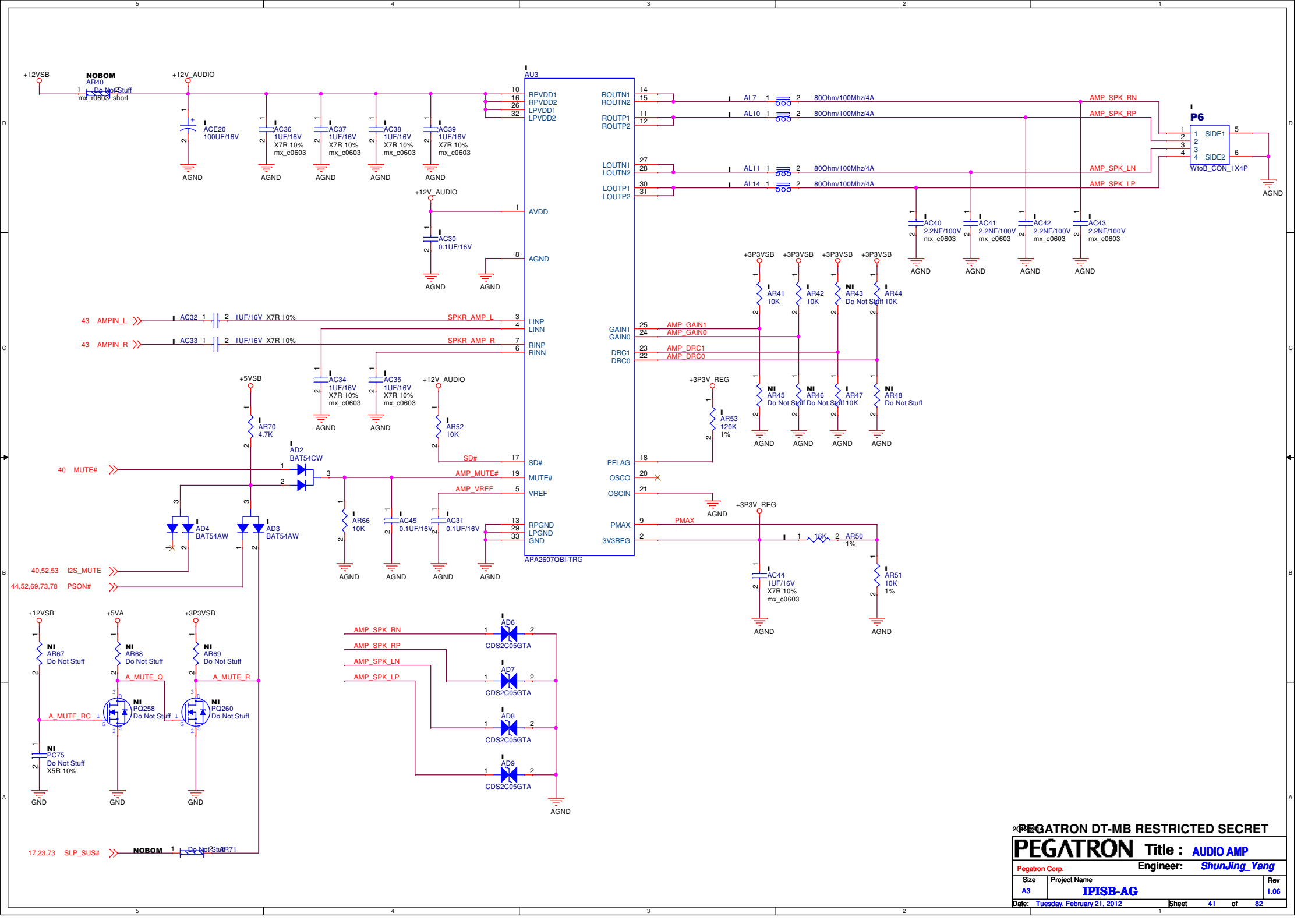


20120214

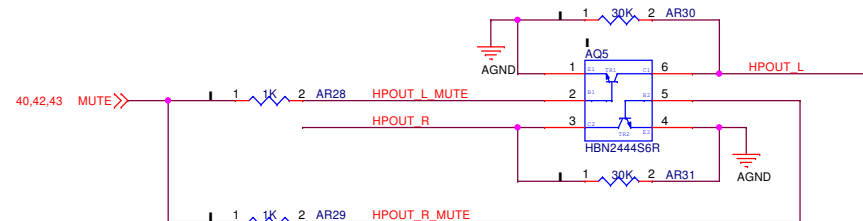
Title			<Title>
Size	Document Number		Rev
A3	<Doc>		1.06
Date:	Tuesday, February 21, 2012	Sheet	39 of 82

INT-SPK

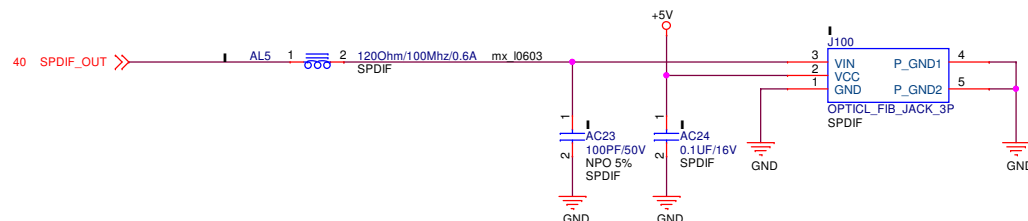
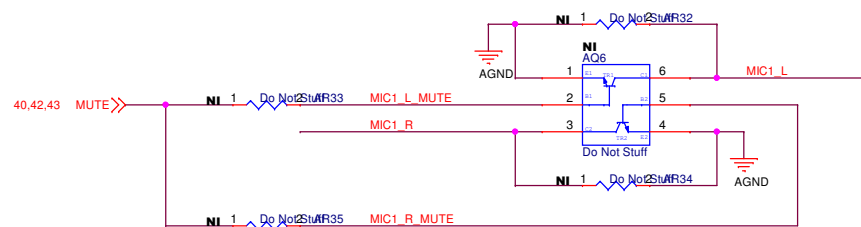


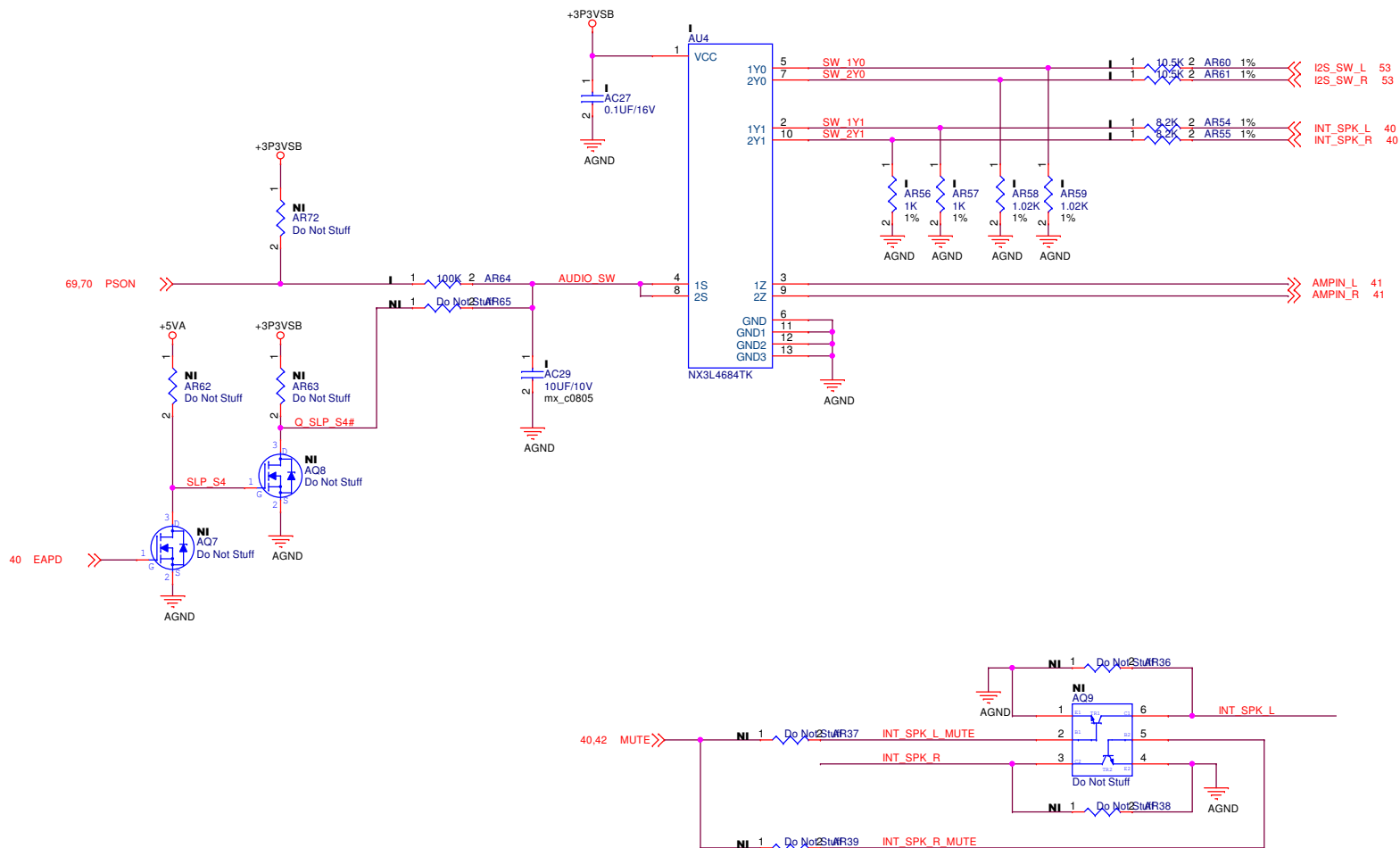


MIC



SPDIF OUT





From I2S DAC

From CODEC

To AMP

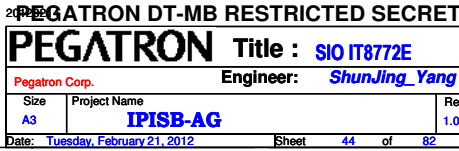
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **AUDIO SW**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: Tuesday, February 21, 2012 Sheet 43 of 82



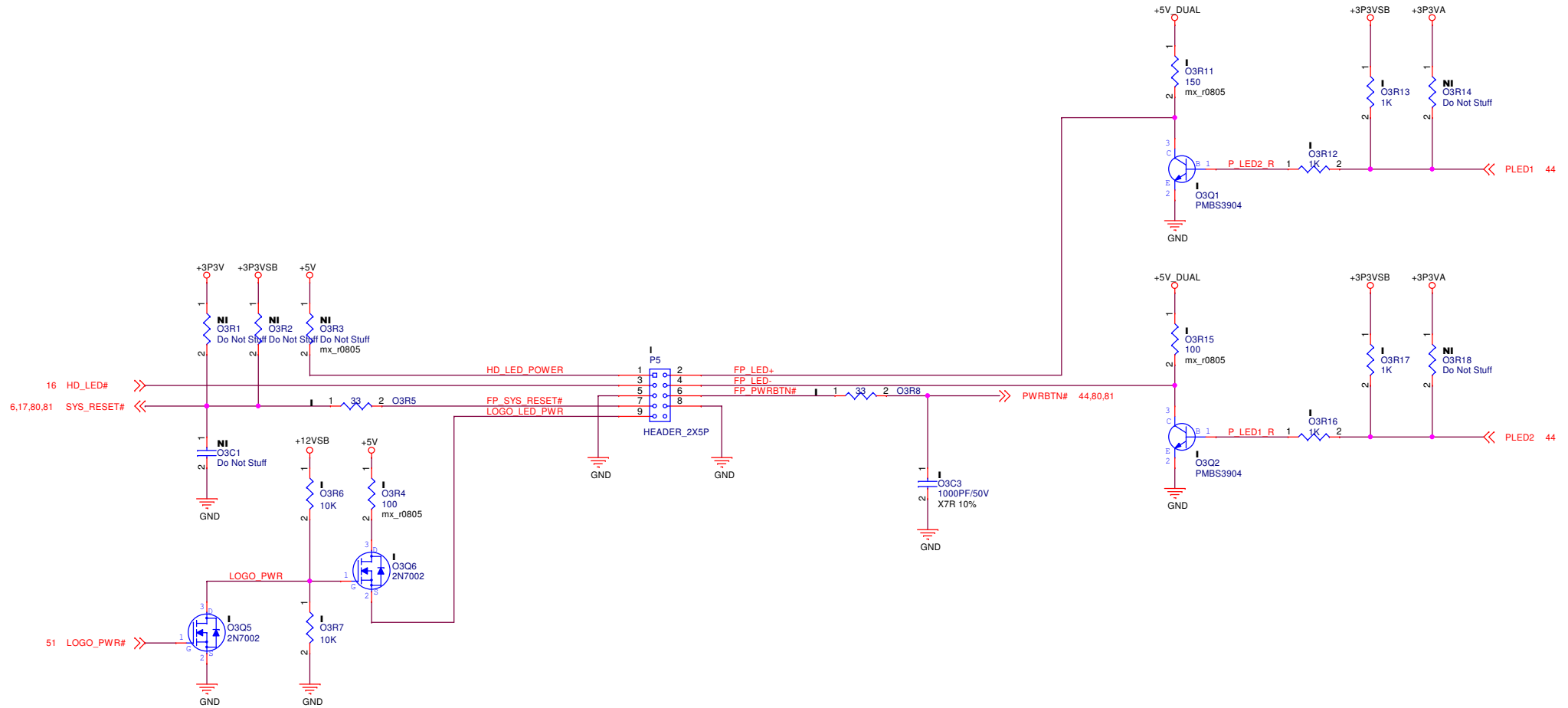
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **FRONT PANEL**

Pegatron Corp. **Engineer:** ShunJing_Yang

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: Tuesday, February 21, 2012 Sheet 45 of 82



CPU FAN CONNECTOR

SYS FAN CONNECTOR

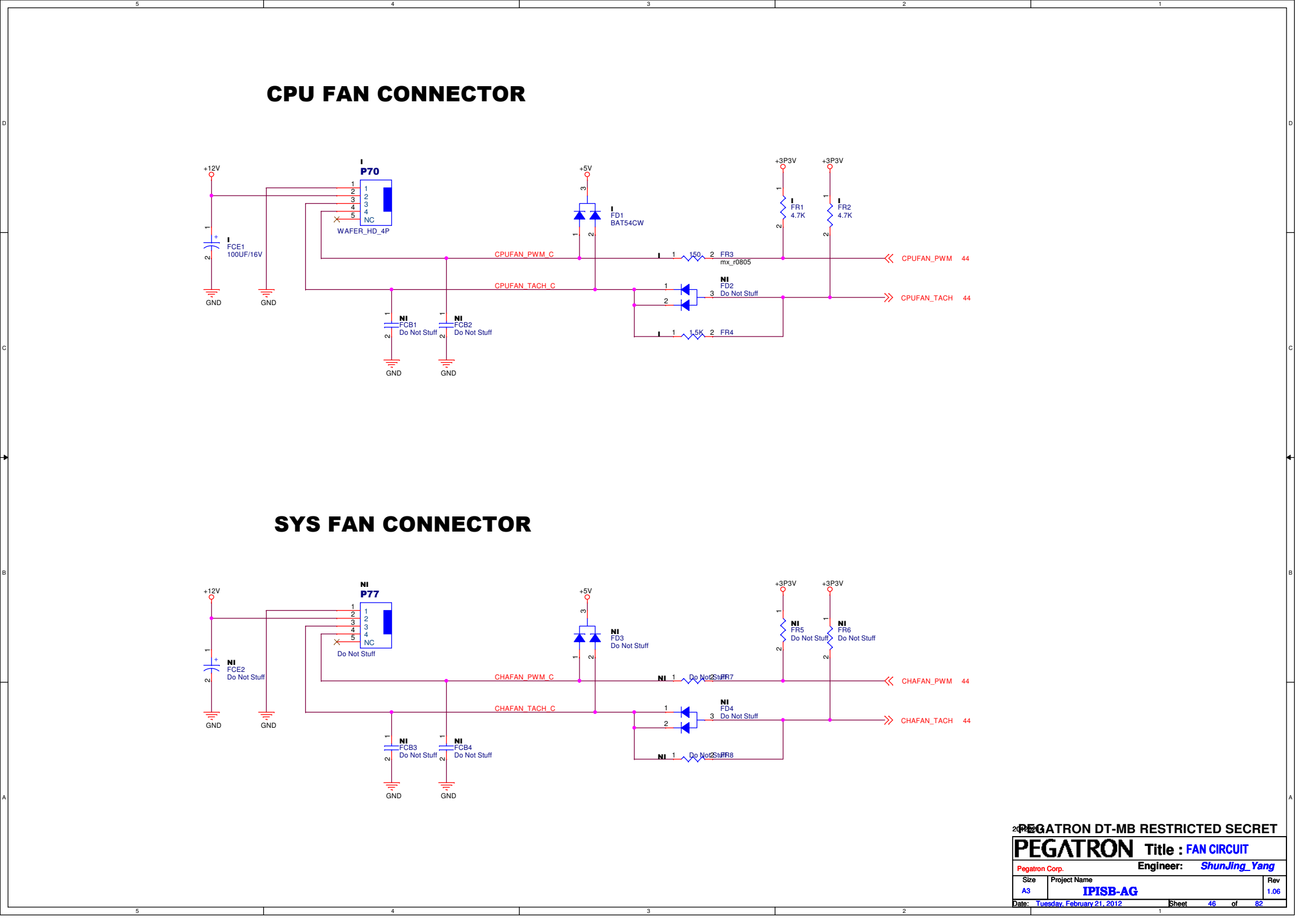
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FAN CIRCUIT

Pegatron Corp. Engineer: ShunJing_Yang

Size	Project Name	Rev
A3	IPISB-AG	1.06

Date: Tuesday, February 21, 2012 Sheet 46 of 82



CPU FAN CONNECTOR

SYS FAN CONNECTOR

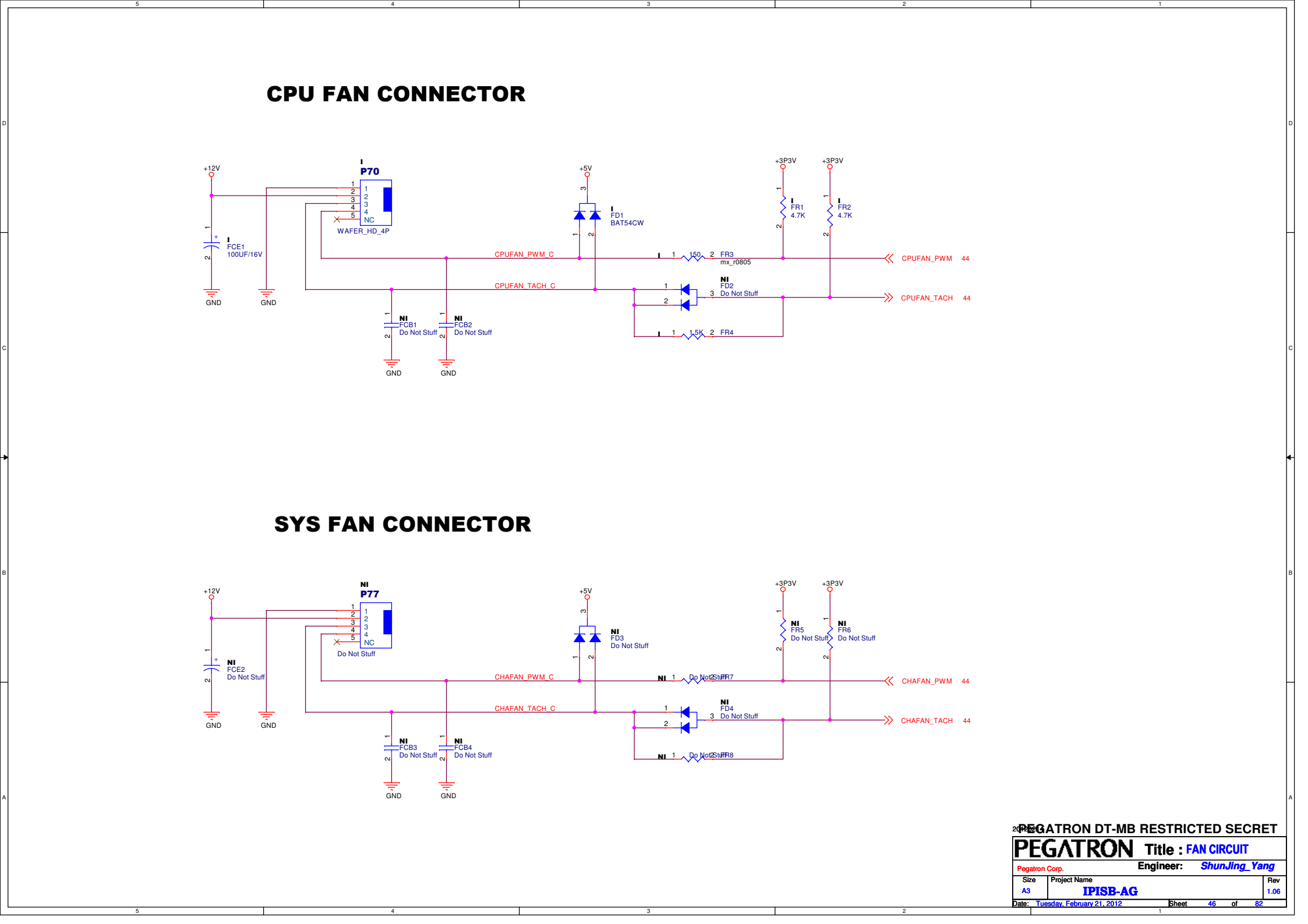
PEGATRON DT-MB RESTRICTED SECRET

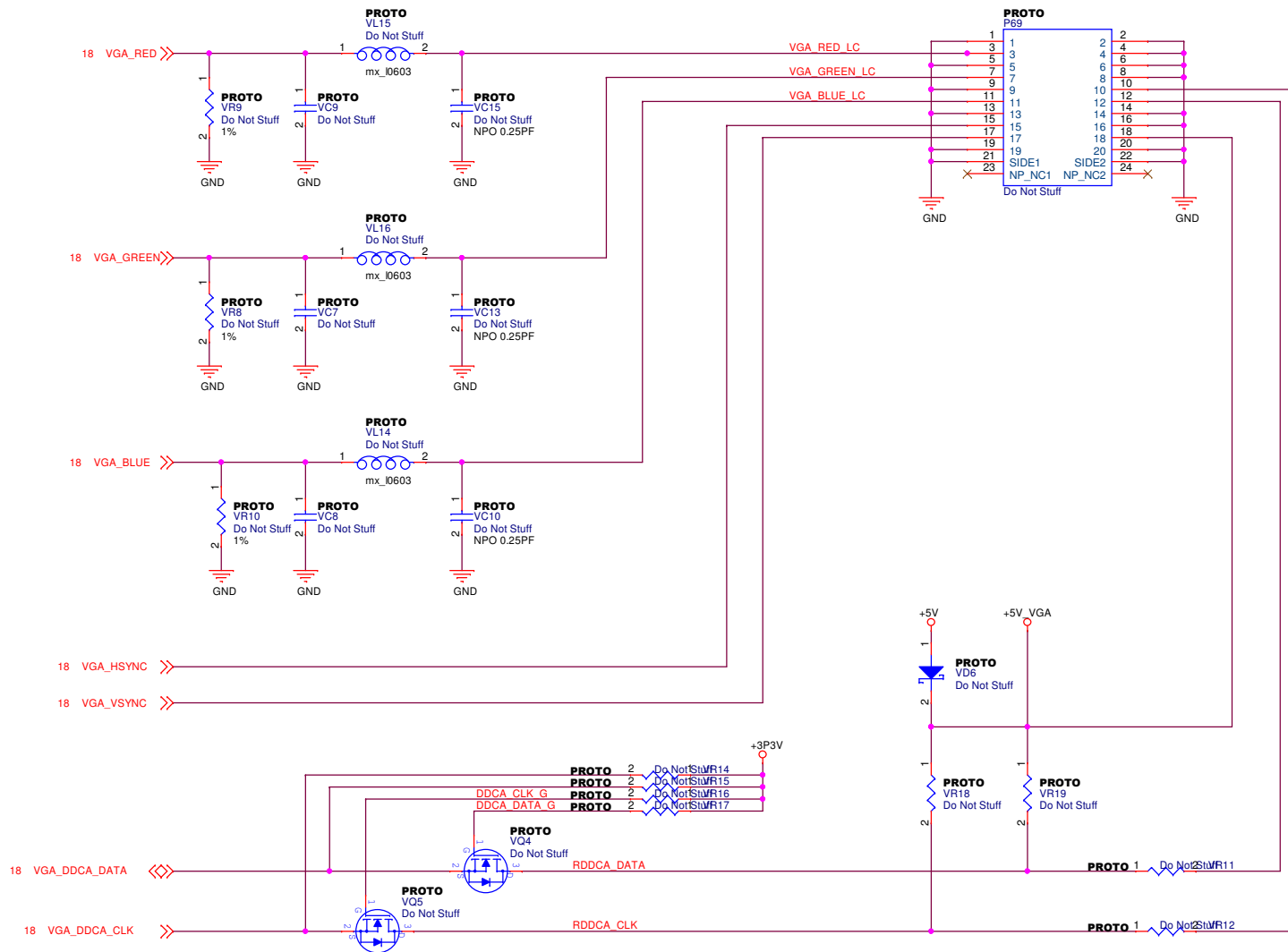
PEGATRON Title : FAN CIRCUIT

Pegatron Corp. Engineer: ShunJing_Yang

Size	Project Name	Rev
A3	IPISB-AG	1.06

Date: Tuesday, February 21, 2012 Sheet 46 of 82





PEGATRON DT-MB RESTRICTED SECRET

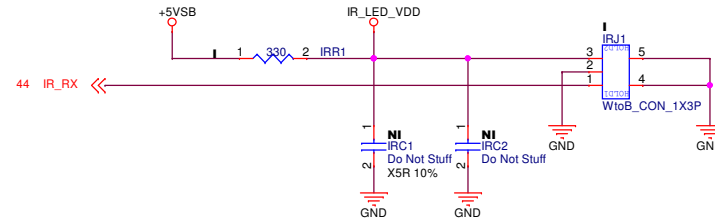
PEGATRON Title : **VGA PORT**

Pegatron Corp. Engineer: **ShunJing_Yang**

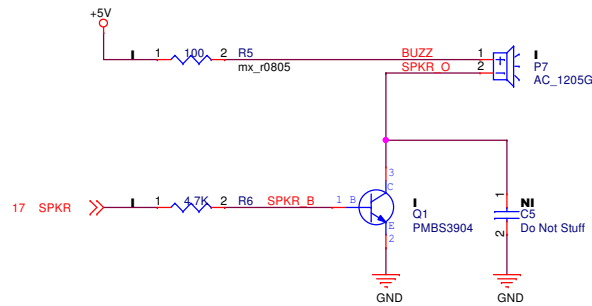
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **47** of **82**

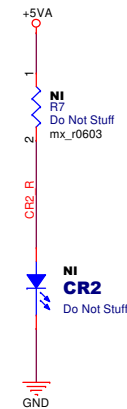
IR LED



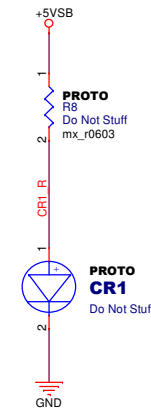
SPEAKER



+5VA : BLUE



+5VSB : GREEN



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **IR / SPKR**

Pegatron Corp. Engineer: **ShunJing_Yang**

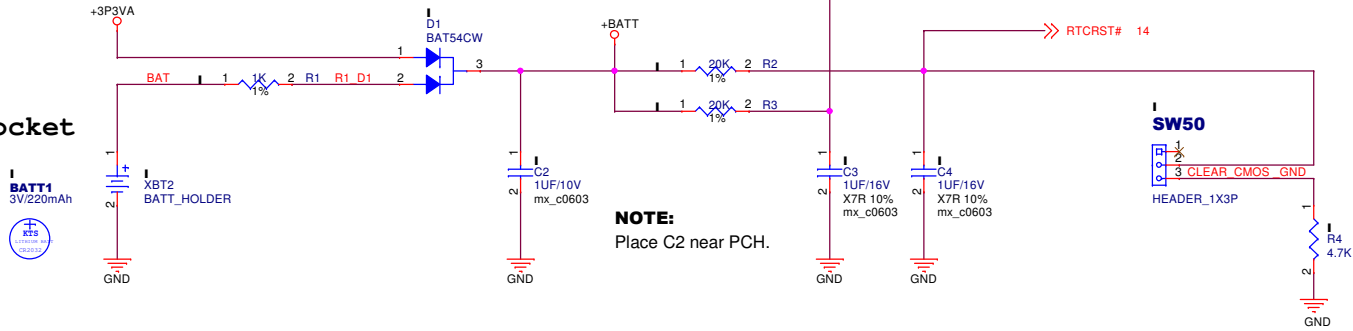
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **48** of **82**

External RTC Circuitry

CLEAR CMOS

Battery Socket



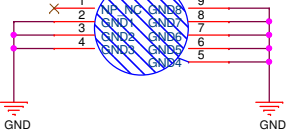
NOTE:
Place C2 near PCH.



NOBOM

H1

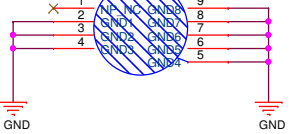
Do Not Stuff



NOBOM

H4

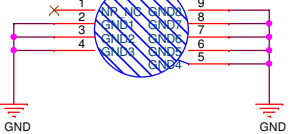
Do Not Stuff



NOBOM

H2

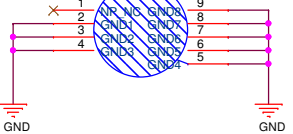
Do Not Stuff



NOBOM

H5

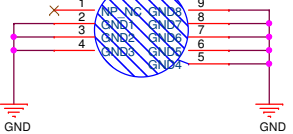
Do Not Stuff



NOBOM

H3

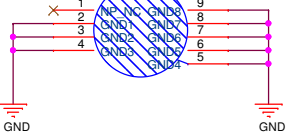
Do Not Stuff



NOBOM

H6

Do Not Stuff



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RTC/COMS/SCREW

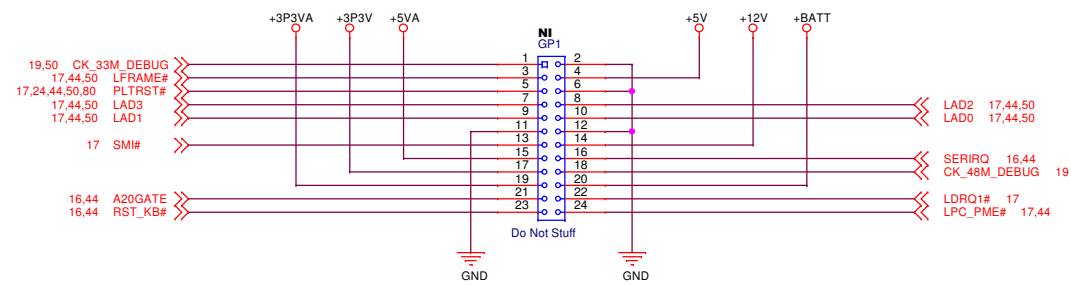
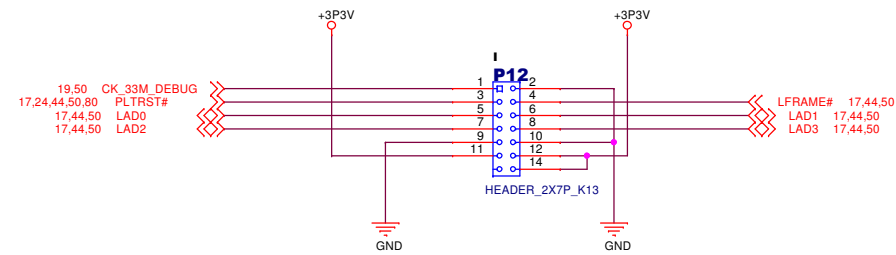
Pegatron Corp. Engineer: ShunJing_Yang

Size Project Name Rev

A3 IPISB-AG 1.06

Date: Tuesday, February 21, 2012 Sheet 49 of 82

LPC DEBUG



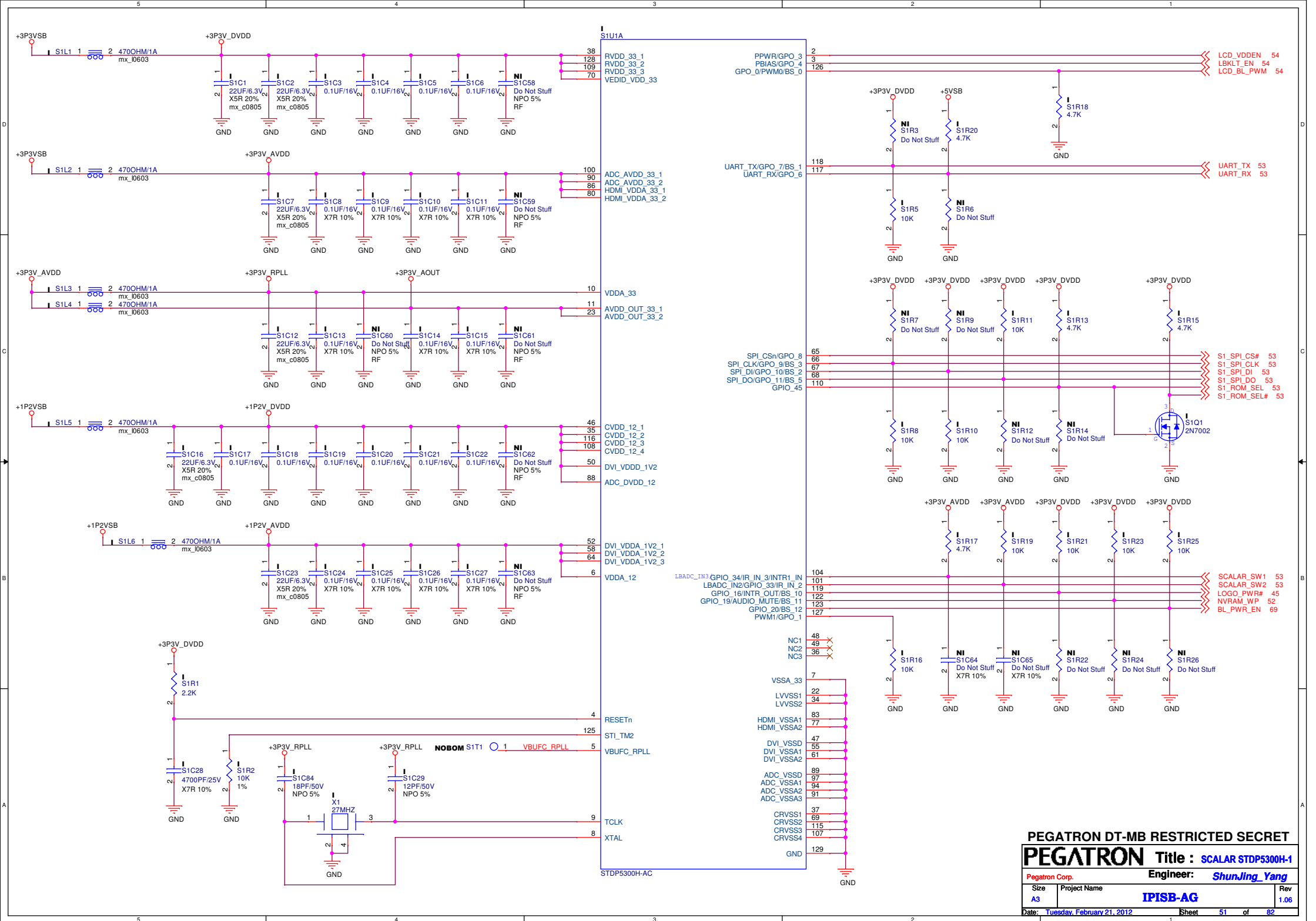
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **DEBUG HEADER**

Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **50** of **82**



PEGATRON DT-MB RESTRICTED SECRET

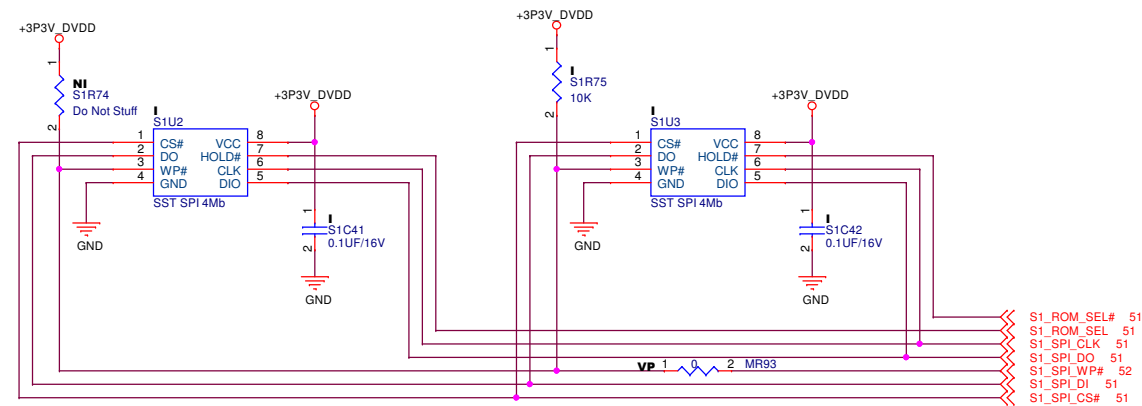
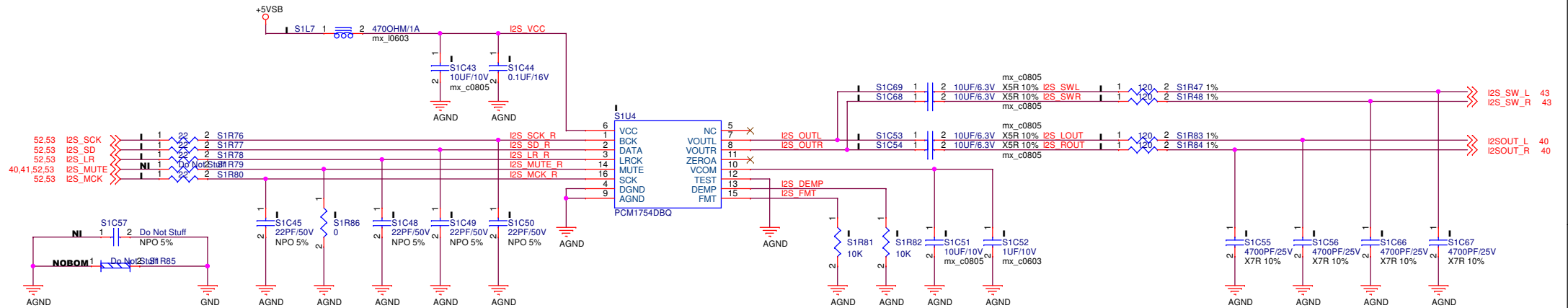
PEGATRON Title : SCALAR STDP5300H-1

Pegatron Corp. Engineer: ShunJing_Yang

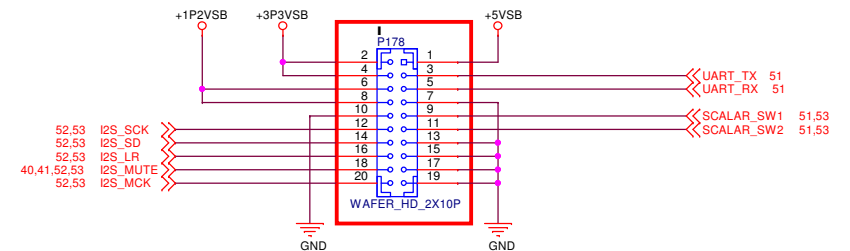
Size A3 Project Name IPISB-AG Rev 1.06

Date: Tuesday, February 21, 2012 Sheet 51 of 82



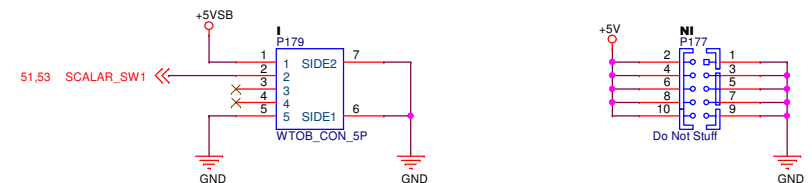
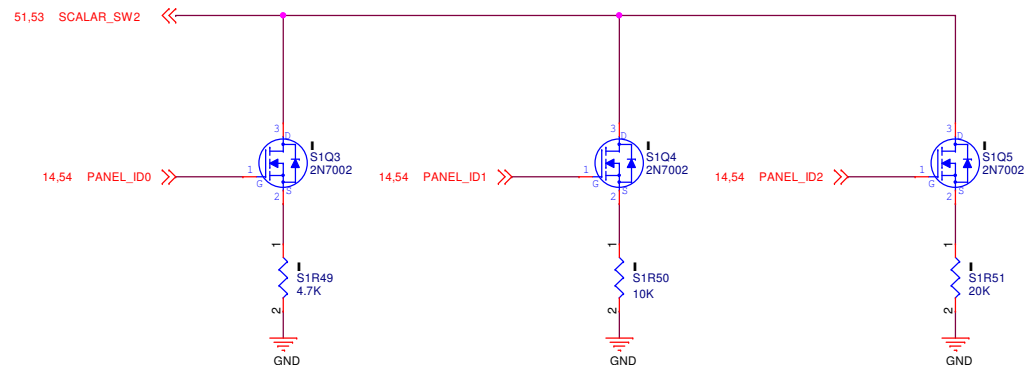


3D Scaler



KEYPAD

3D PANEL



PEGATRON DT-MB RESTRICTED SECRET

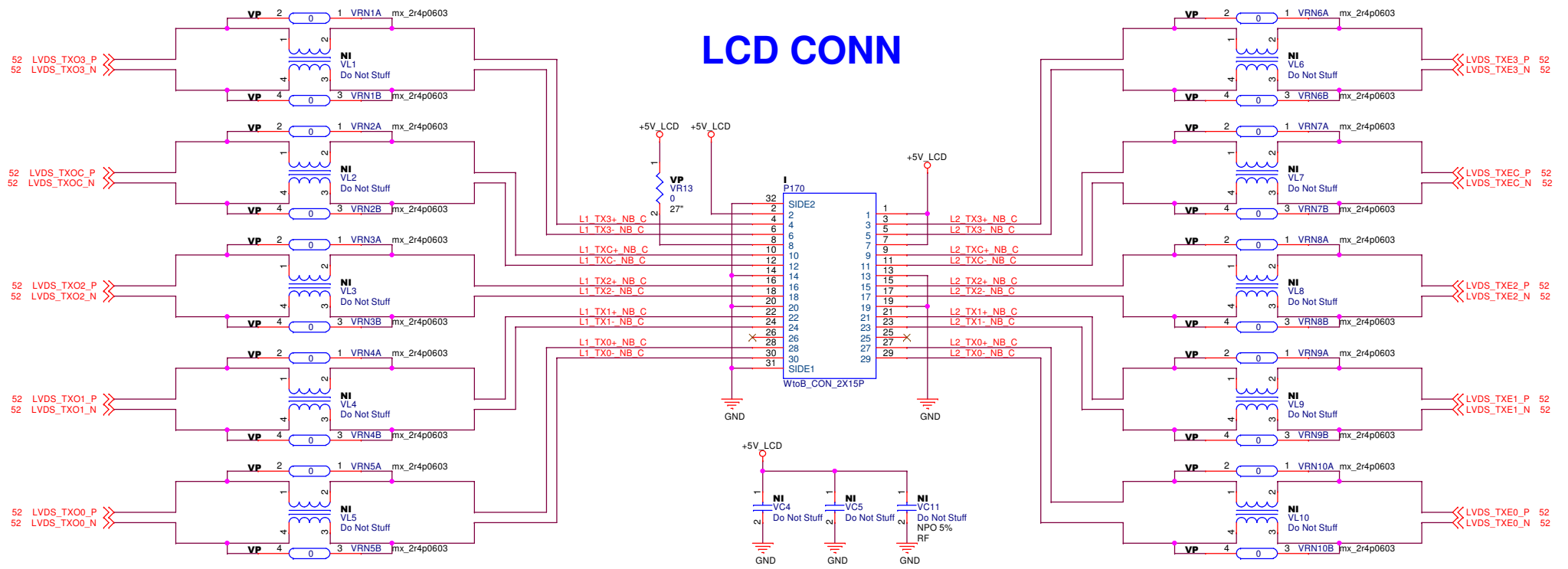
PEGATRON Title : **I2S AUDIO DAC**

Pegatron Corp. Engineer: **ShunJing_Yang**

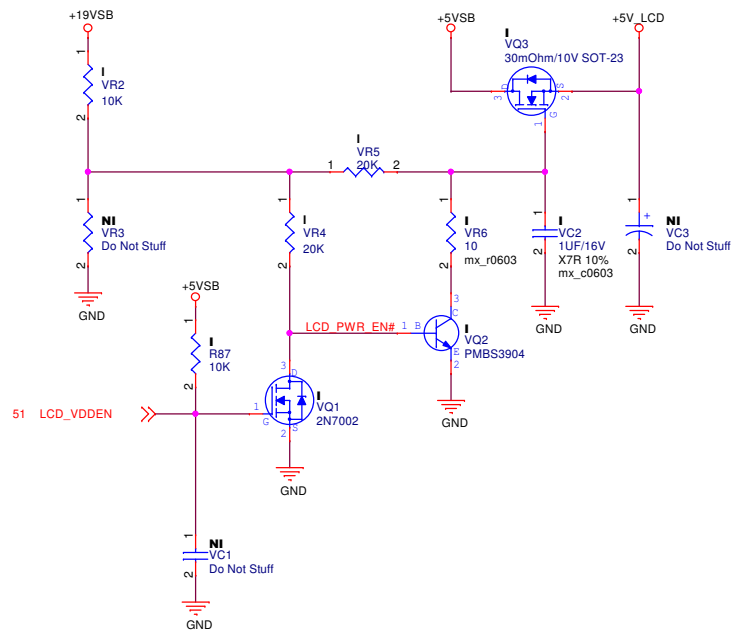
Size A3 Project Name **IPISB-AG** Rev 1.06

Date: Tuesday, February 21, 2012 Sheet 53 of 82

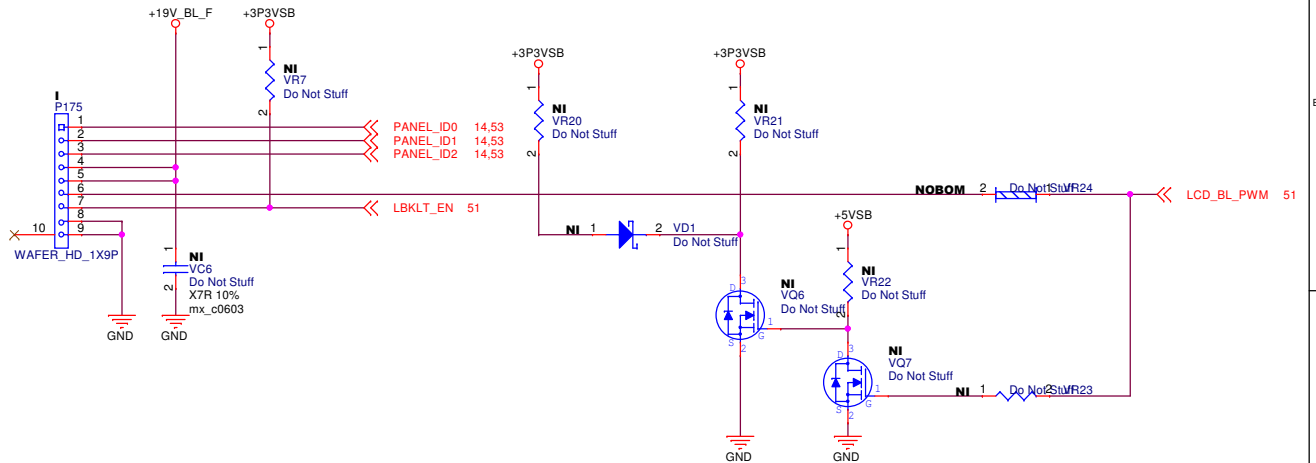
LCD CONN



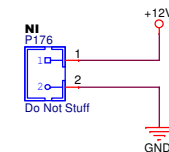
LCD ON/OFF

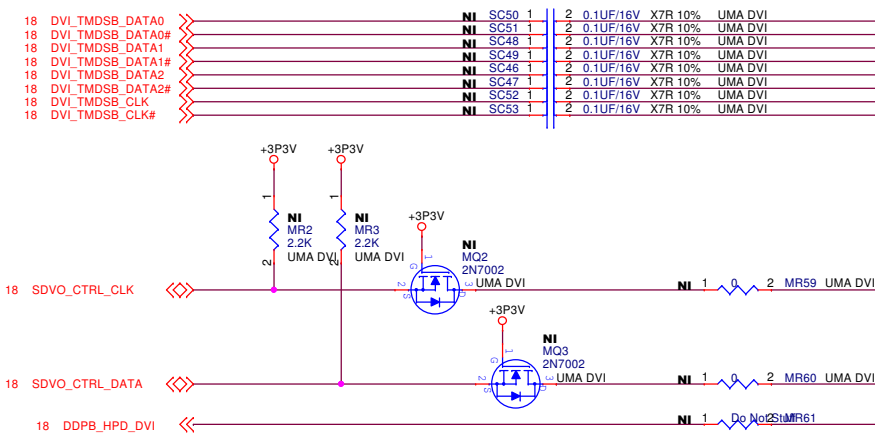
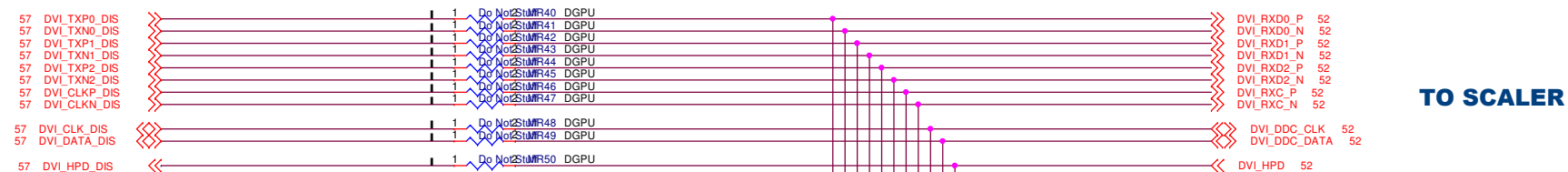


CONVERTER CONN.



TOUCH

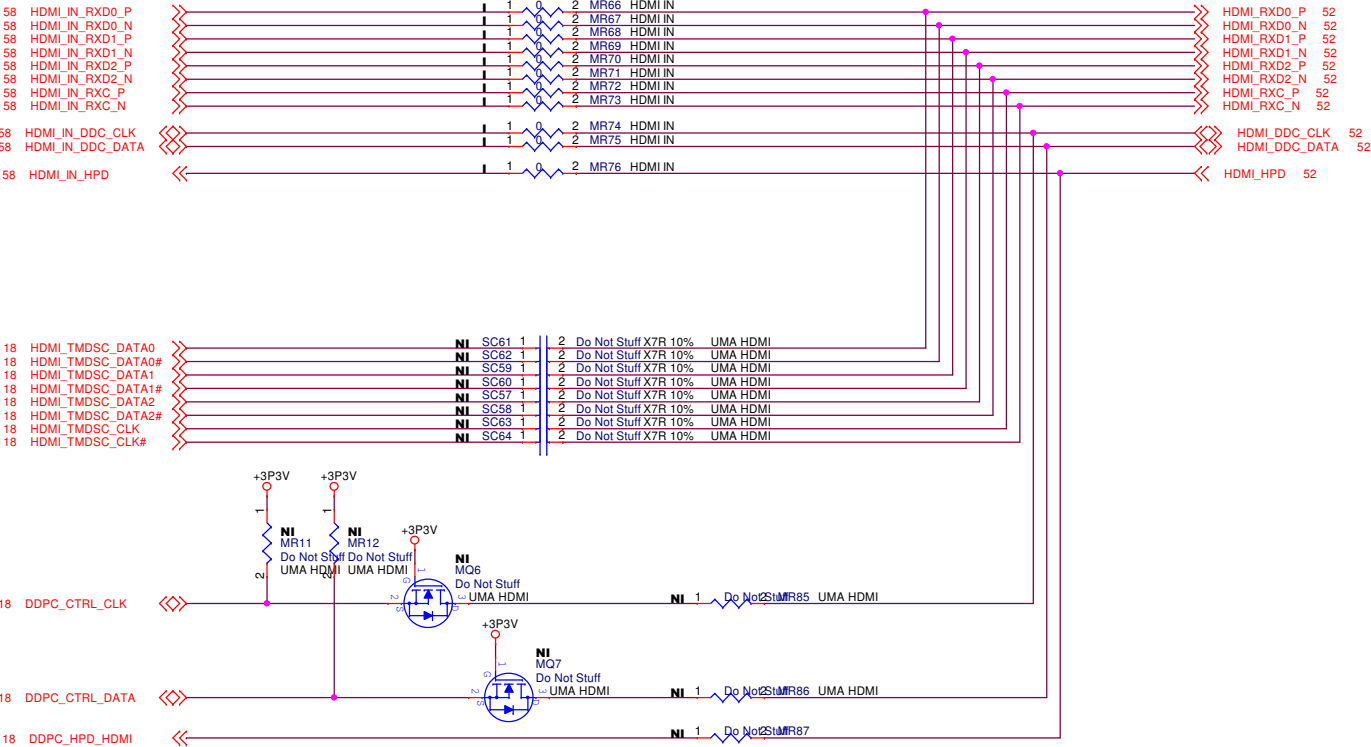


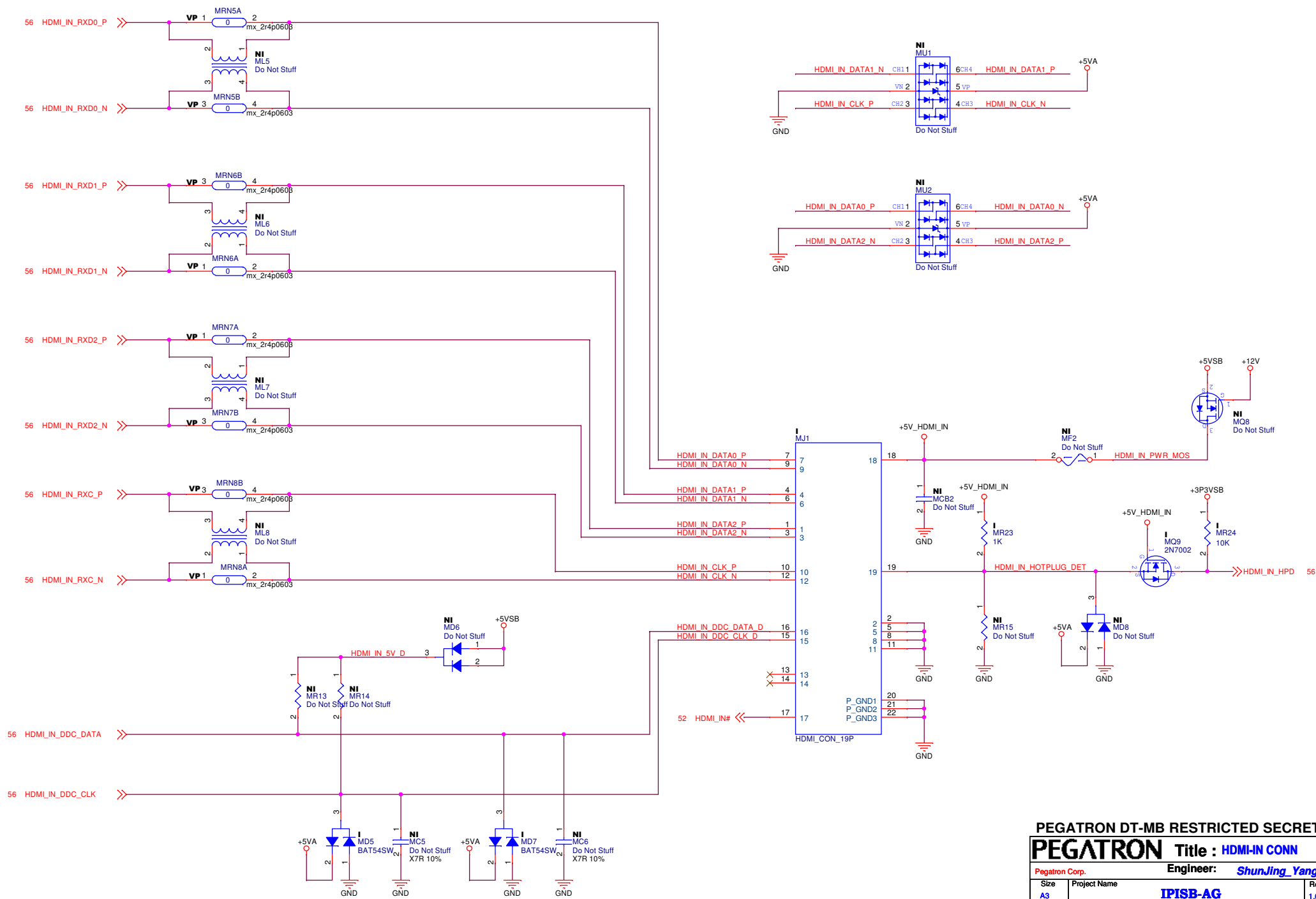


FROM CONN

TO SCALER

FROM PCH





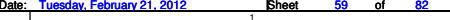
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : HDMI-IN CONN

Pegatron Corp. Engineer: ShunJing_Yang

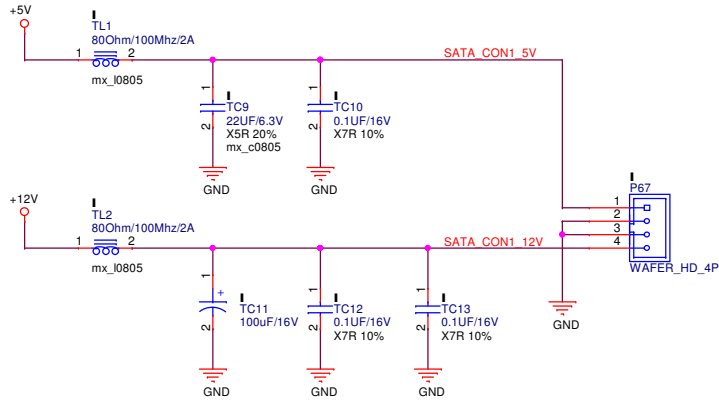
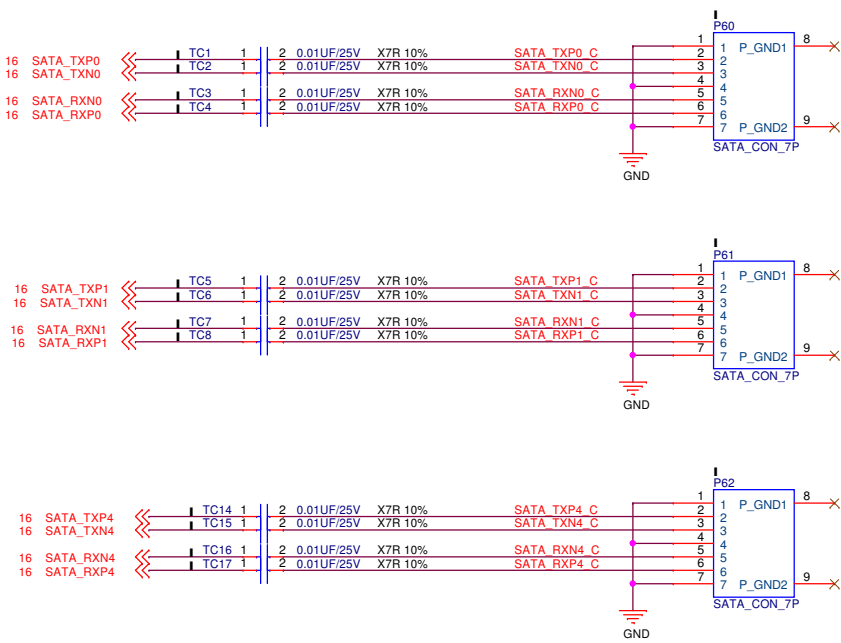
Size A3	Project Name IPISB-AG	Rev 1.06
------------	--------------------------	-------------

Date: Tuesday, February 21, 2012 Sheet 56 of 82





SATA CONNECTOR



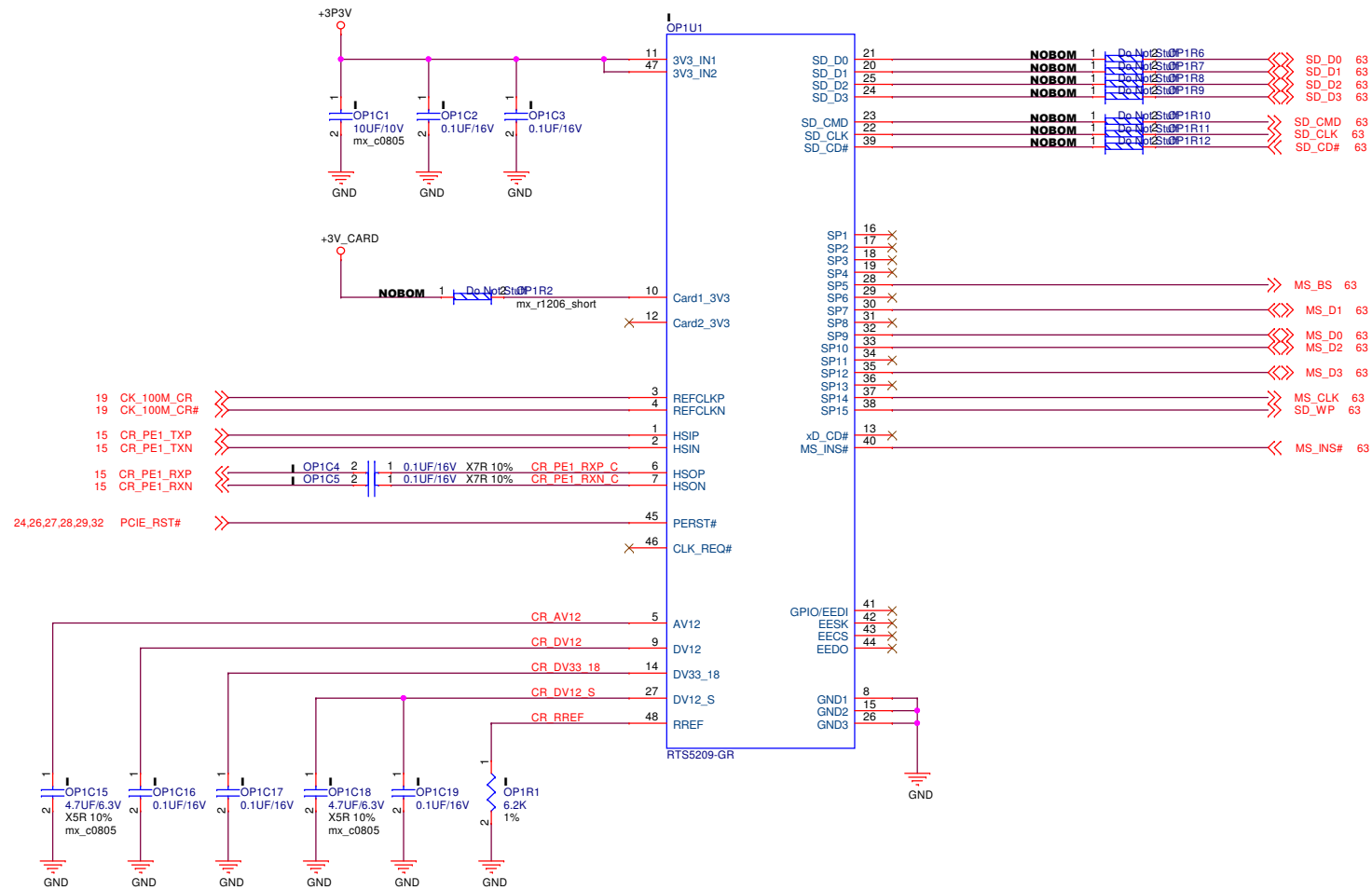
PEGATRON DT-MB RESTRICTED SECRET

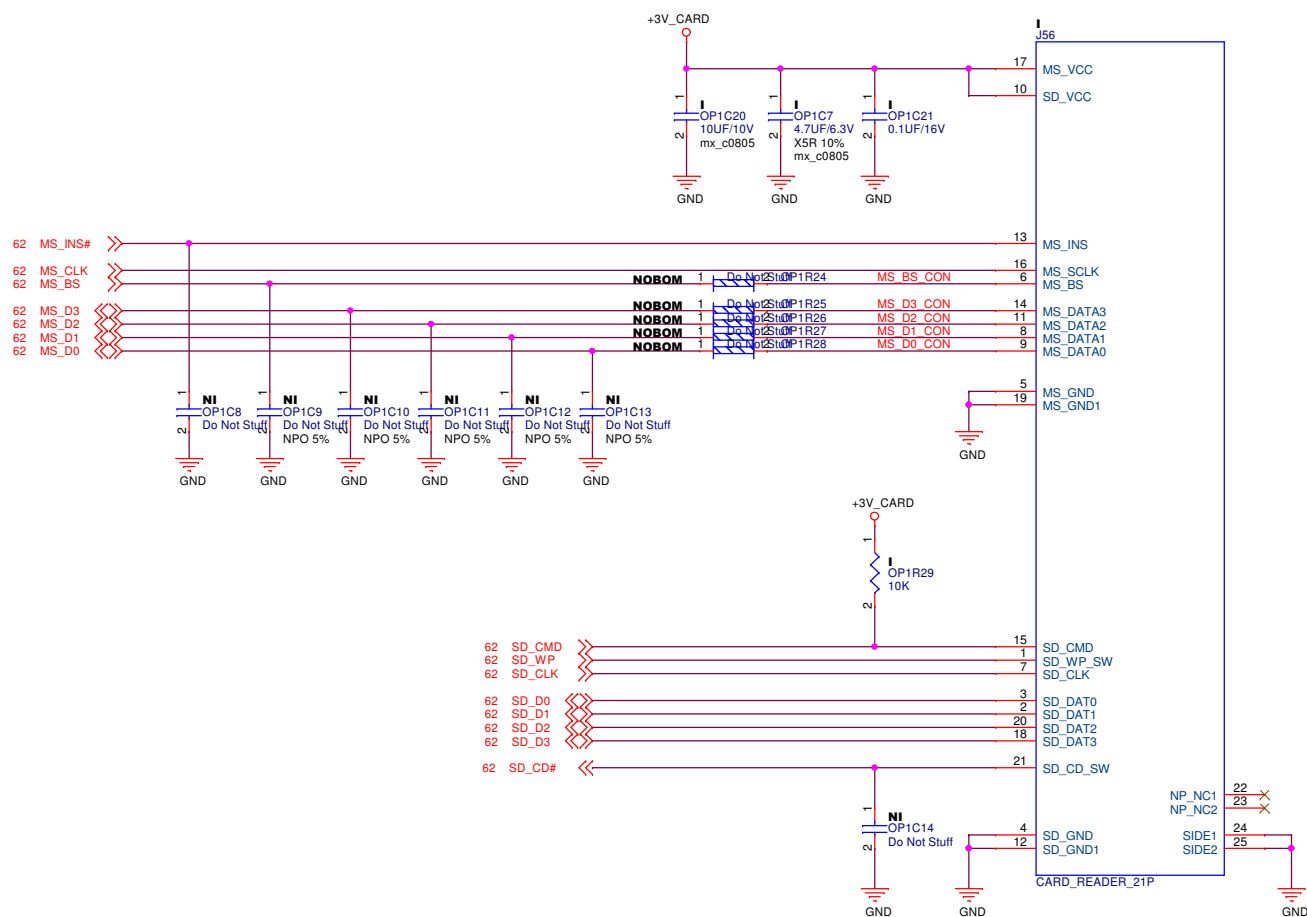
PEGATRON Title : **SATA CONNECTOR**

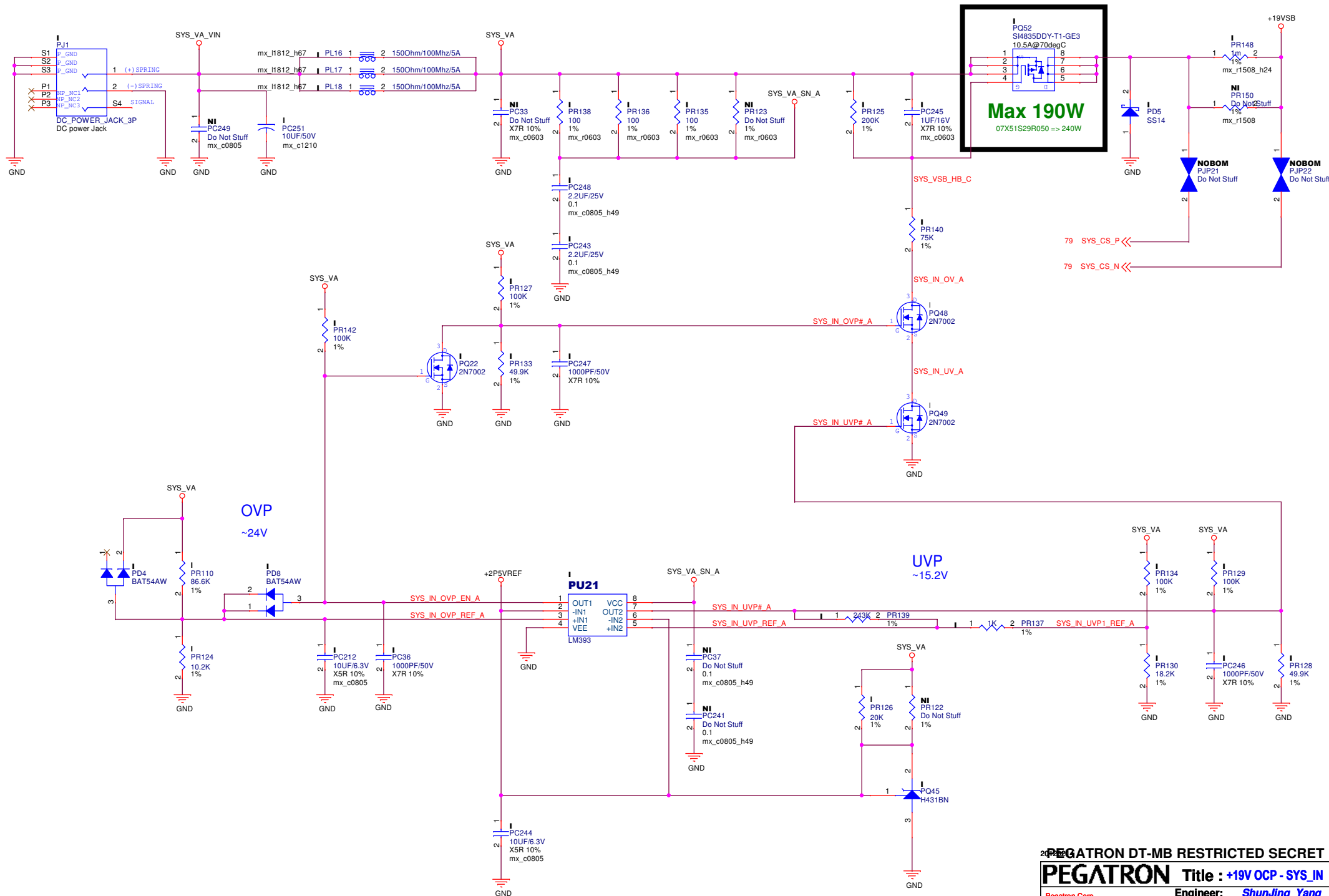
Pegatron Corp. Engineer: **ShunJing_Yang**

Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: **Tuesday, February 21, 2012** Sheet **61** of **82**







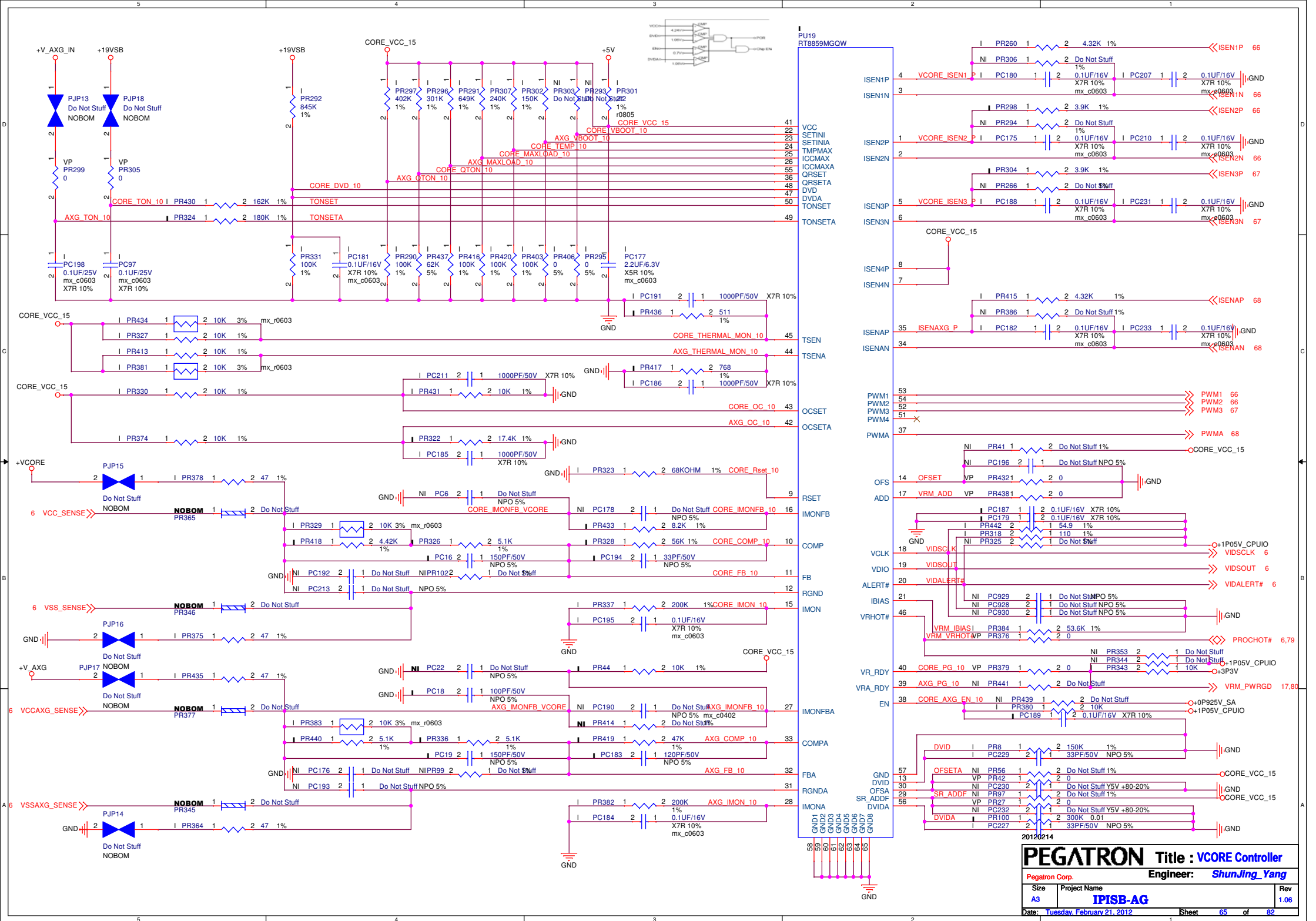
PEGATRON DT-MB RESTRICTED SECRET

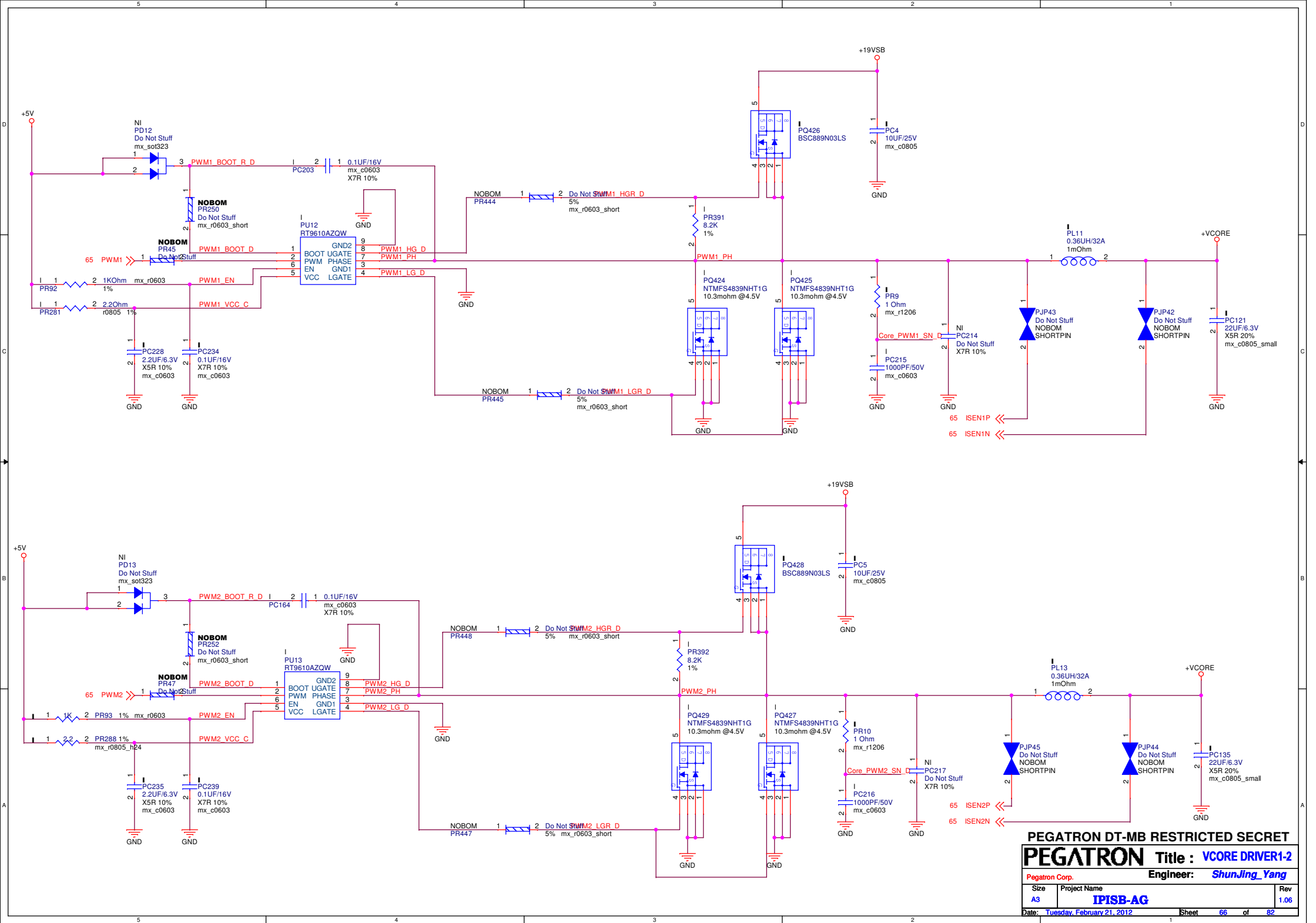
PEGATRON Title : +19V OCP - SYS_IN

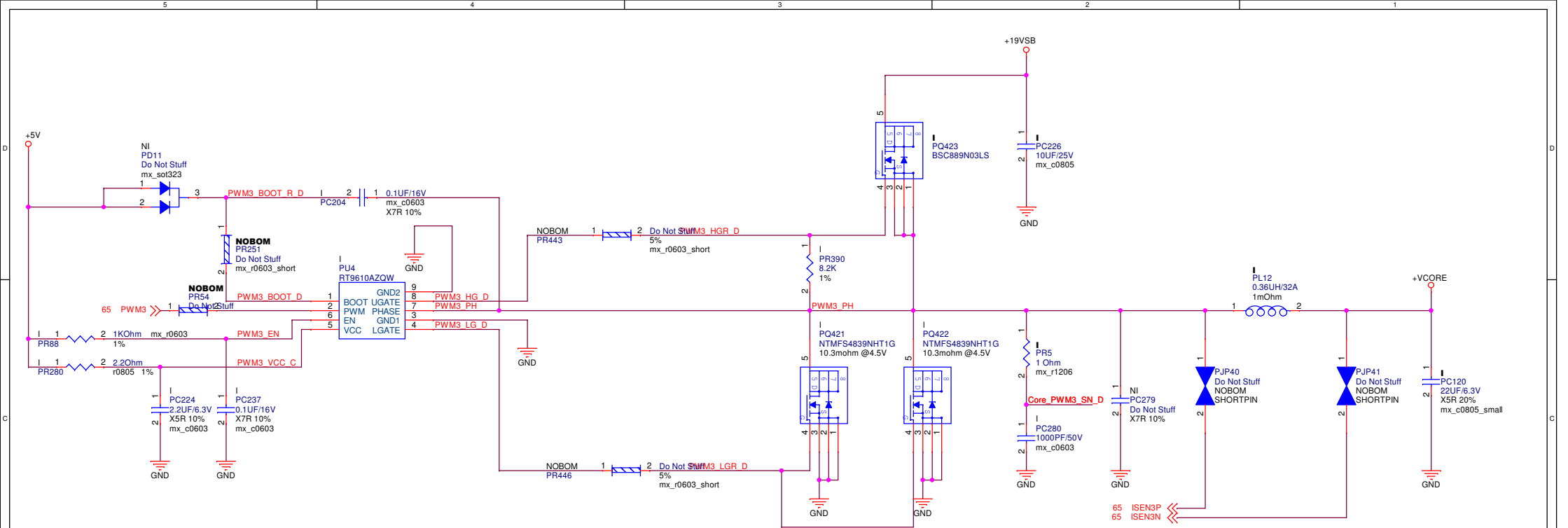
Pegatron Corp. Engineer: ShunJing_Yang

Size	Project Name	Rev
A3	IPISB-AG	1.06

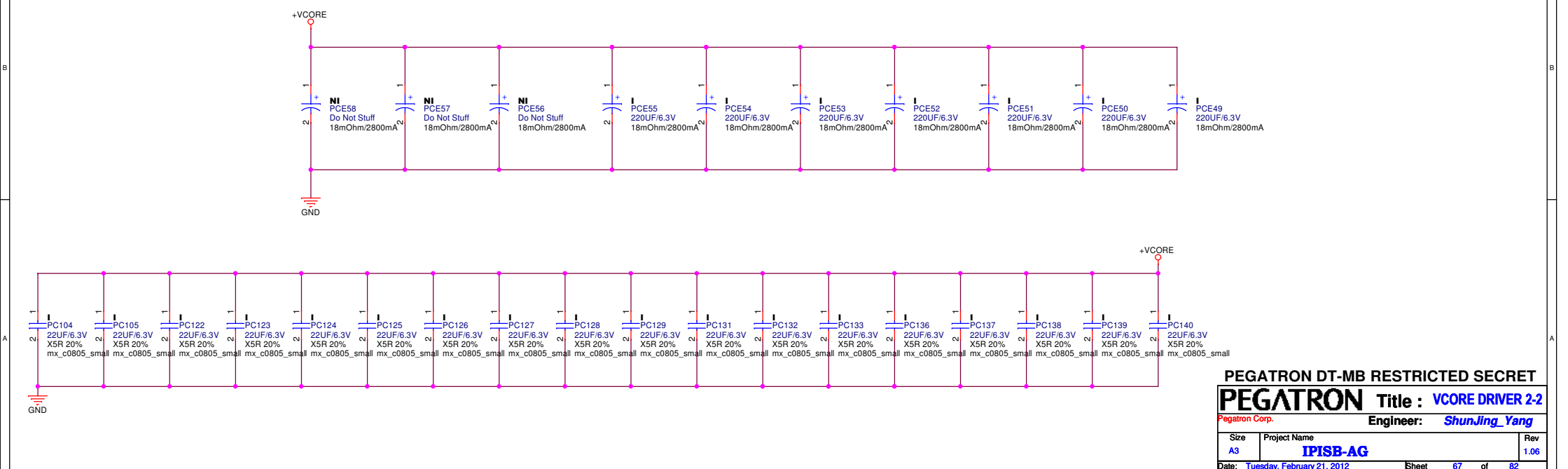
Date: Tuesday, February 21, 2012 Sheet 64 of 82







Output CAP



PEGATRON DT-MB RESTRICTED SECRET

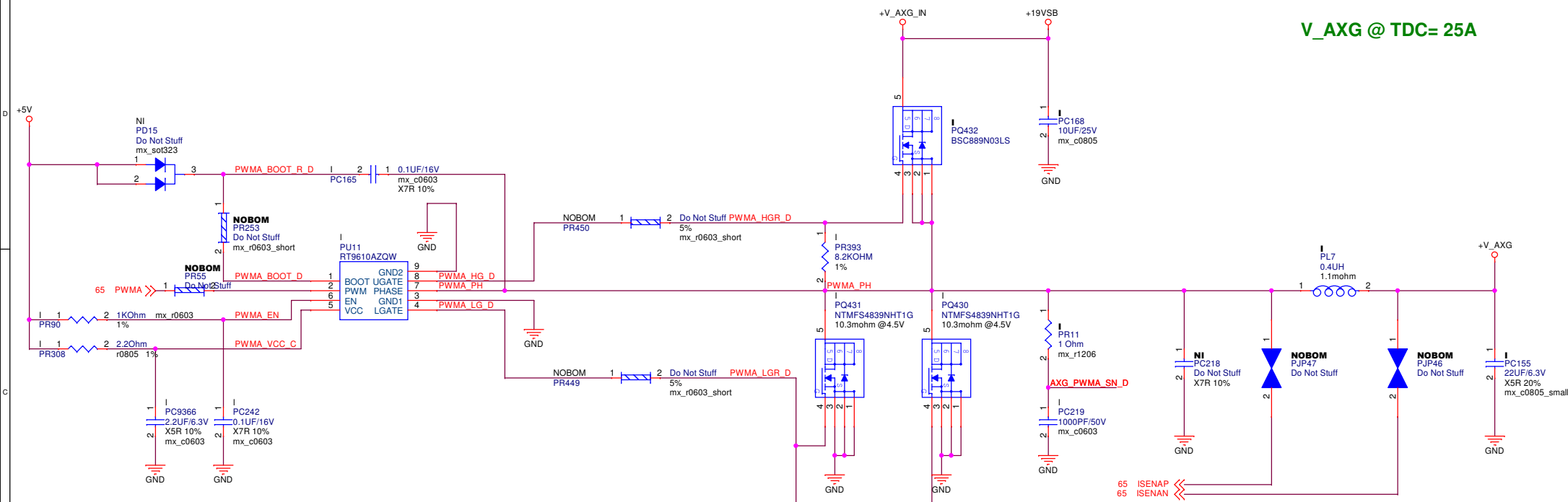
PEGATRON Title : **Vcore DRIVER 2-2**

Pegatron Corp. Engineer: **ShunJing_Yang**

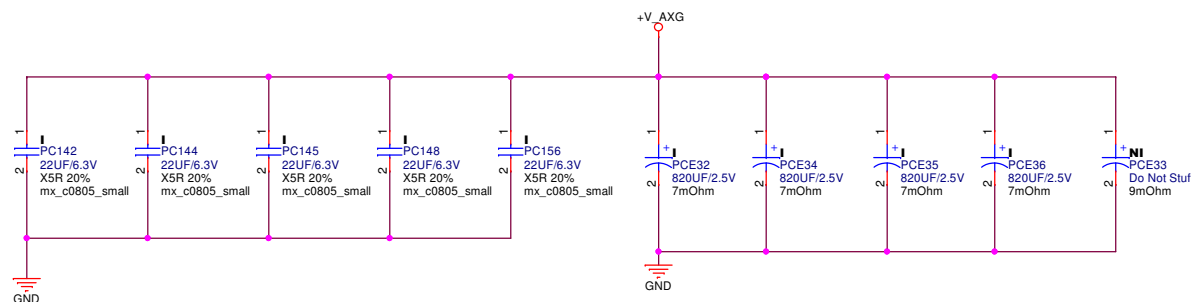
Size A3 Project Name **IPISB-AG** Rev 1.06

Date: Tuesday, February 21, 2012 Sheet 67 of 82

V_AXG @ TDC= 25A



Output CAP



PEGATRON DT-MB RESTRICTED SECRET

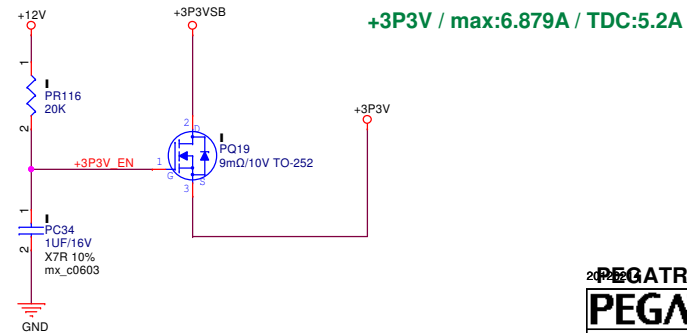
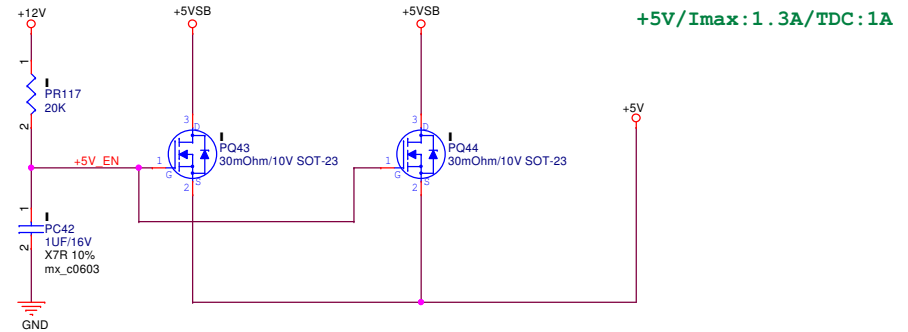
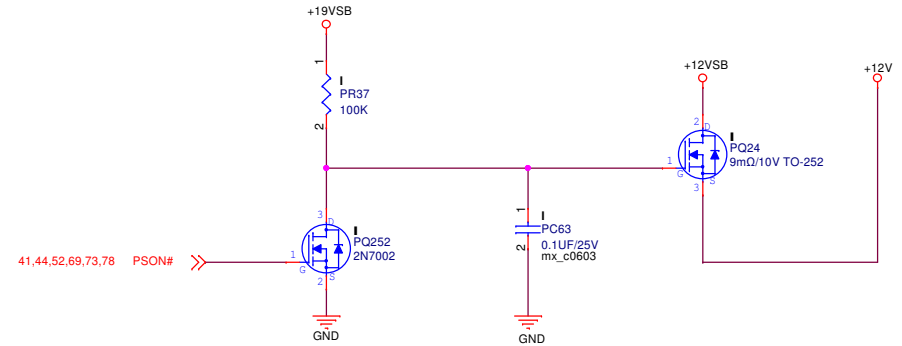
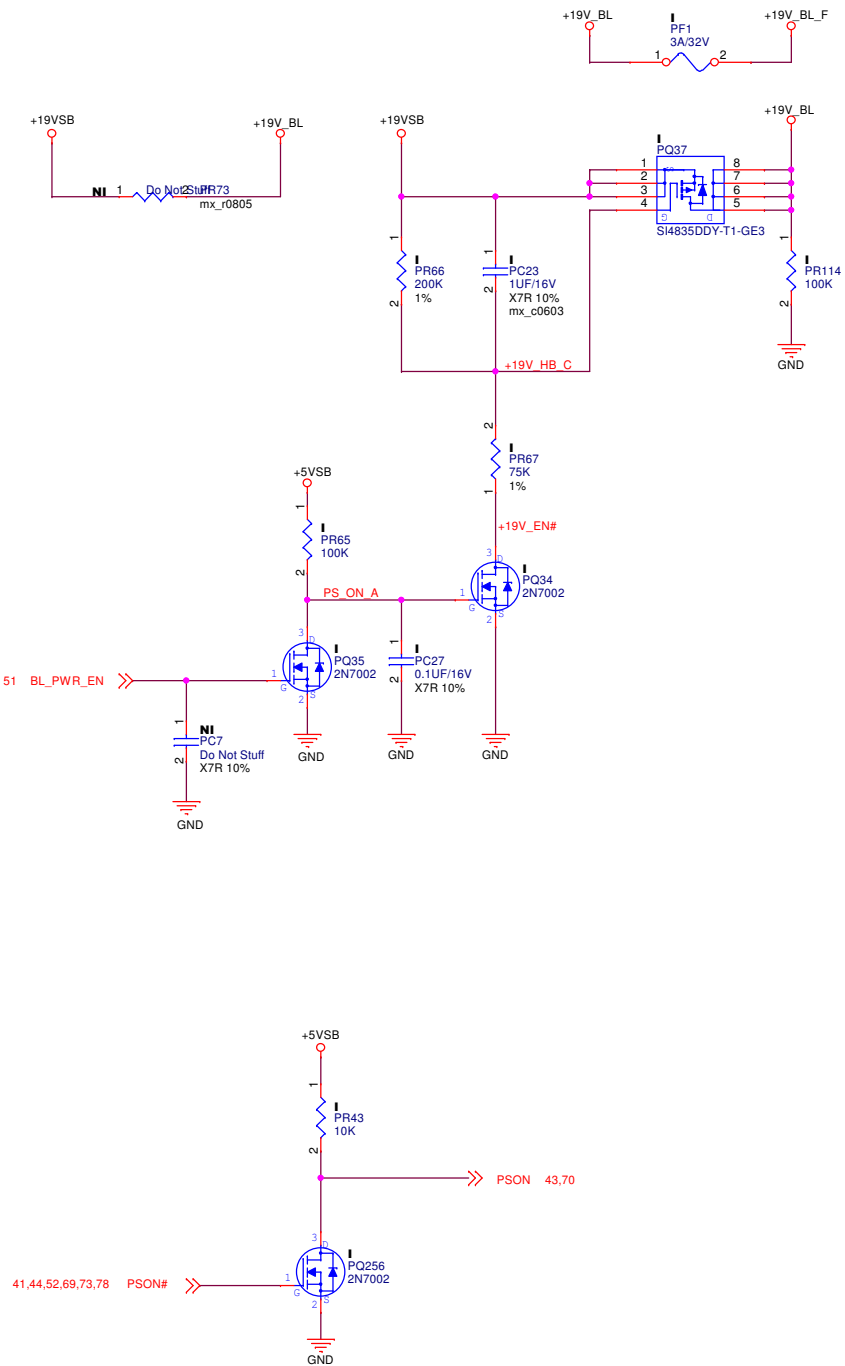
PEGATRON Title : +V_AXG DRIVER

Pegatron Corp. Engineer: ShunJing_Yang

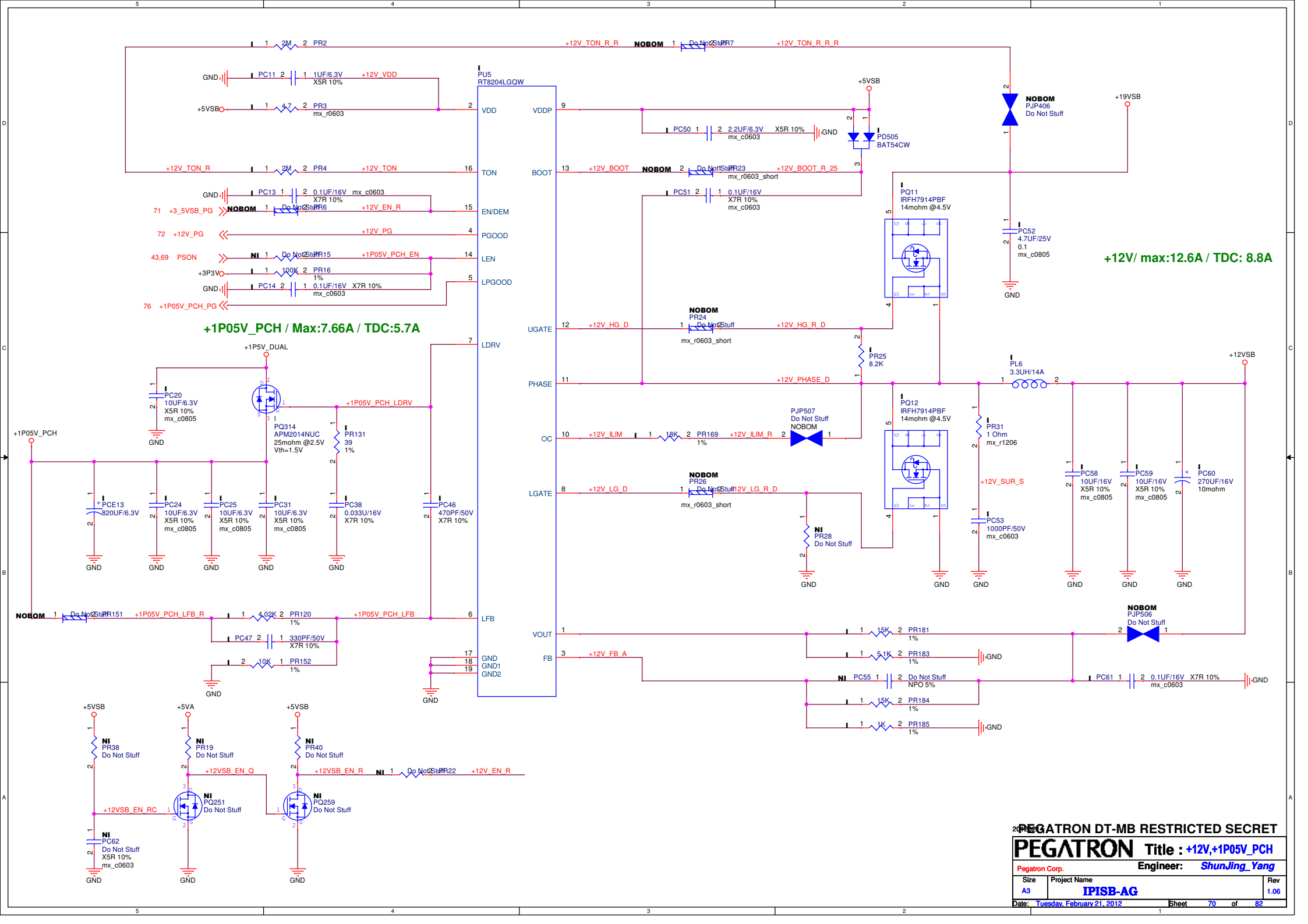
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

Date: Tuesday, February 21, 2012 Sheet 68 of 82

+19V / max=2.1A / TDC:1.58A



2012-2013 PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title : +19V,+5V,+3P3V	
Pegatron Corp.		Engineer: <u>ShunJing_Yang</u>	
Size A3	Project Name IPISB-AG	Rev 1.06	
Date: <u>Tuesday, February 21, 2012</u>		Sheet 69	of 82

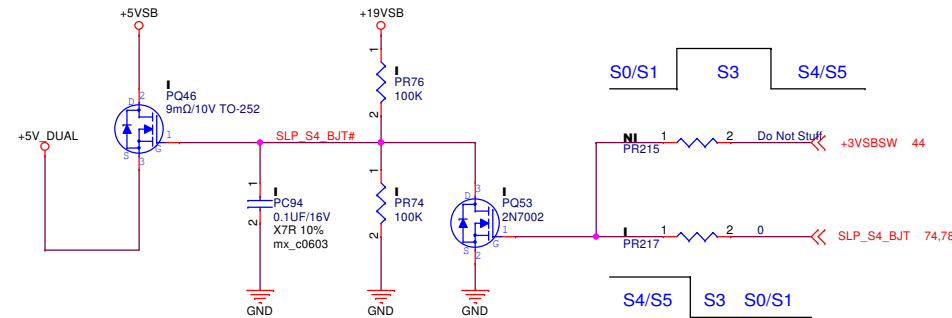


+12V/ max:12.6A / TDC: 8.8A

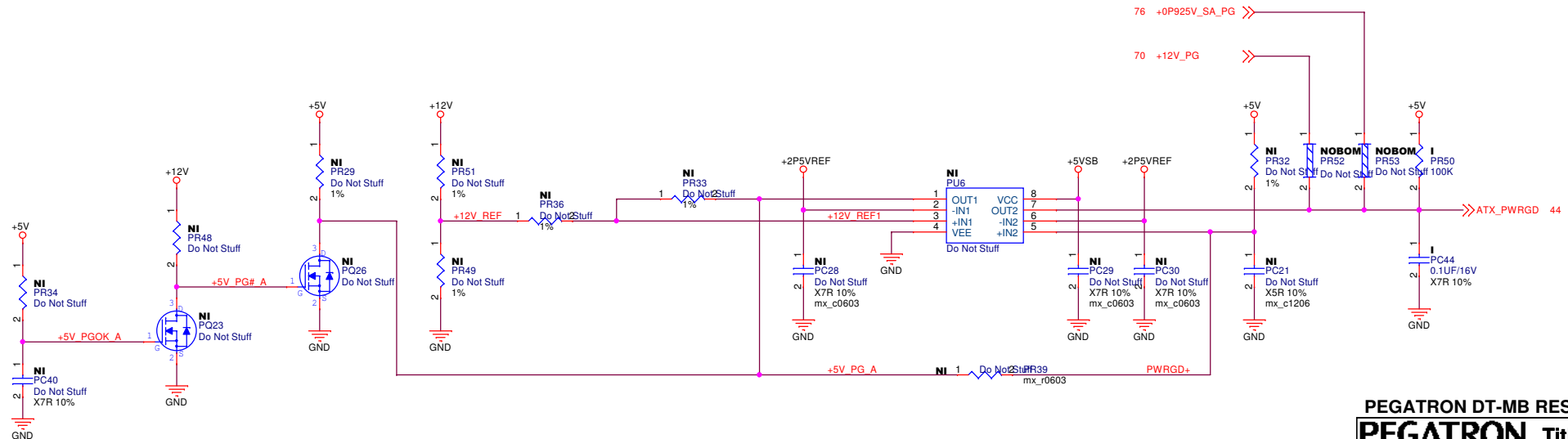
+1P05V_PCH / Max:7.66A / TDC:5.7A



+5V_DUAL /
max:5.3A / TDC:4A



ATX_PWRGD



PEGATRON DT-MB RESTRICTED SECRET

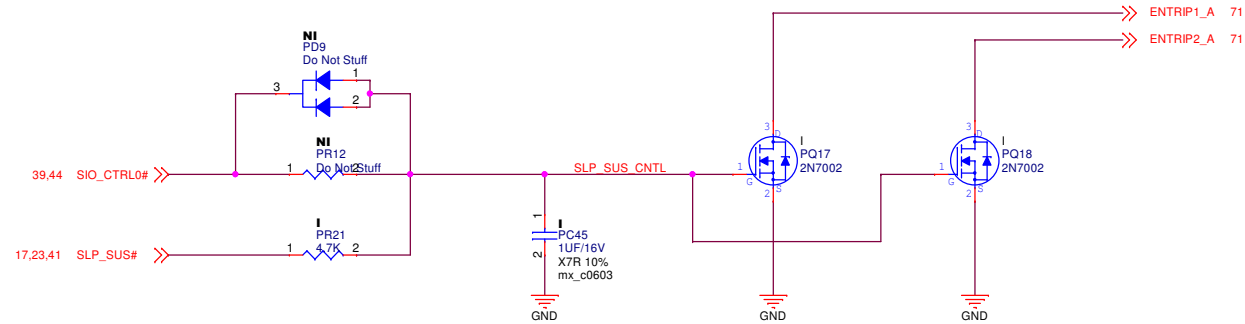
PEGATRON Title : **+5V_DUAL**

Pegatron Corp. Engineer: **ShunJing_Yang**

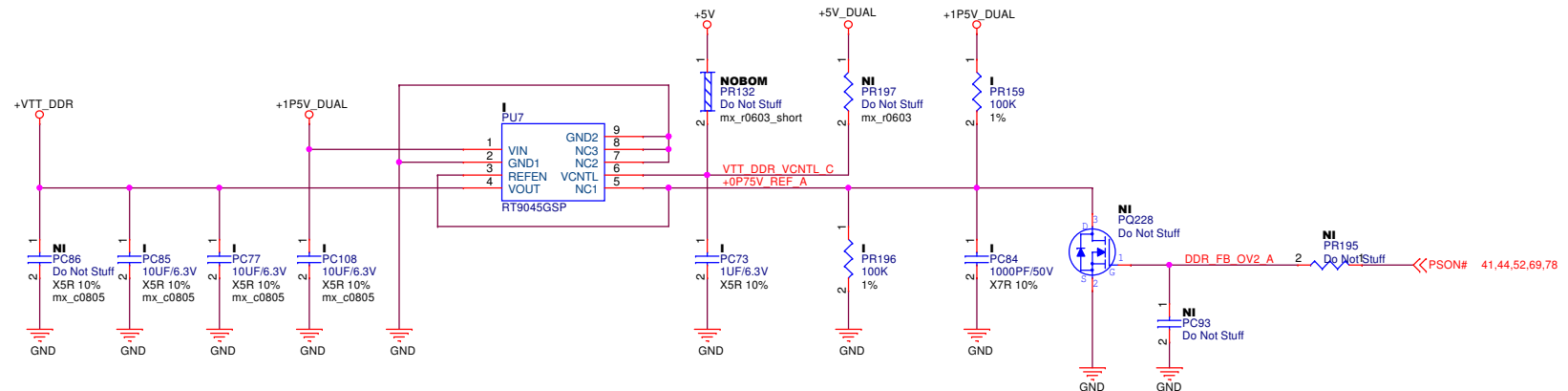
Size A3	Project Name IPISB-AG	Rev 1.06
------------	---------------------------------	-------------

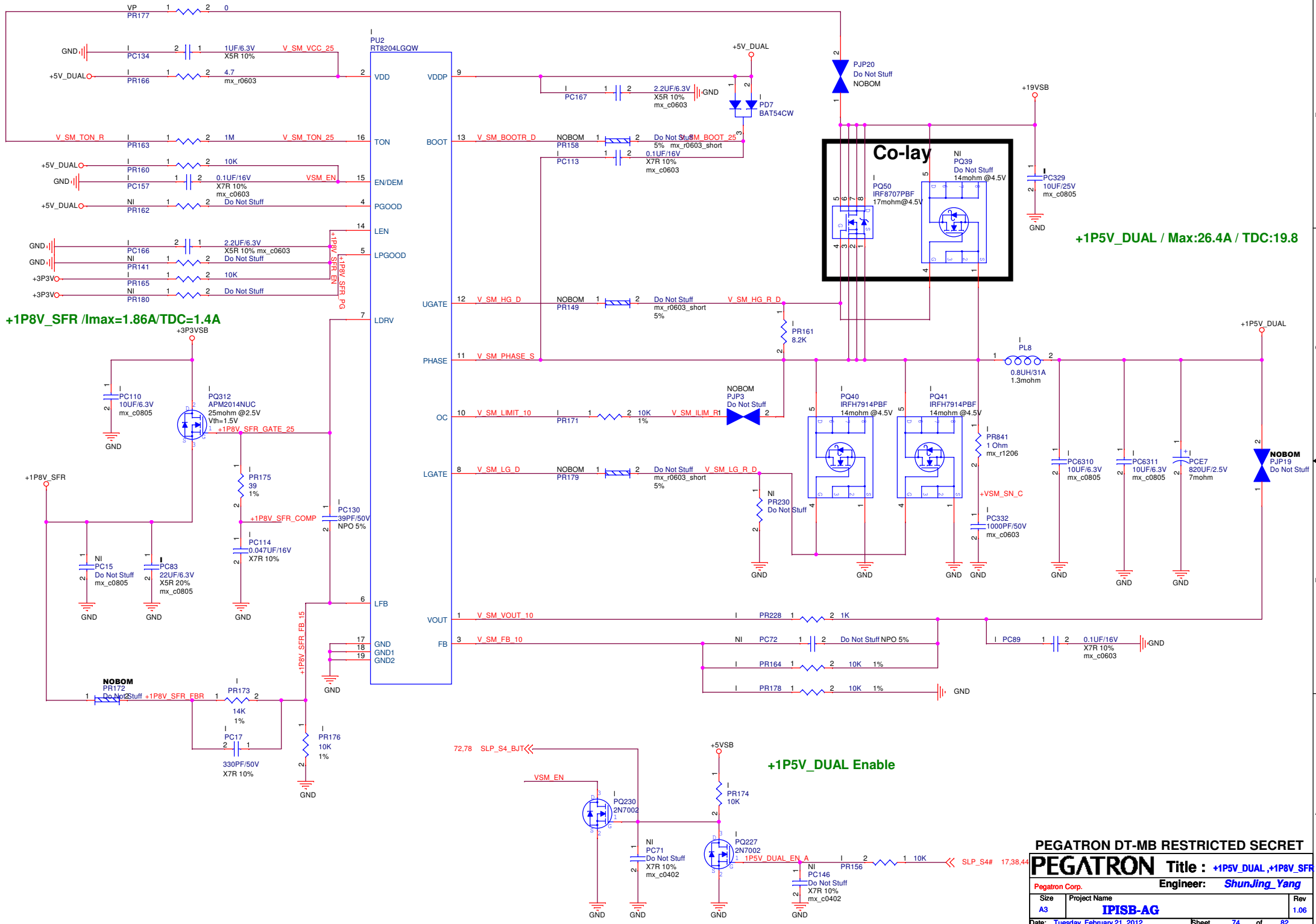
Date: **Tuesday, February 21, 2012** Sheet **72** of **82**

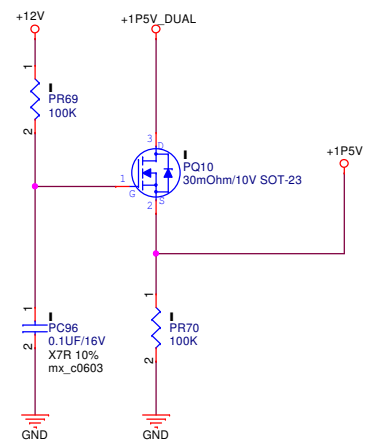
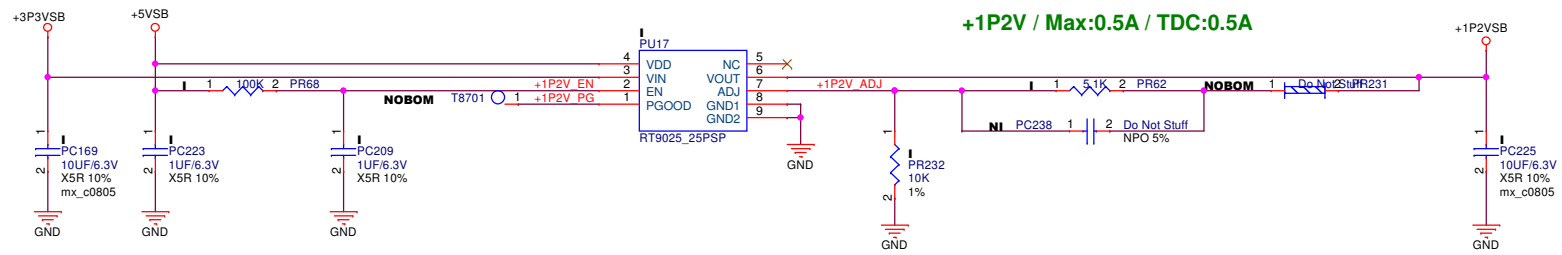
+5VSB-EN
+3VSB-EN

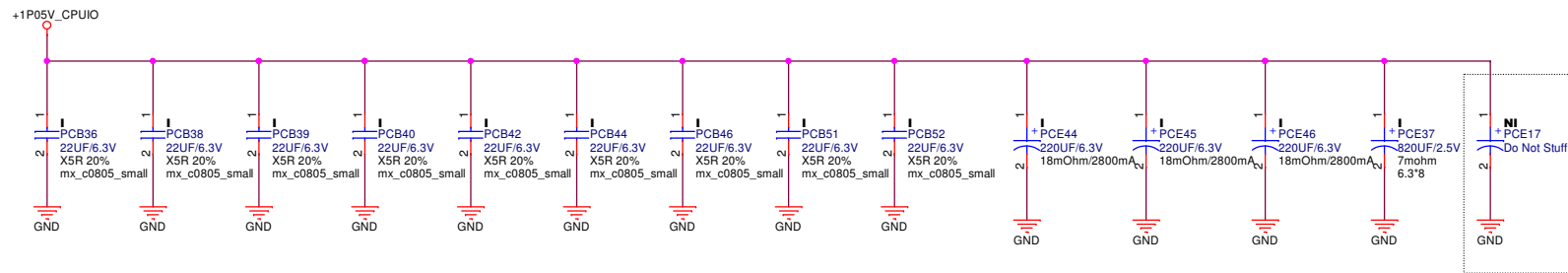
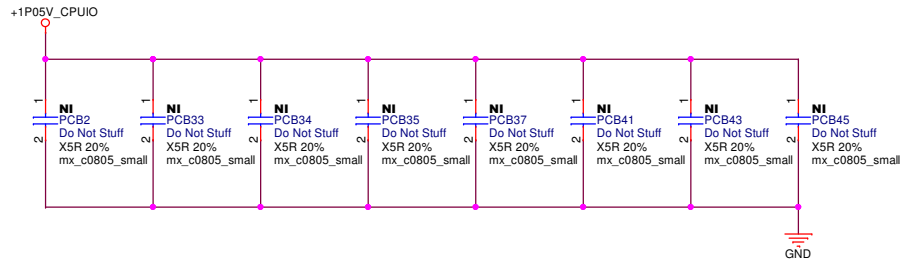
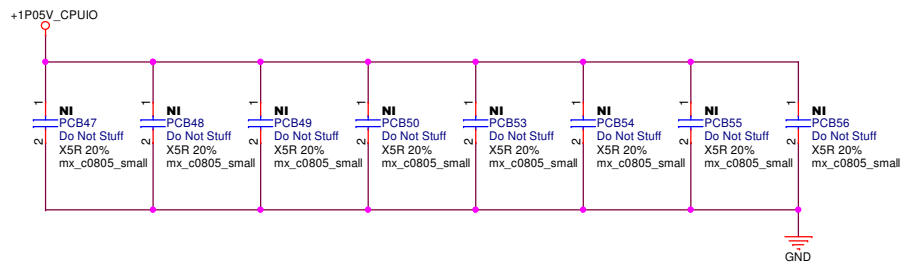


+VTT_DDR / Max:3A / TDC:2.25A

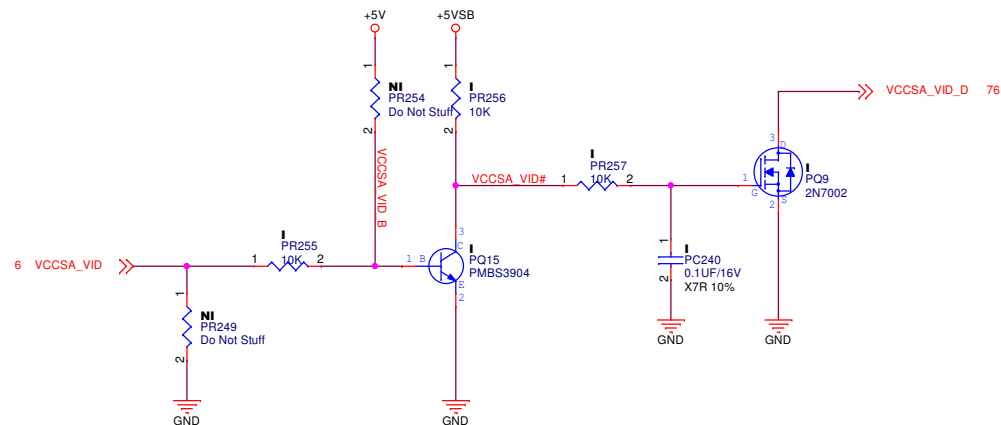






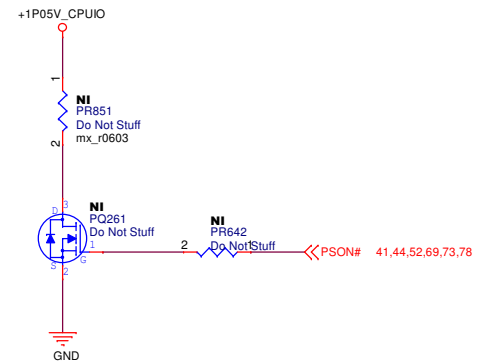
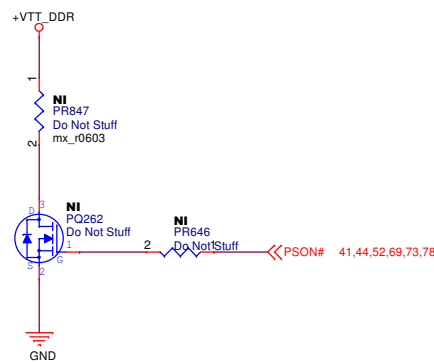
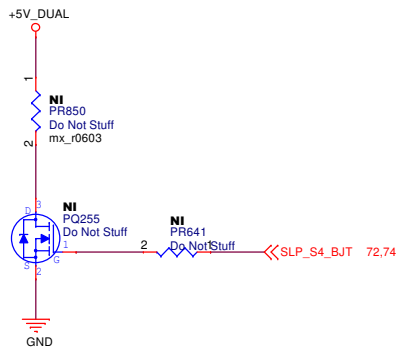
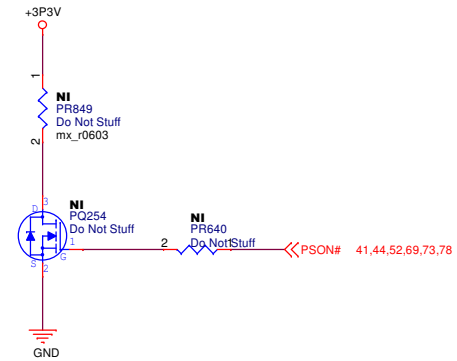
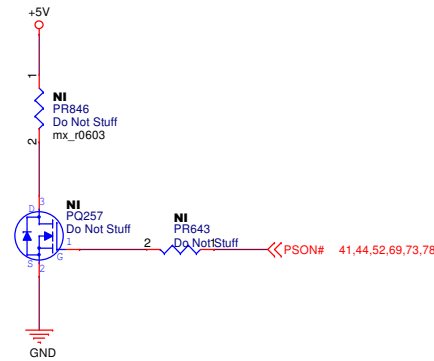
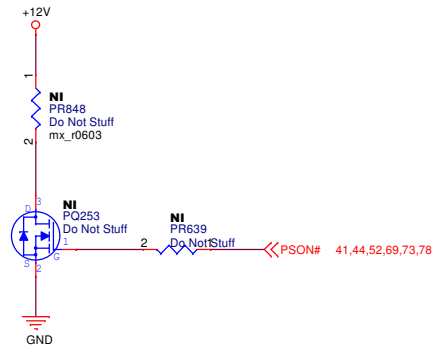


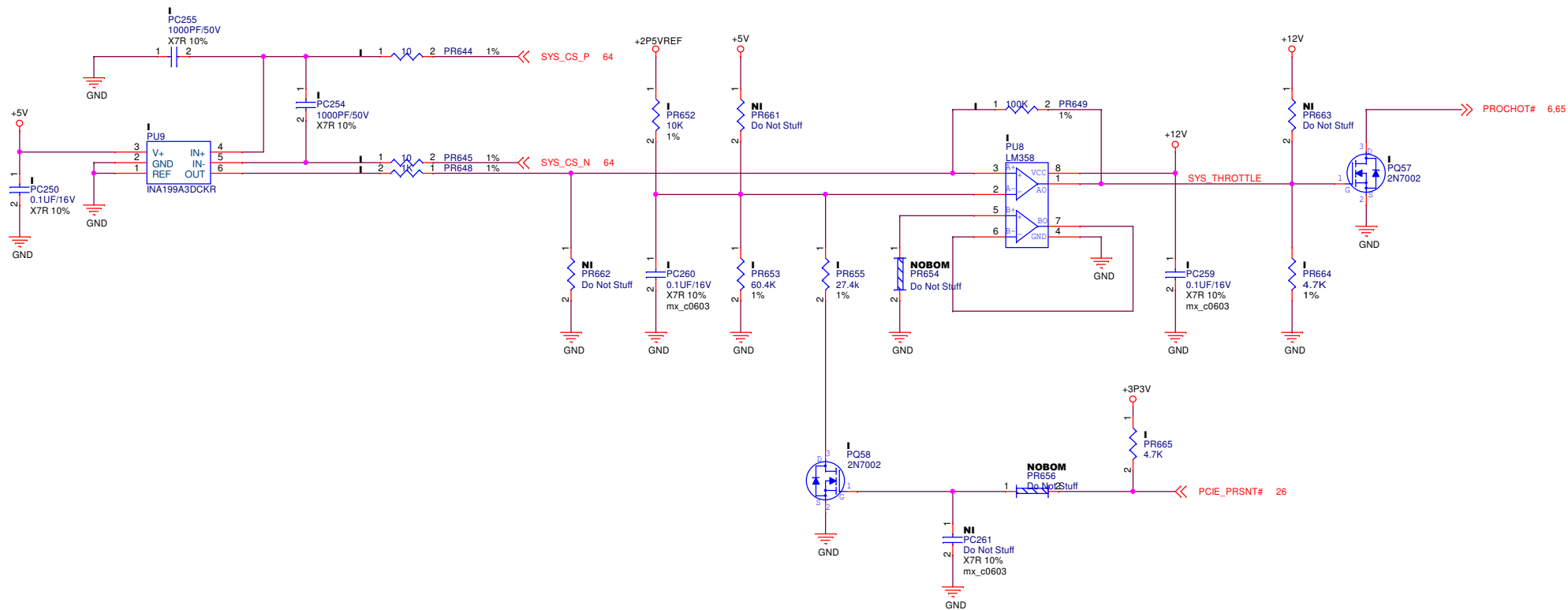
+0P925V_SA Selector



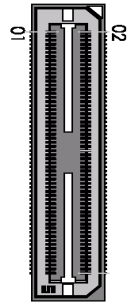
+1P05V_ME



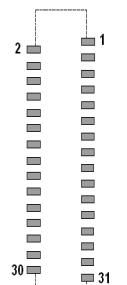




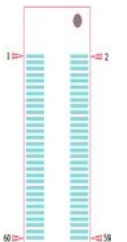




TOP SIDE VIEW

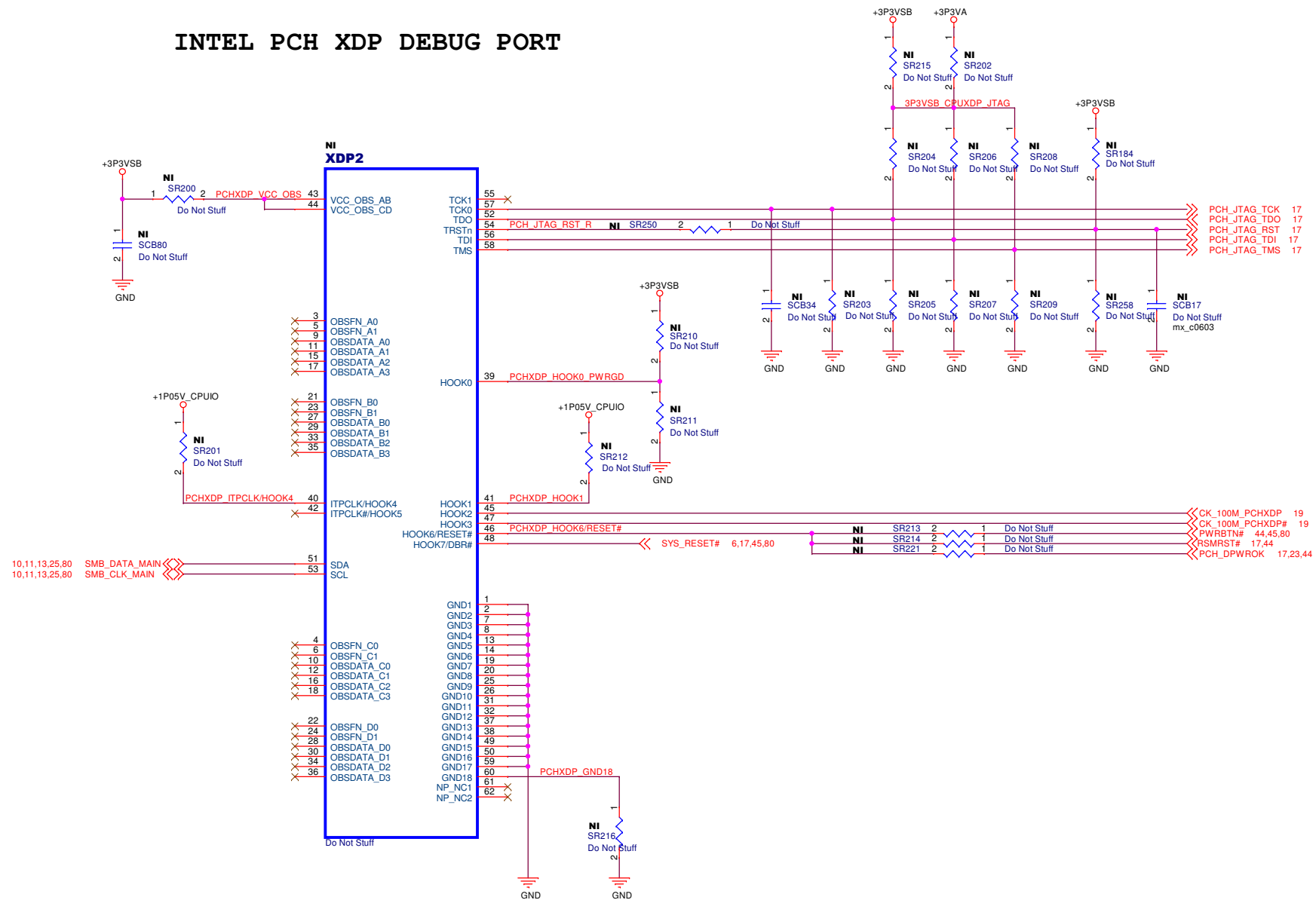


HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



BOTTOM SIDE VIEW

INTEL PCH XDP DEBUG PORT



20120221 PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH XDP DEBUG
Pegatron Corp. Engineer: ShunJing_Yang

Size	Project Name	Rev
A3	IPISB-AG	1.06
Date: Tuesday, February 21, 2012 Sheet 81 of 82		

