Model Name : V5MM2_Ezel_HW
File Name : LA-A021P

Compal Confidential

M/B Schematics Document

Intel Shark Bay ULT (Hasswell + Lynx Point-LP)

nVidia N14P-GT

2013-08-XX

REV:1.0

ZZZ1

Part Number	Description
DAZ0YY00100	PCB V5MM2 LA-A021P LS-A001P/A002P/A003P/A005P/A006P/A007P

Security Classification	Compal Secret Data		
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Title: *Cover Page*

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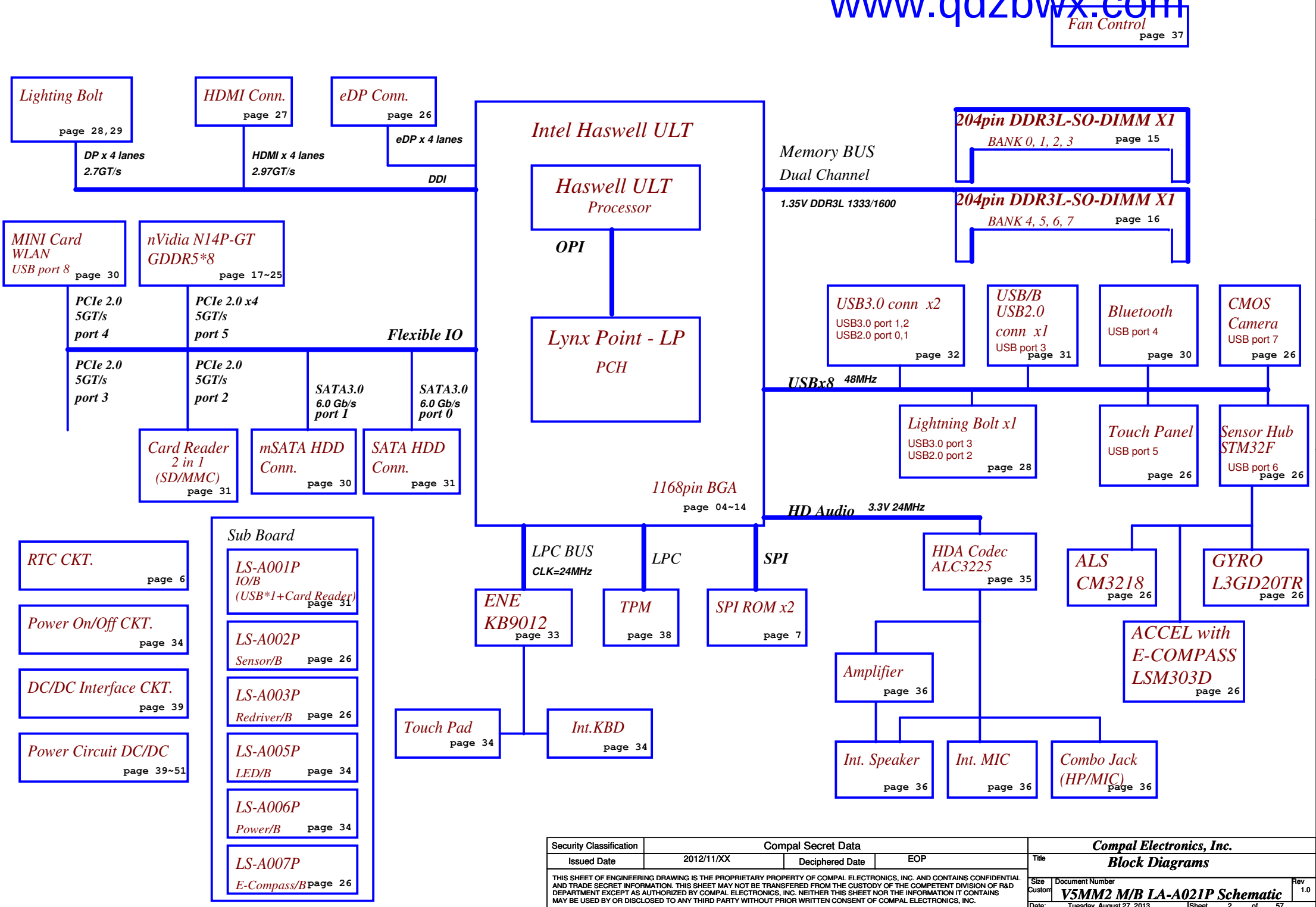
Date: Tuesday, August 27, 2013 | Sheet 1 of 57



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Title	Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDRIIIL	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU switched power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X

EC SM Bus2 address

Device	Address
On Board Thermal Senser	0100 110x
VGA Internal Thermal Senser	0100 000x
G Senser	0011 000x

PCH SM Bus address

Device		Address	
ChannelA	DIMM0	1001 000x	JDIMM1
ChannelB	DIMM1	1001 010x	JDIMM2

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

USB Port Table

USB 2.0	Port	
EHCI1	0	USB3.0 Connector (Left)
	1	USB3.0 Connector (Left)
	2	Lightning Bolt mDP Conn.
	3	USB2.0 (USB/B)
	4	Mini Card (WLAN+BT)
	5	Touch Panel
	6	Sensor Hub
	7	Camera

USB 3.0	Port	
XHCI	1	USB Port(Left 3.0)
	2	USB Port(Left 3.0)
	3	Lightning Bolt USB3.0
	4	

B0M Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
UMA only	UMA@
nVidia N14P-GT	DIS@
VRAM Selection	X76@
With GC6	GC6@
Without GC6	NGC6@
USB Charger	CHR@
TPM Module	TPM@
without TPM	NTPM@
Buzzer	BUZZ@
EMI,ESD parts	EMC@
	XEMC@
RF parts	RF@
	XRF@
Support DP++	DM@
no support DP++	NDM@

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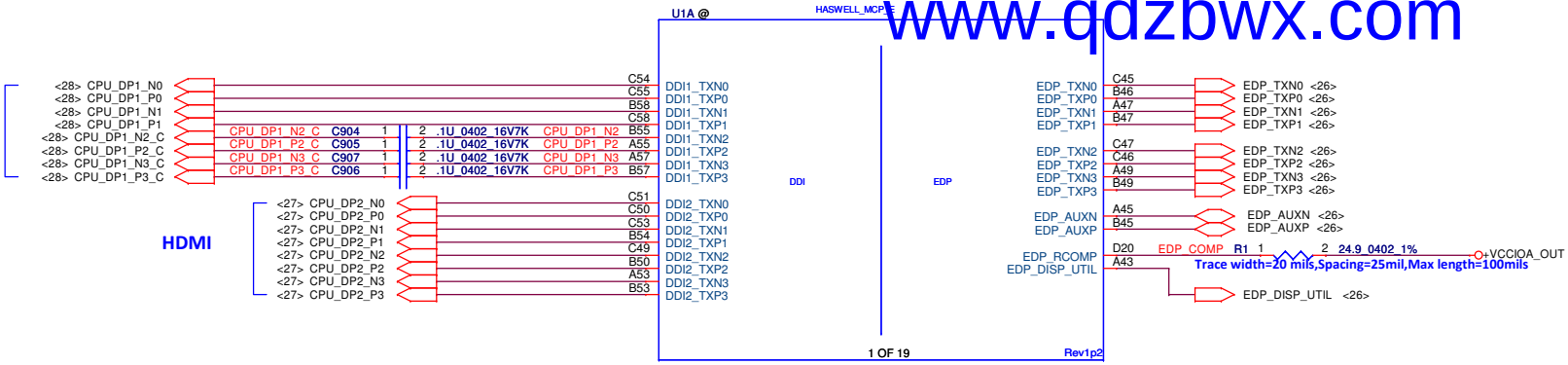
Size: Custom	Document Number: V5MM2 M/B LA-A021P Schematic		Rev: 1.0
Date: Tuesday, August 27, 2013	Sheet 3 of 57		

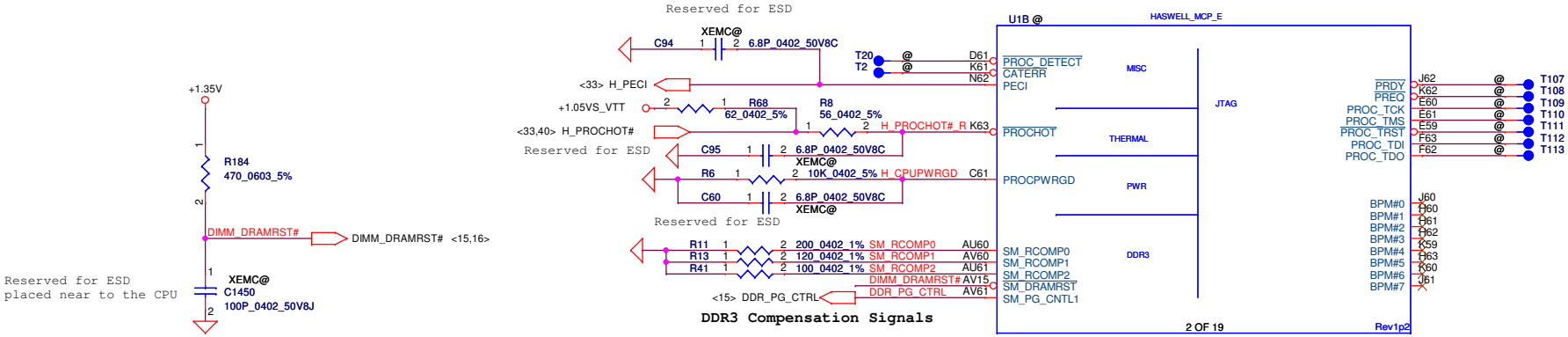
DP for Lightning-Bolt

1, 0 Directly to mDP connector

3, 2 connected to TI-HD3SS2521

HDMI





U1	U1	U1	U1
CPU_QDJB_B1	CPU_QDJ7_B1	CPU_QDJ8_B1	CPU_QEA4_C0
QDJB@	QDJ7@	QDJ8@	QEA4@
SA000067060	SA000067H50	SA00006G710	SA00006NM00

ES:
SA000067060 - QDJB B1 0.8G
SA000067H50 - QDJ7 B1 0.8G
SA00006G710 - QDJ8 B1 0.8G

Pre-QS:
SA00006NM00 - QEA4 C0 1.3G

43L:
4319NZBOL05
4319NZBOL06
4319NZBOL07
4319NZBOL08
4319NZBOL09

U1	U1	U1	U1	U1
CPU_QDJB_B1	CPU_QDJ7_B1	CPU_QDJ6_B1	CPU_QDJ9_B1	CPU_QDJC_B1
QDJBe@	QDJ7e@	QDJ6@	QDJ9@	QDJC@
SA000067060	SA000067H50	SA00006FY20	SA00006G120	SA00006EY30

43L:
4319NZBOL01
4319NZBOL02
4319NZBOL03
4319NZBOL04

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Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: HSW MCP(1/11) DDI,MSIC,XDP

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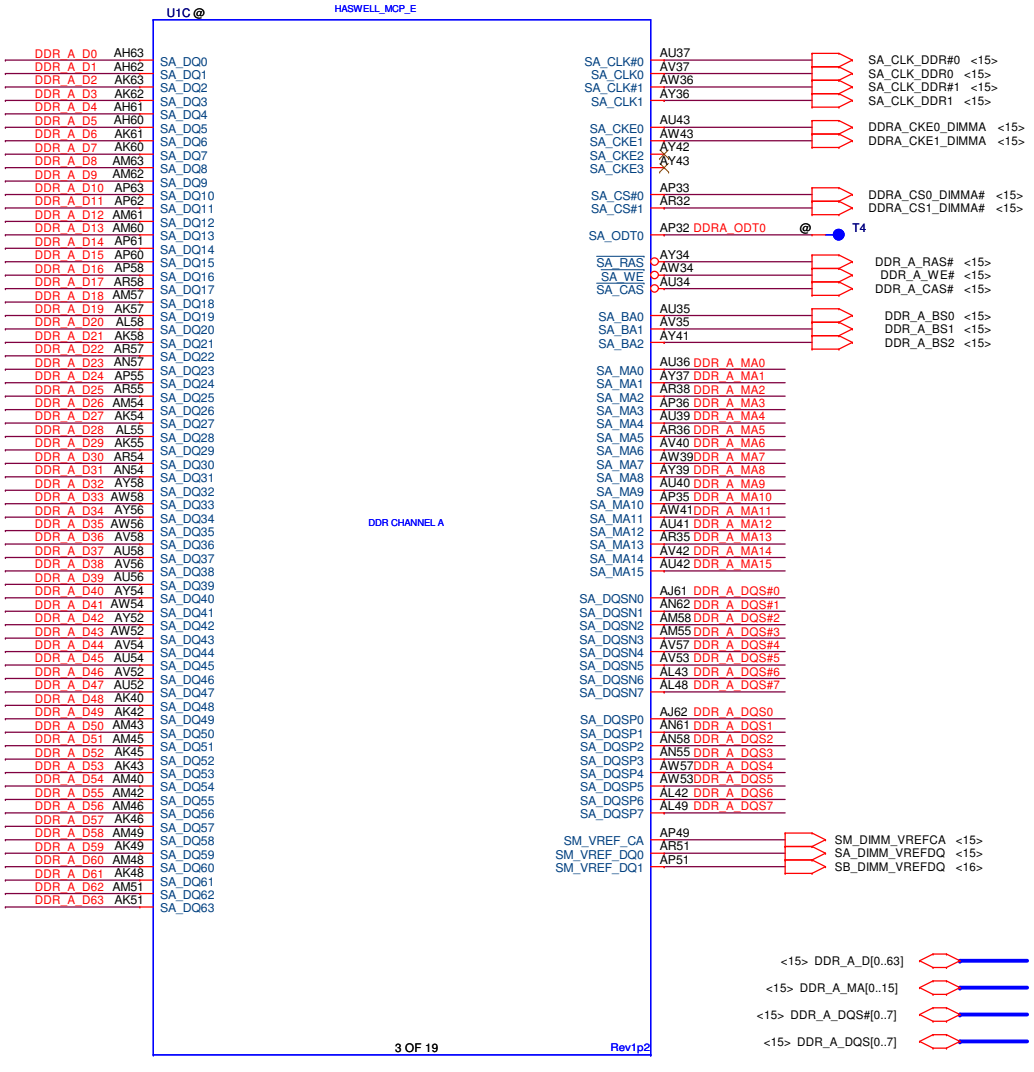

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Compal Electronics, Inc.			
Title	HSW MCP(2/11) DDRIII		
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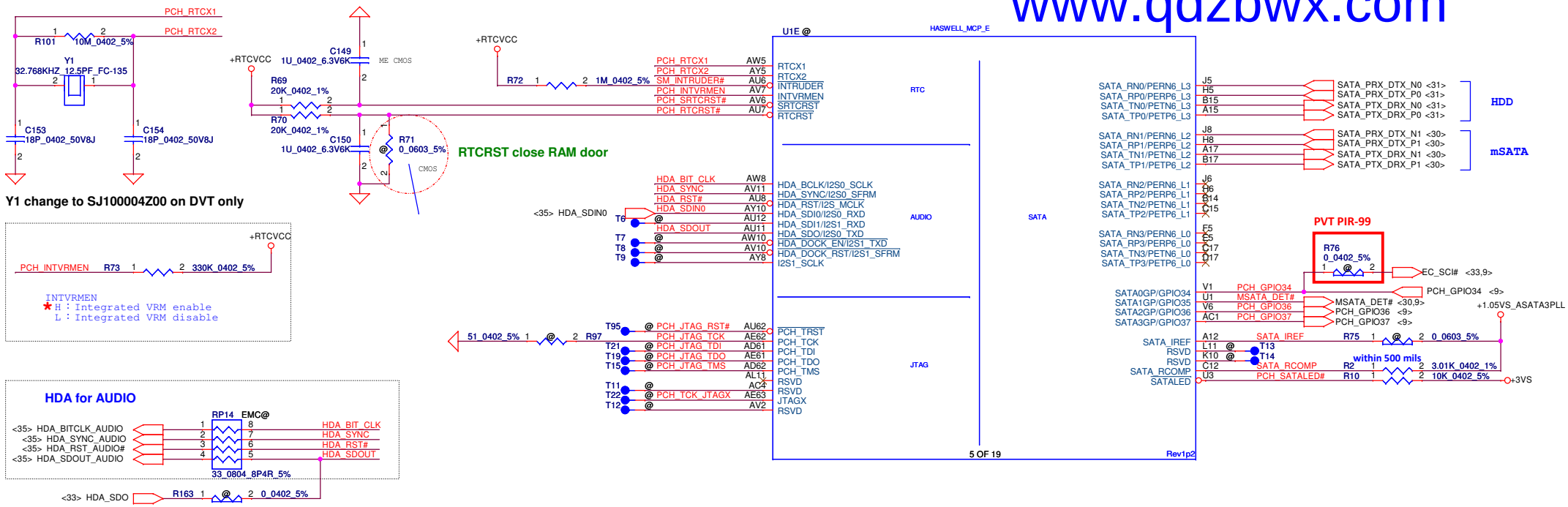
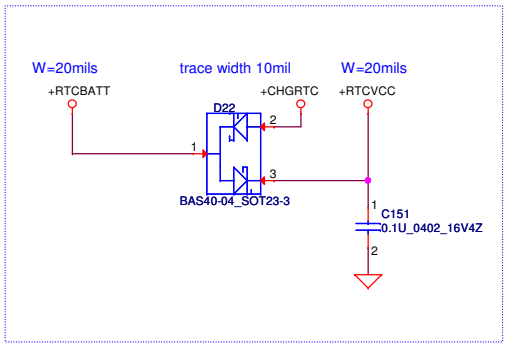


Y1 change to SJ100004Z00 on DVT only



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Compal Electronics, Inc.			
Title	HSW MCP(3/11) RTC,SATA,XDP		
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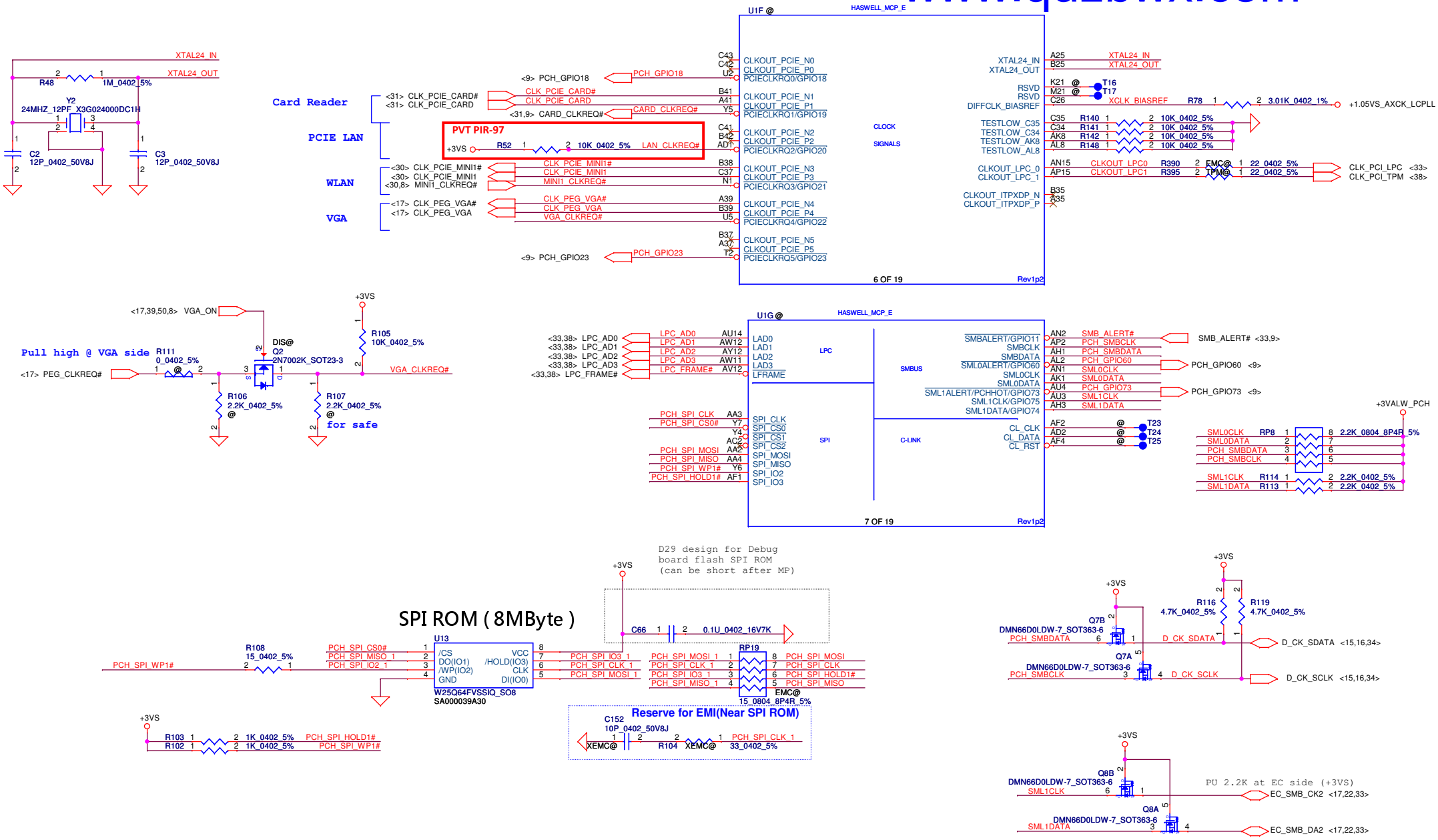

Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.			
Title	HSW MCP(4/11) CLK,SPI,SMBUS		
Size: Custom	Document Number: V5MM2 M/B LA-A021P Schematic		Rev: 1.0
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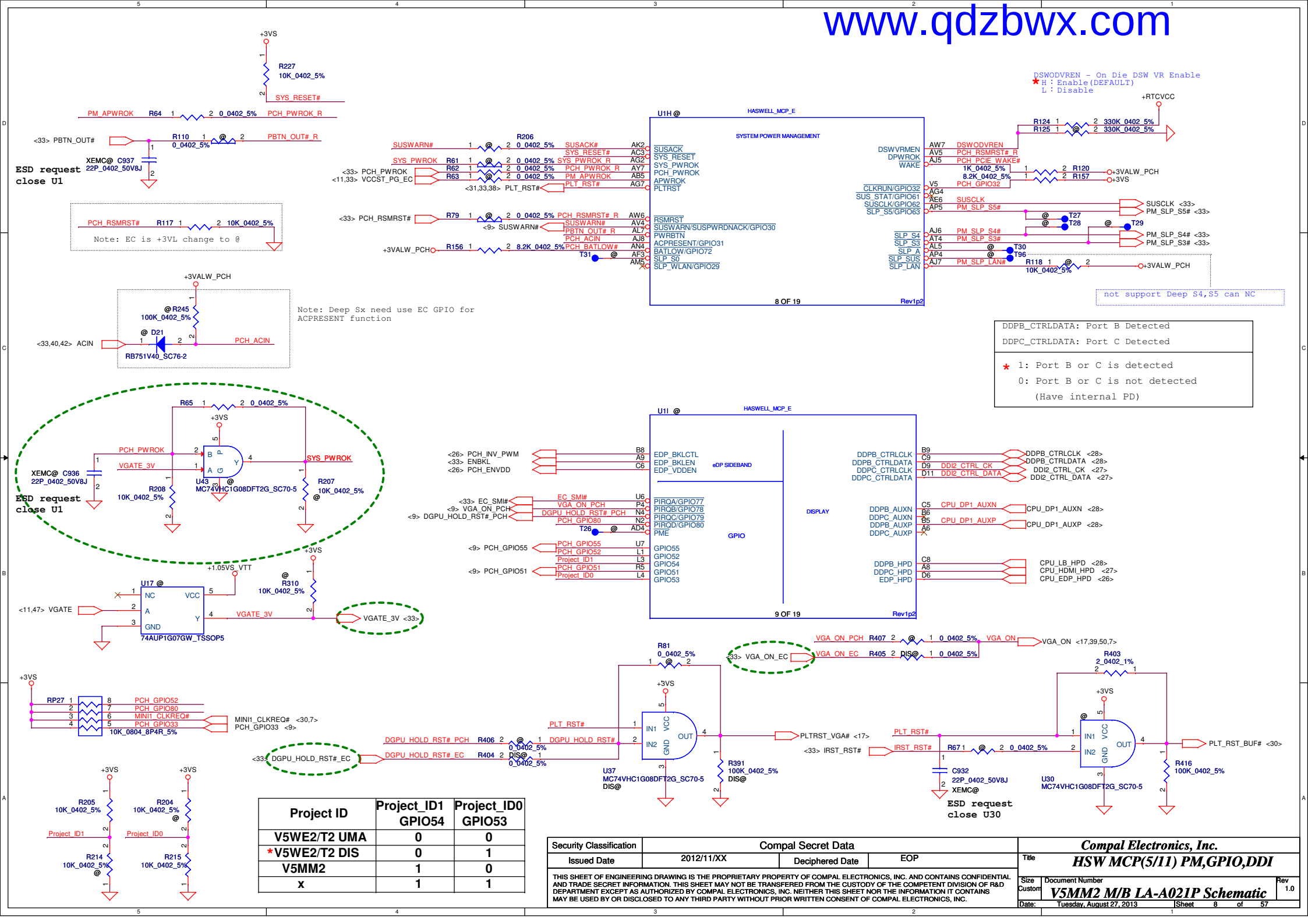

Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
V5WE2/T2 UMA	0	0
*V5WE2/T2 DIS	0	1
V5MM2	1	0
x	1	1

Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: HSW MCP(5/11) PM,GPIO,DDI

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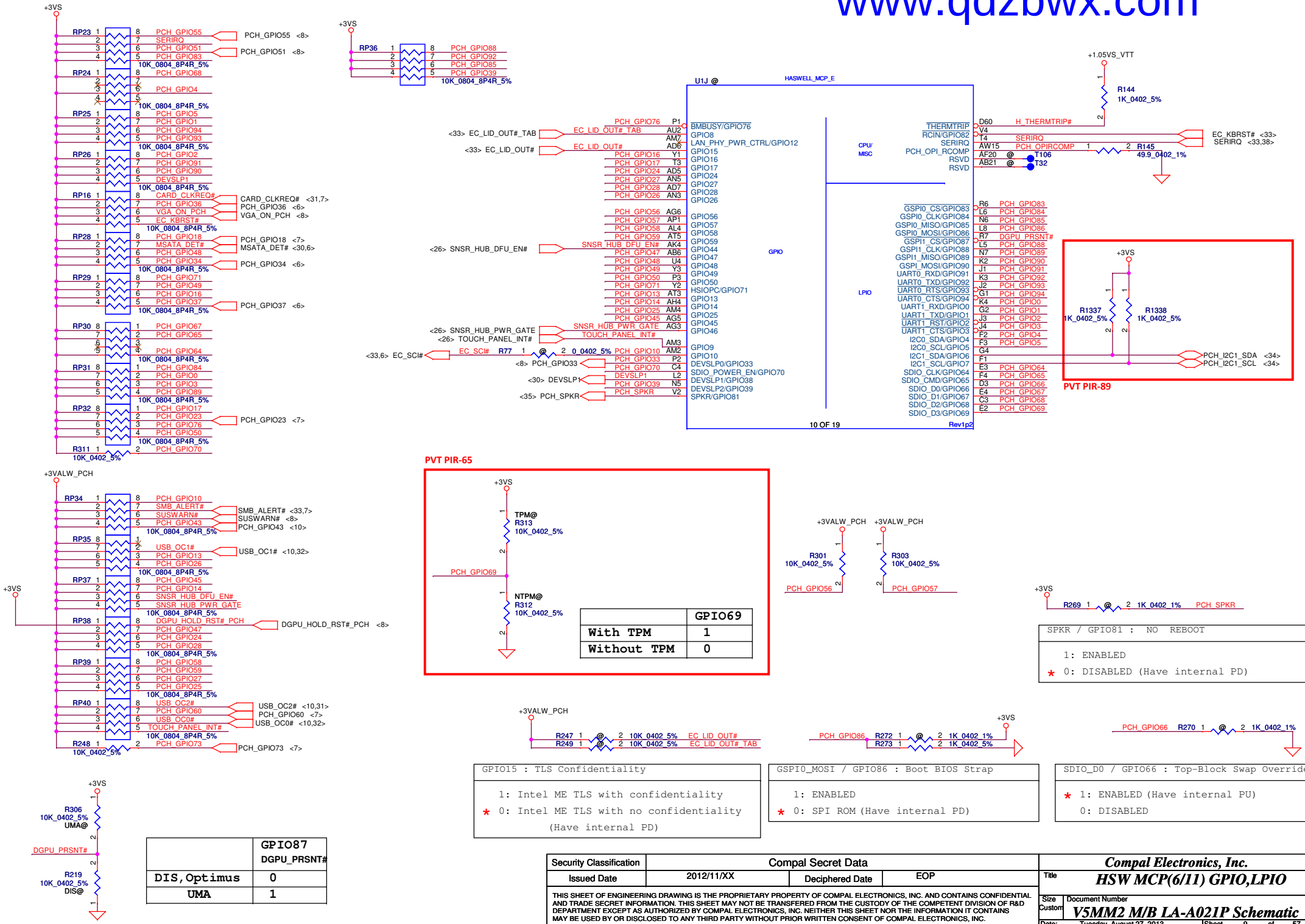

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Compal Electronics, Inc.

Title: HSW MCP(6/11) GPIO,LPIO

Size	Document Number	Rev
Custom	V5MM2 M/B LA-A021P Schematic	1.0

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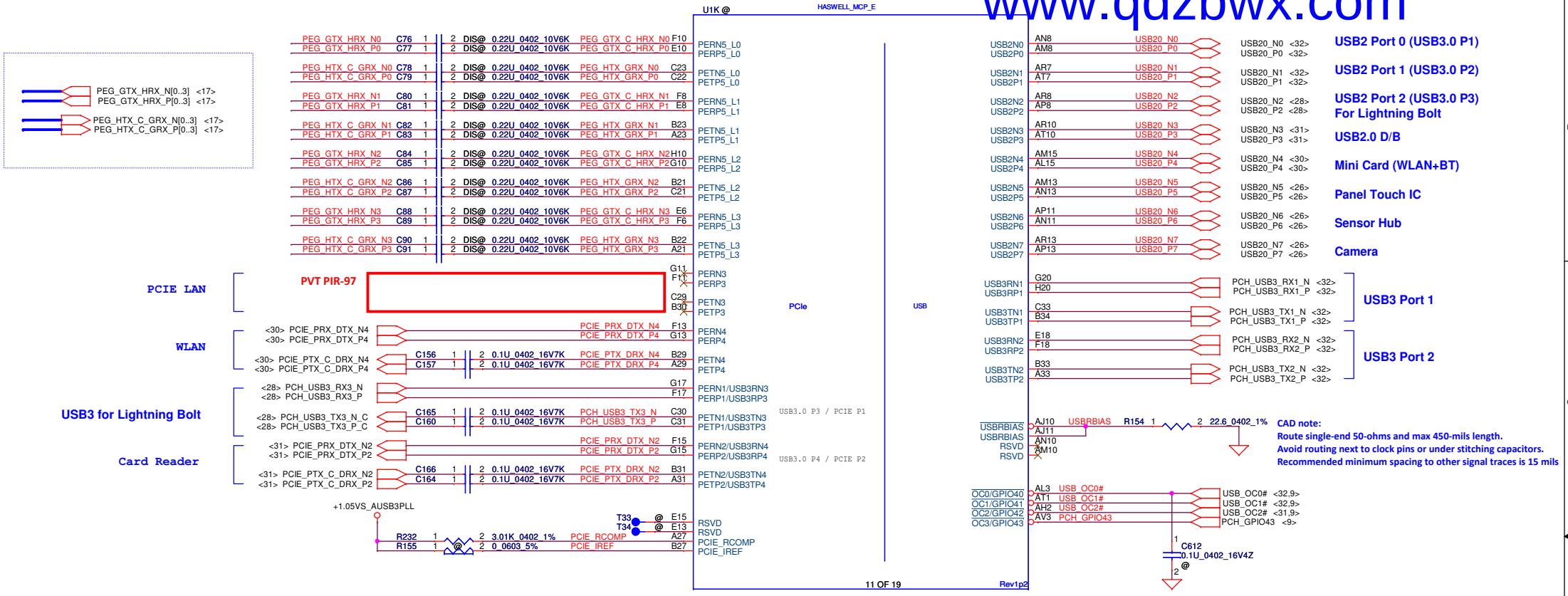

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Compal Electronics, Inc.			
Title	HSW MCP(7/11) PCIE,USB		
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Shark Bay ULT have internal gate for VDDQ

+1.35V — @J2 — +1.35V_CPU

JUMP_43X118

PVT PIR-99

+3VS — R422 100K_0402_5% @ — U16 (74AUP1G07GW_TSSOP5: NC, VCC, A, Y, GND) — +3VALW_PCH — +1.05VS_VTT — R309 10K_0402_5%

<33,8> VCCST_PG_EC — R180 0_0402_5% — VCCST_PG_EC_R

C925 22P_0402_50V8J XEMC@

ESD request close U16

<33,45> VCCST_PWRGD — R166 0_0402_5%

EC端加0ohm斷點

C920 22P_0402_50V8J XEMC@

ESD request close PU601

SVID ALERT

+1.05VS_VTT — Place the PU resistors close to CPU

R171 75_0402_1%

R172 43_0402_1%

<47> VR_ALERT# — H_CPU_SVIDALRT#

SVID DATA

+1.05VS_VTT — Place the PU resistors close to CPU

R173 130_0402_1%

R174 @ 0_0402_5%

<47> VR_SVID_DATA — VIDSOUT

+CPU_CORE — R177 100_0402_1% — Note: 0 ohm PLACED CLOSE TO CPU

VCC_SENSE_R — R178 0_0402_5% — VCC_SENSE <47>

<13> VSS_SENSE_R — R235 0_0402_5% — VSS_SENSE <47>

R233 100_0402_1%

+1.05VS_VTT — @ R169 150_0402_1% — CPU_PWR_DEBUG — R170 10K_0402_5% @

+1.05VS_VTT — EMC@ C8 22U_0805_6.3V6M — C7 10U_0402_6.3V6K @

PVT PIR-76

+CPU_CORE

+1.35V_CPU — VDDQ: AH26, AJ31, AJ33, AJ37, AN33, AP43, AR48, AY35, AY40, AY44, AY50

+CPU_CORE — VCC: F59

+VCCIO_OUT — VCC_SENSE_R — R164 0_1206_5% — +1.05VS_VTT

+VCCIOA_OUT

VCC_SENSE: E63; VCCIO_OUT: A59; VCCIOA_OUT: E20

T37 @ L59 RSVD; T38 @ J58 RSVD; T39 @ N58 RSVD; T40 @ AC58 RSVD; T41 @ AB23 RSVD; T42 @ AD23 RSVD; T43 @ AA23 RSVD; T44 @ AE59 RSVD

<47> VR_SVID_CLK — R165 0_0402_5% — H_CPU_SVIDCLK: N63; VIDSOUT: L63

<47> VR_ON — R167 0_0402_5% — PCH_VR_EN: F60

<47,8> VGATE — R168 0_0402_5% — VR_READY: C59

C167 0.1U_0402_16V7K

CPU_PWR_DEBUG: D63; H_CPU_SVIDALRT#: L62; VIDALERT; VIDSCLK; VIDSOUT; VCCST_PWRGD; VR_EN; VR_READY; VSS; PWR_DEBUG; VSS

Reserved Only

T45 @ P60 RSVD_TP; T46 @ P61 RSVD_TP; T47 @ N59 RSVD_TP; T48 @ N61 RSVD_TP; T98 @ T59 RSVD_TP

T142 @ AD60 RSVD; T143 @ AD59 RSVD; T144 @ AA59 RSVD; T141 @ AE60 RSVD; T140 @ AC59 RSVD; T147 @ AG58 RSVD; T145 @ U59 RSVD; T146 @ V59 RSVD

+1.05VS_VTT — +CPU_CORE

VCCST: AC22, AE22, AE23

VCC: AB57, AD57, AG57, C24, C28, C32

HSW ULT POWER

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Rev1p2

VCC: C36, C40, C44, C48, C52, C56, E23, E25, E27, E29, E31, E33, E35, E37, E39, E41, E43, E45, E47, E49, E51, E53, E55, E57, F24, F28, F32, F36, F40, F44, F48, F52, F56, G23, G25, G27, G29, G31, G33, G35, G37, G39, G41, G43, G45, G47, G49, G51, G53, G55, G57, H23, J23, K23, K57, L22, M23, M57, P57, U57, W57

VDDQ DECOUPLING

+1.35V_CPU

@ C8 2.2U_0402_6.3V6M; C9 2.2U_0402_6.3V6M; C10 2.2U_0402_6.3V6M; C11 2.2U_0402_6.3V6M; C12 10U_0603_6.3V6M; C15 10U_0603_6.3V6M; C16 10U_0603_6.3V6M; C17 10U_0603_6.3V6M; C18 330U_2.5V_M

+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

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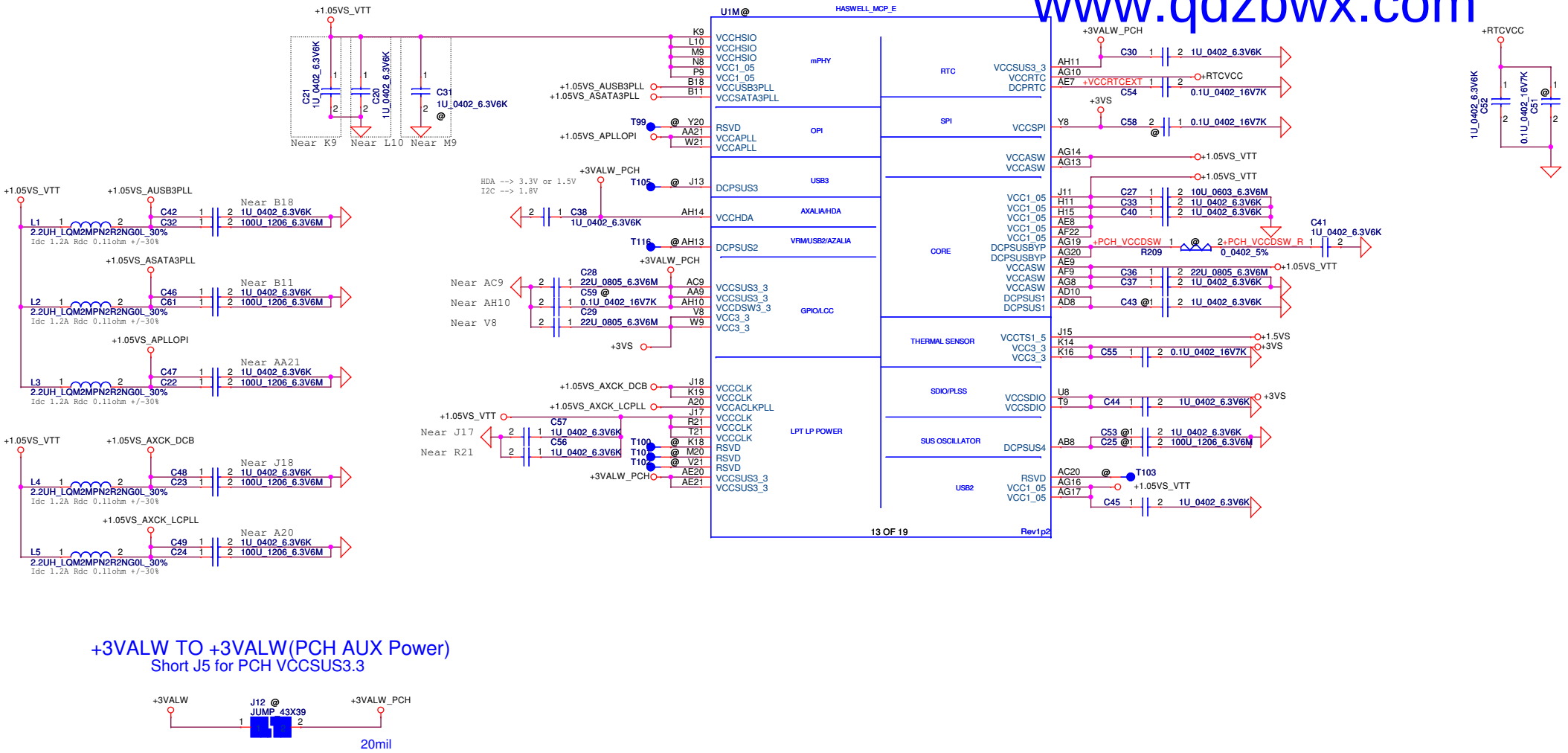

+3VALW TO +3VALW(PCH AUX Power)

Short J5 for PCH VCCSUS3.3

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Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: HSW MCP(9/11) Power

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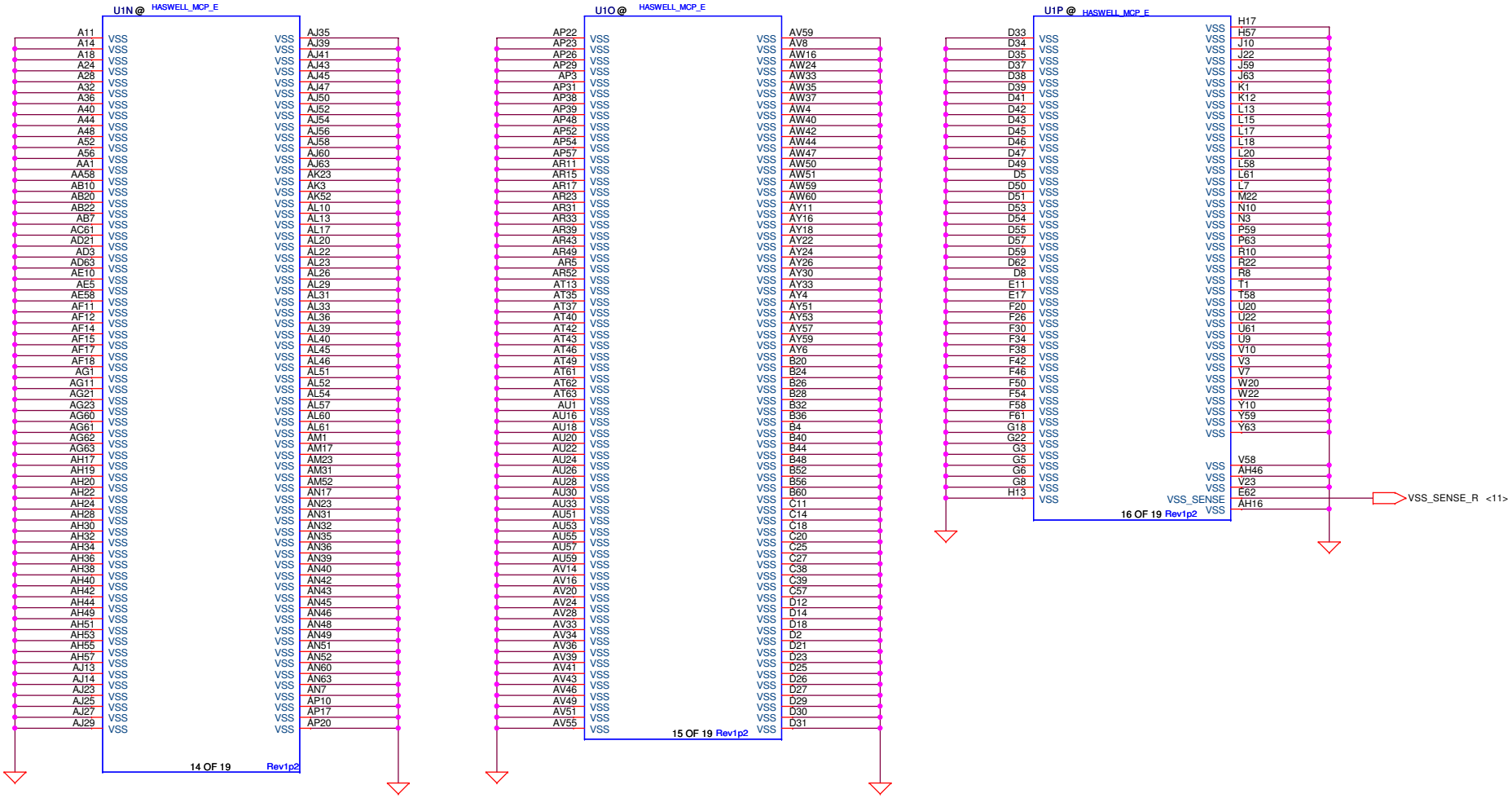

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Compal Electronics, Inc.		
Title: HSW MCP(10/11) GND		
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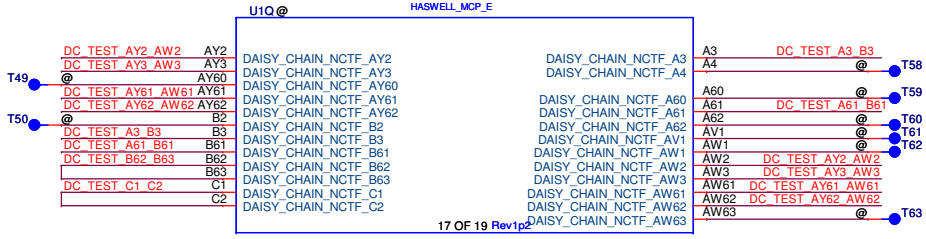
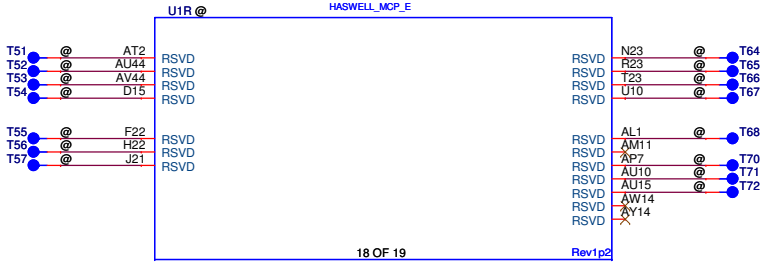
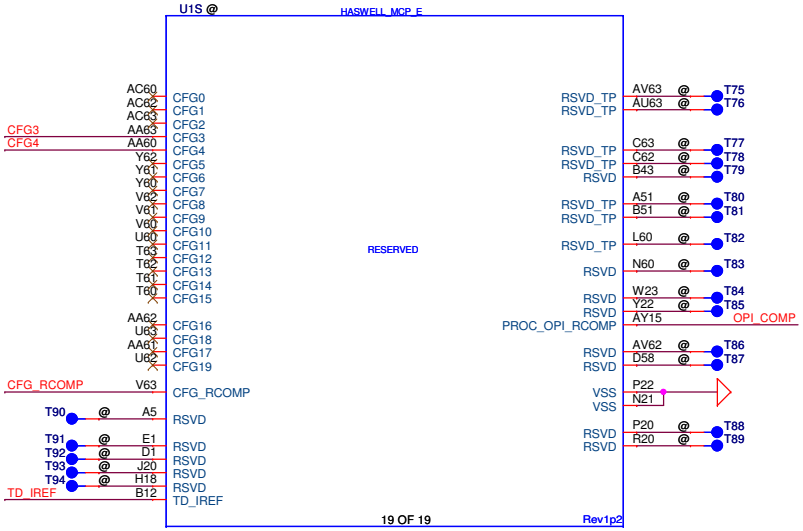
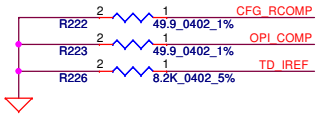
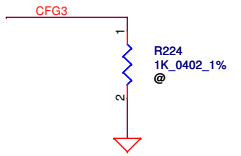




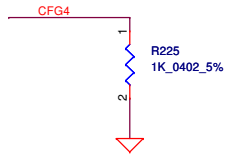




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title	HSW MCP(11/11) RSVD		
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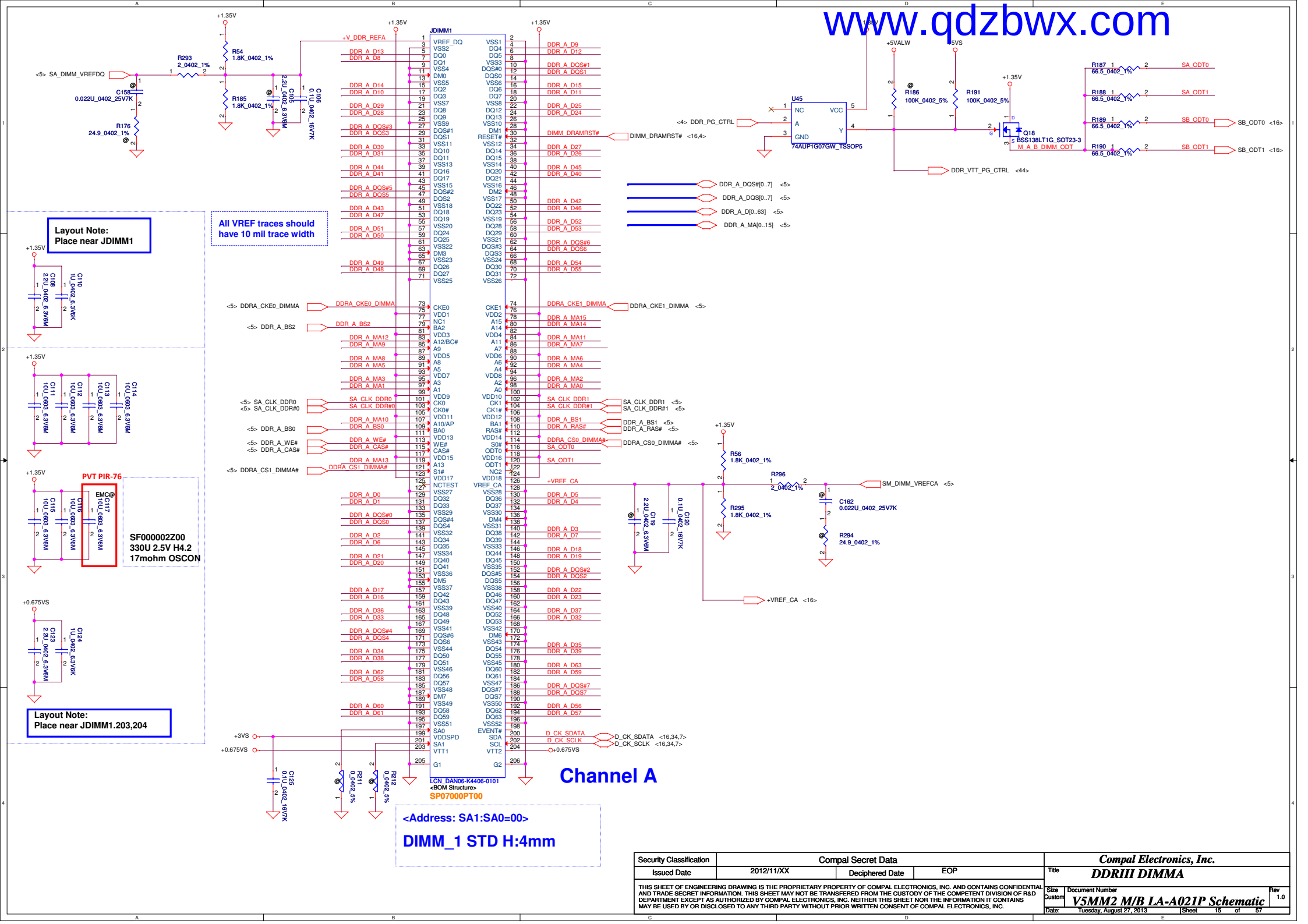

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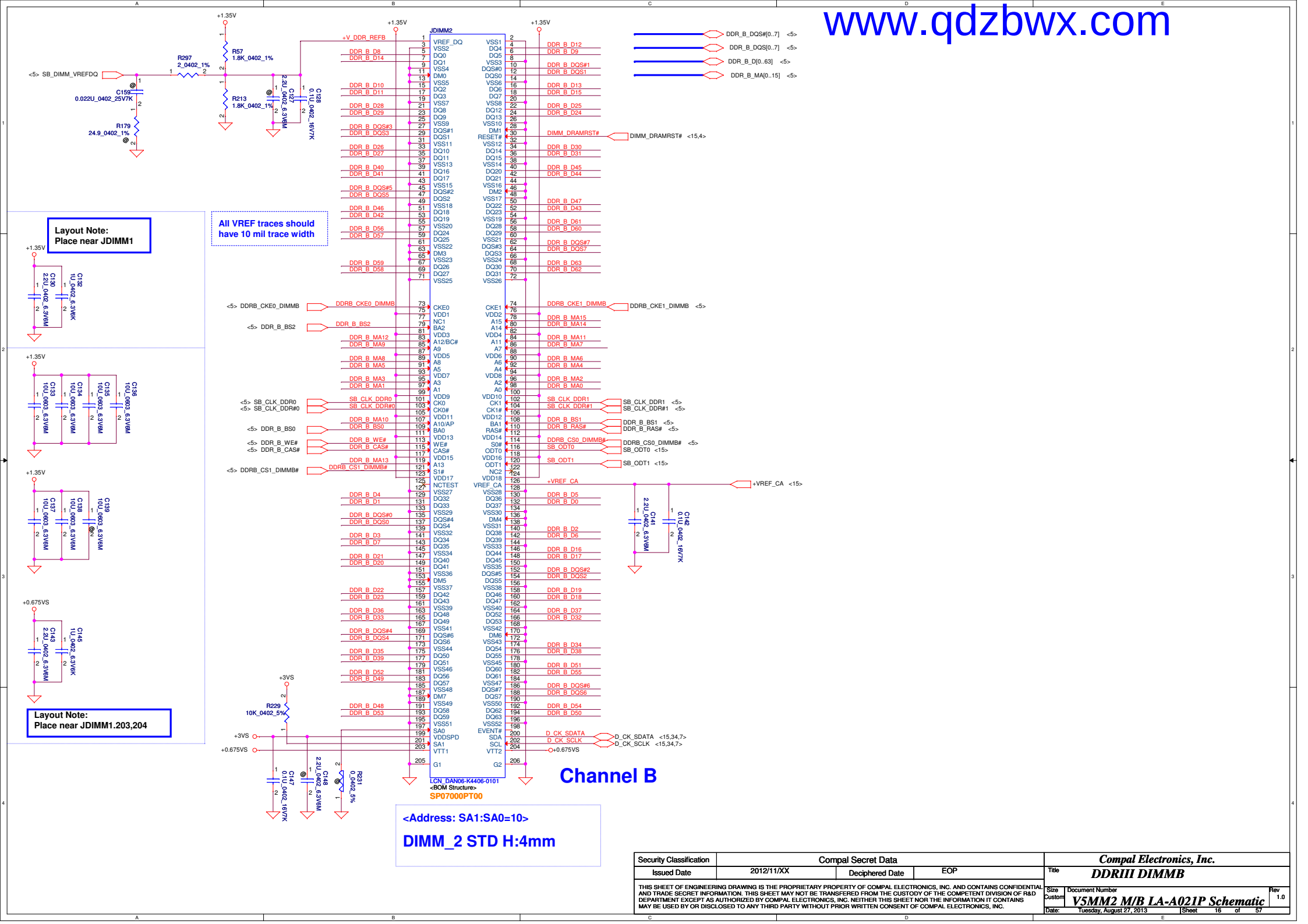
Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: V5MM2 M/B LA-A021P Schematic		Rev: 1.0
Date: Tuesday, August 27, 2013		Sheet: 15 of 57	



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Title: DDRIII DIMMB			
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Date: Tuesday, August 27, 2013		Sheet: 16 of 57	

GPIO need confirm with nVidia

GPIO	I/O	USAGE
GPIO0	I	FB_CLAMP_MON
GPIO1	O	MEM_VD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	Reserved
GPIO6	O	FB_CLAMP_TGL_REQ
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	O	FRM_CLK
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21		Reserved
GPIO22		
GPIO23		
GPIO24		

U62 Change to SCS00000Z00

NV FAE Recommand ; 10/31

Place Under AD8

Place Under AE8,AD7

SM010019400 3000ma 33ohm@100mhz DCR 0.05

SM010028480 1500ma 180ohm@100mhz DCR 0.18

Near GPU

Near GPU

GC6 function

PVT PIR-87

from EC

NV DG PLL_VDD
0.1Ux1
22Ux1 33ohm(ESR0.05)x1

NV DG SP_PLLVDD,VID_PLLVDD
0.1Ux2 Under GPU
4.7Ux1,22Ux1
180ohm(ESR0.2)x1

Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

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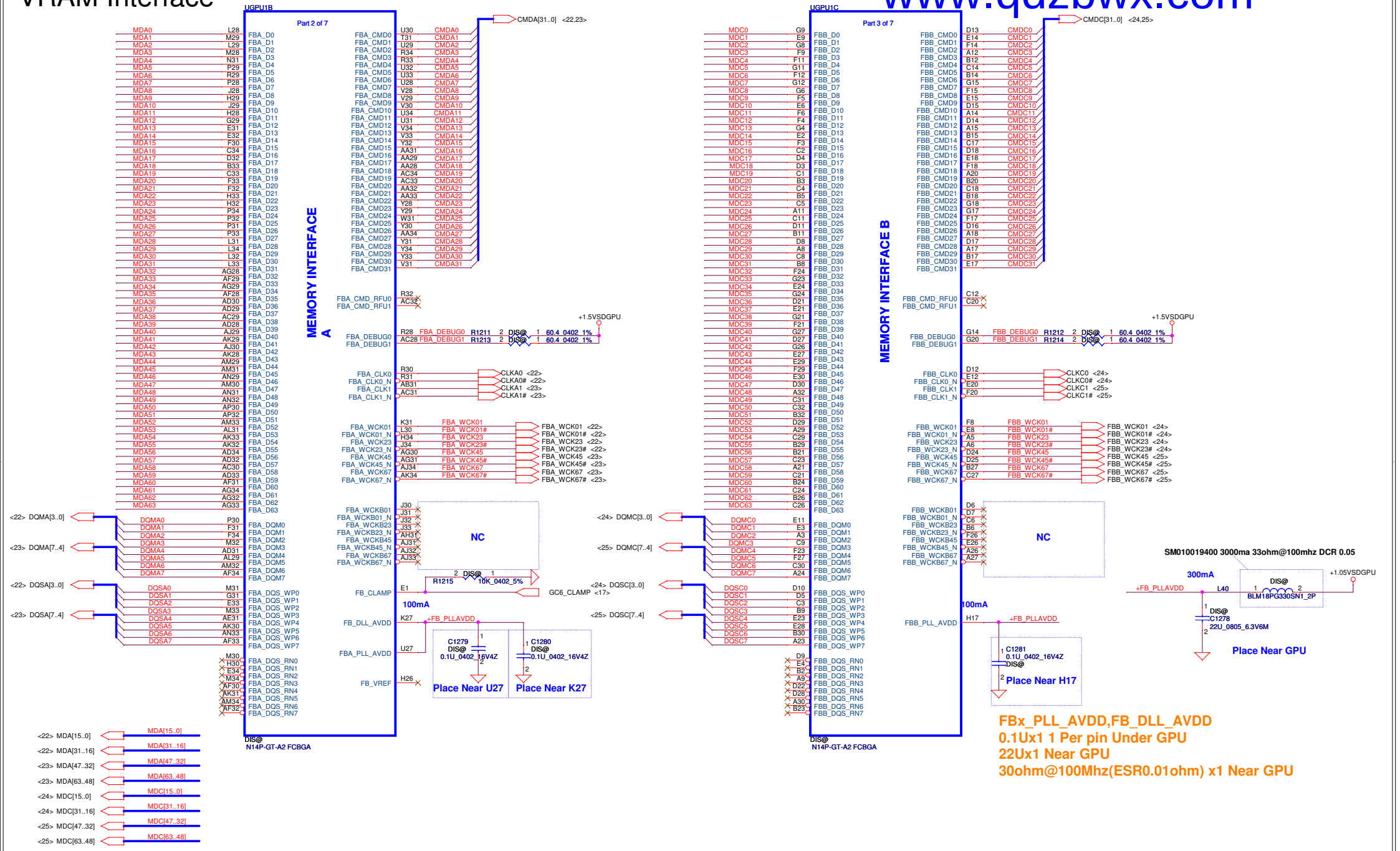
Compal Electronics, Inc.

Title: N14P PEG 1/9

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

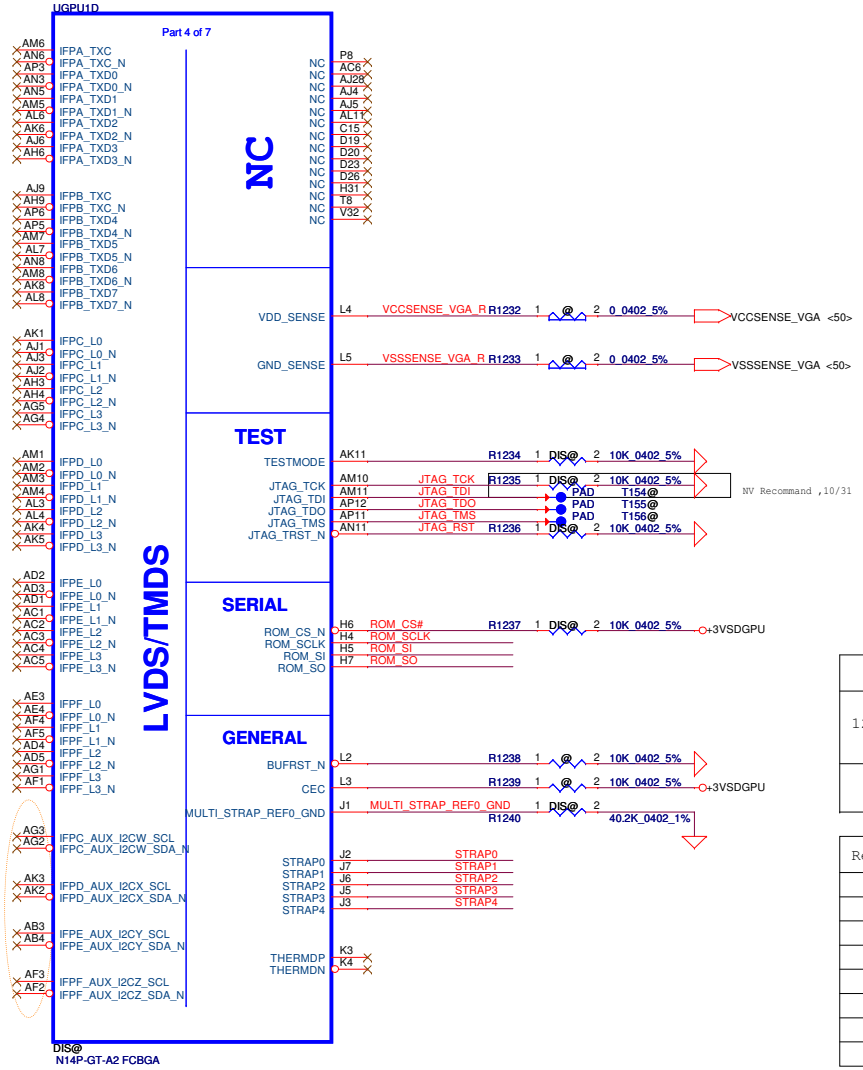
Date: Tuesday, August 27, 2013 | Sheet 17 of 57

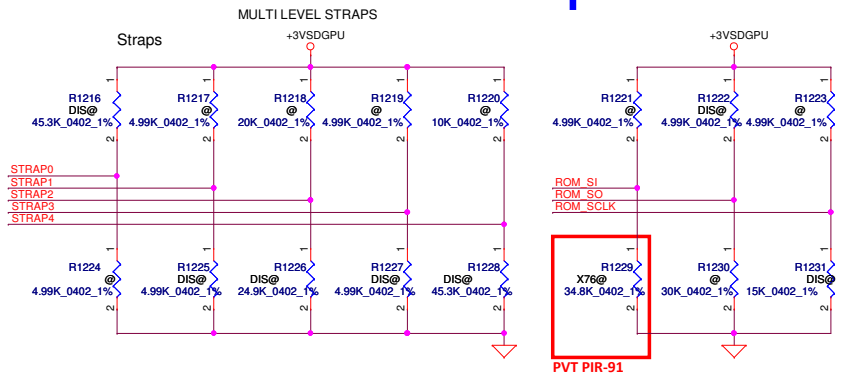
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.			
Title: N14P VRAM 2/9			
Size: Custom	Document Number: V5MM2 M/B LA-A021P Schematic		Rev: 1.0
Date: Tuesday, August 27, 2013		Sheet 18 of 57	





VRAM BOM Config **VRAM P/N**

64Mx32x4 **HYN** **64*32** **2000M** SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!)

64Mx32x4 **HYN** **64*32** **2000M** SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!)

GDDR5	Vendor	Strap	ROM_SI
128M x 16	Hynix(M)	Ox4	24.9K
	Samsung	Ox5	30.1K
	Hynix(M)	Ox6	34.8K

Resistor Values	Pull-up to +3V	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SOR[3:0]
STRAP4	PEG_SPEED_CHANGE_GEN3, PEX_MAX_SPEED,DP_PLLVDD33V
ROM_SCLK	PCI_DEV[4],SUB_VENDOR, PCI_DEV[5],PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3:0]
ROM_SO	FB_BAR_SIZE[1:0],SMB_ ALT_ADDR, VGA_DEVICE

For N14P-GT-A1(ES2) A2(QS) strap table **Decive ID : 0x0FE4**

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GT	900 MHZ	128M*16	Hynix	R PU 45K	R PD 5K	R PD 25K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PD 15K
			Samsung						R PD 30K		

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *N14P LVDS 3/9*

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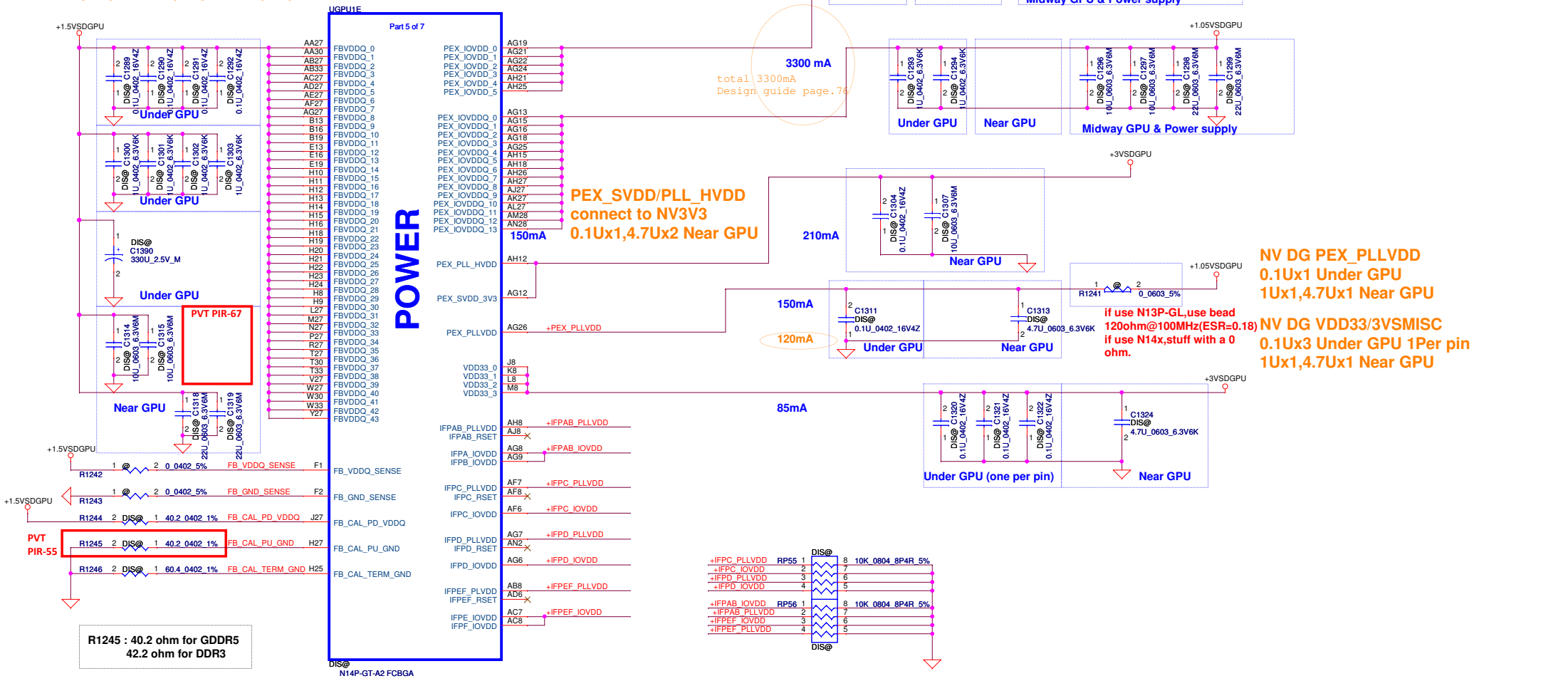
NV 14x DG FBVDDQ(DDR3) GB4-128
0.1Ux4,1Ux4,4.7Ux4 Under GPU
10Ux2,22Ux2 Near GPU

NV DG FBVDDQ(GDDR5)
0.1Ux6(3@),1Ux6(3@),Under GPU
4.7Ux6(3@) ,10Ux4(2@),22Ux4(2@) Near GPU

N13P-GS 10.44A
N13P-GT 10.51A

NV DG PEX_IOVVD/Q combined
1Ux4 Under GPU
4.7Ux2 Near GPU
10Ux4,22Ux4 Midway GPU & Power supply



NV DG PEX_PLLVDD
0.1Ux1 Under GPU
1Ux1,4.7Ux1 Near GPU

NV DG VDD33/3VSMISC
0.1Ux3 Under GPU 1Per pin
1Ux1,4.7Ux1 Near GPU

if use N13P-GL,use bead 120ohm@100MHz(ESR=0.18)
if use N14x,stuff with a 0 ohm.

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Compal Electronics, Inc.

Title: N14P POWER & GND 4/9

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

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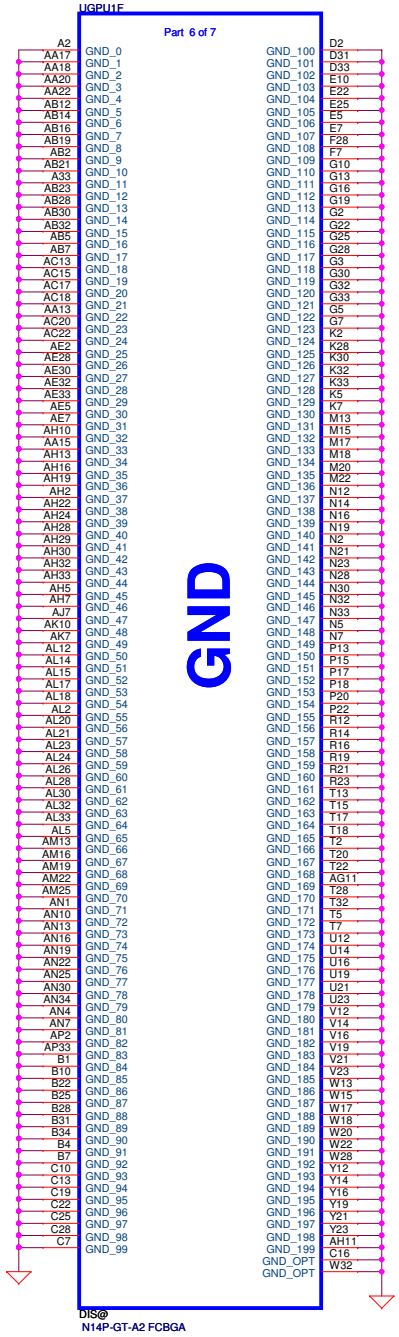

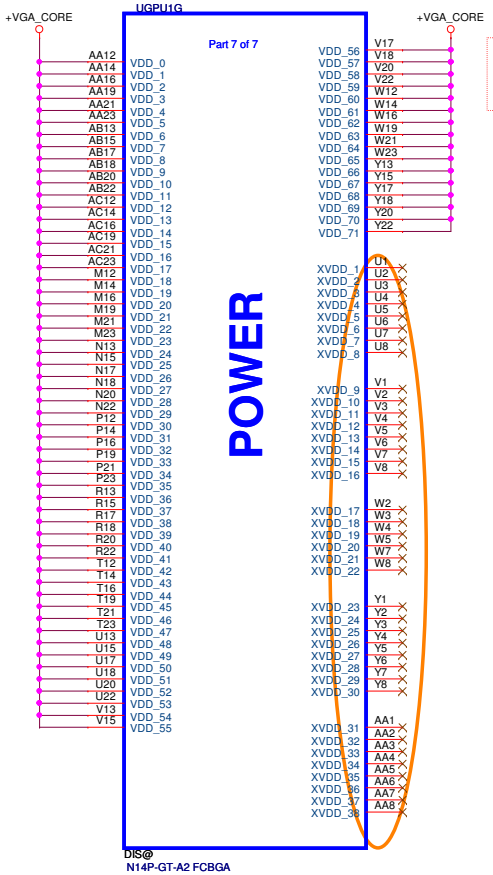

N14P-GT EDP peak 45A

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: N14P POWER & GND 5/9

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Memory Partition A Lower 32 Bit

TOP / M3

GDDR5 Mode H Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

U5 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!
U6 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!
U7 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!
U8 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!

U5 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!
U6 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!
U7 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!
U8 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!

For gDDR5(DG-06246-001_v04)
VREFD=>外接線路可改成不上
VREFC=>外接線路一定要上

PVT PIR-68

Near ball

External VRAM Thermal Sensor

SA00003PU00
S IC W83L771AWG-2 TSSOP 8P SENSOR

建議線路

0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

目前

0.1ux8+1ux8+4.7ux3(@)+10ux2

VRAM BOM Config

X76364BOL01: 1G HYN 128*16 2.5G SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!)

Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: N14P GDDR5 6/9

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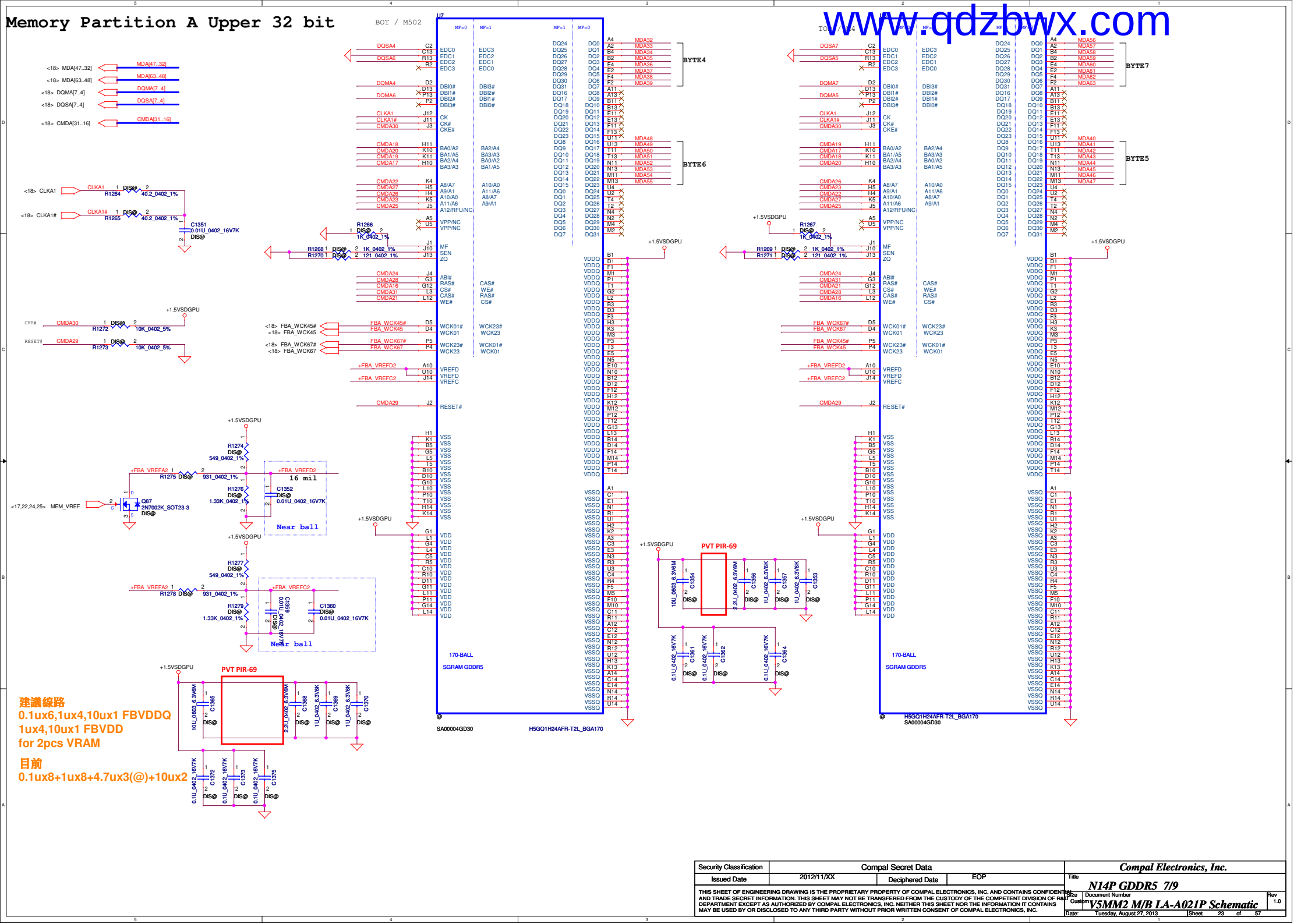
Memory Partition A Upper 32 bit

BOT / M502

TOP / M504

U7



建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

目前
0.1ux8+1ux8+4.7ux3(@)+10ux2

Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.			
Title: N14P GDDR5 7/9			
Size: Custom	Document Number: V5MM2 M/B LA-A021P Schematic		Rev: 1.0
Date: Tuesday, August 27, 2013	Sheet 23 of 57		

Memory Partition C Lower 32 bit

TOP / M1

GDDR5 Mode H Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

U9 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!
U10 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!
U11 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!
U12 HYNMFR@ SA00004GD30 S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!

U9 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!
U10 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!
U11 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!
U12 HYNAFR@ SA00004GD50 S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!

U9 SA00004GD30 170-BALL SGRAM GDDR5 H5GQ1H24AFR-T2L_BGA170
U10 SA00004GD30 170-BALL SGRAM GDDR5 H5GQ1H24AFR-T2L_BGA170

PVT PIR-70

PVT PIR-127 for debug

建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

目前
0.1ux8+1ux8+4.7ux3(@)+10ux2

VRAM BOM Config
X76364BOL01: 1G HYN 128*16 2.5G SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: N14P GDDR5 8/9

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

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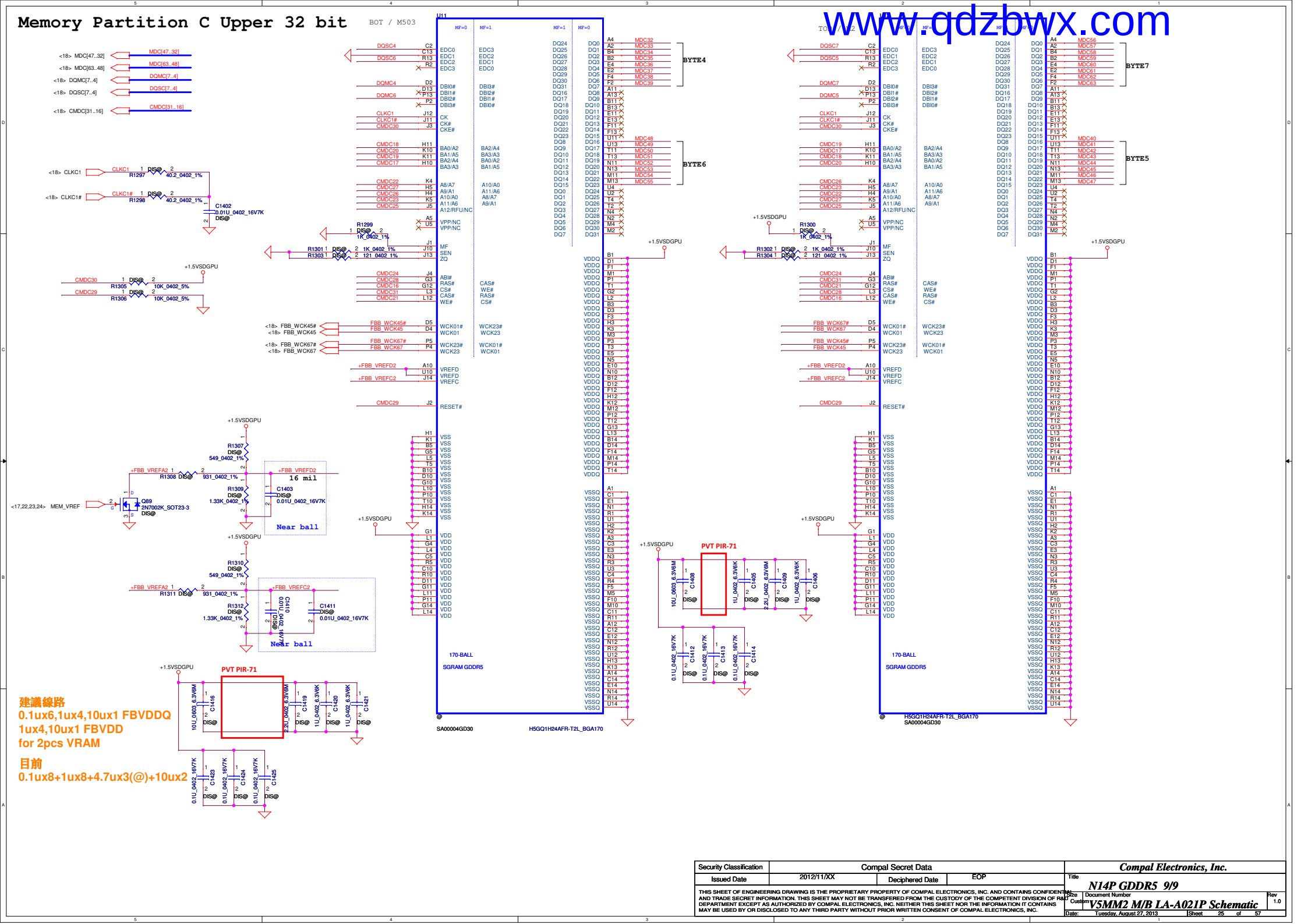
Memory Partition C Upper 32 bit

BOT / M503



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/11/XX	Deciphered Date	EOP

Title	N14P GDDR5 9/9		
Size	Document Number		Rev
Custom	V5MM2 M/B LA-A021P Schematic		1.0
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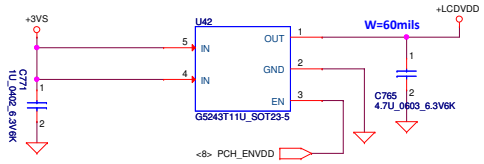
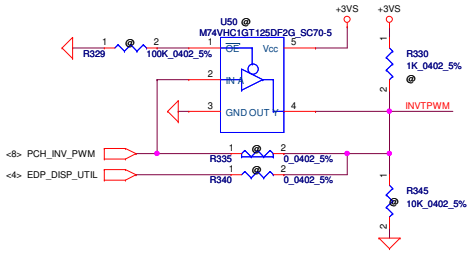
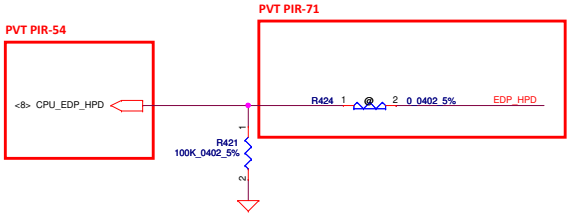
eDP Panel Power Circuit

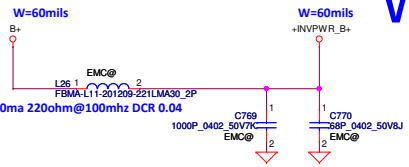


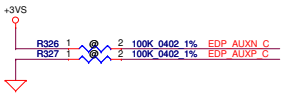
Need to check eDP panel sequence in the future.

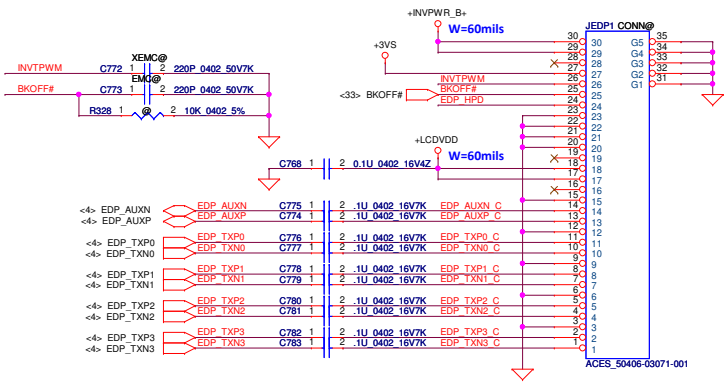


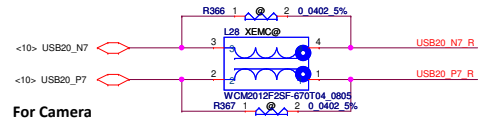
PVT PIR-54 / PVT PIR-71

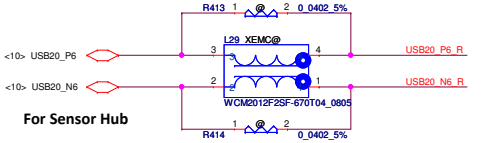


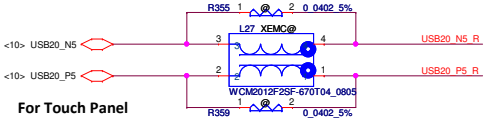


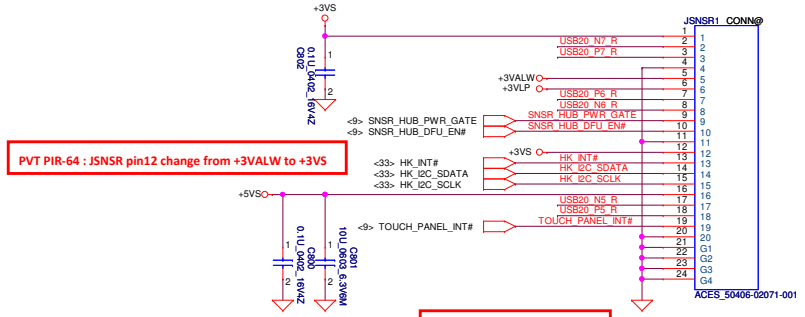




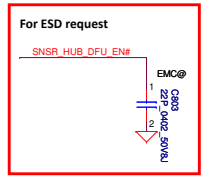








PVT PIR-64 : JSNSR pin12 change from +3VALW to +3VS



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Title: *eDP Connector*

Size	Document Number	Rev
Custom	*V5MM2 M/B LA-A021P Schematic*	1.0

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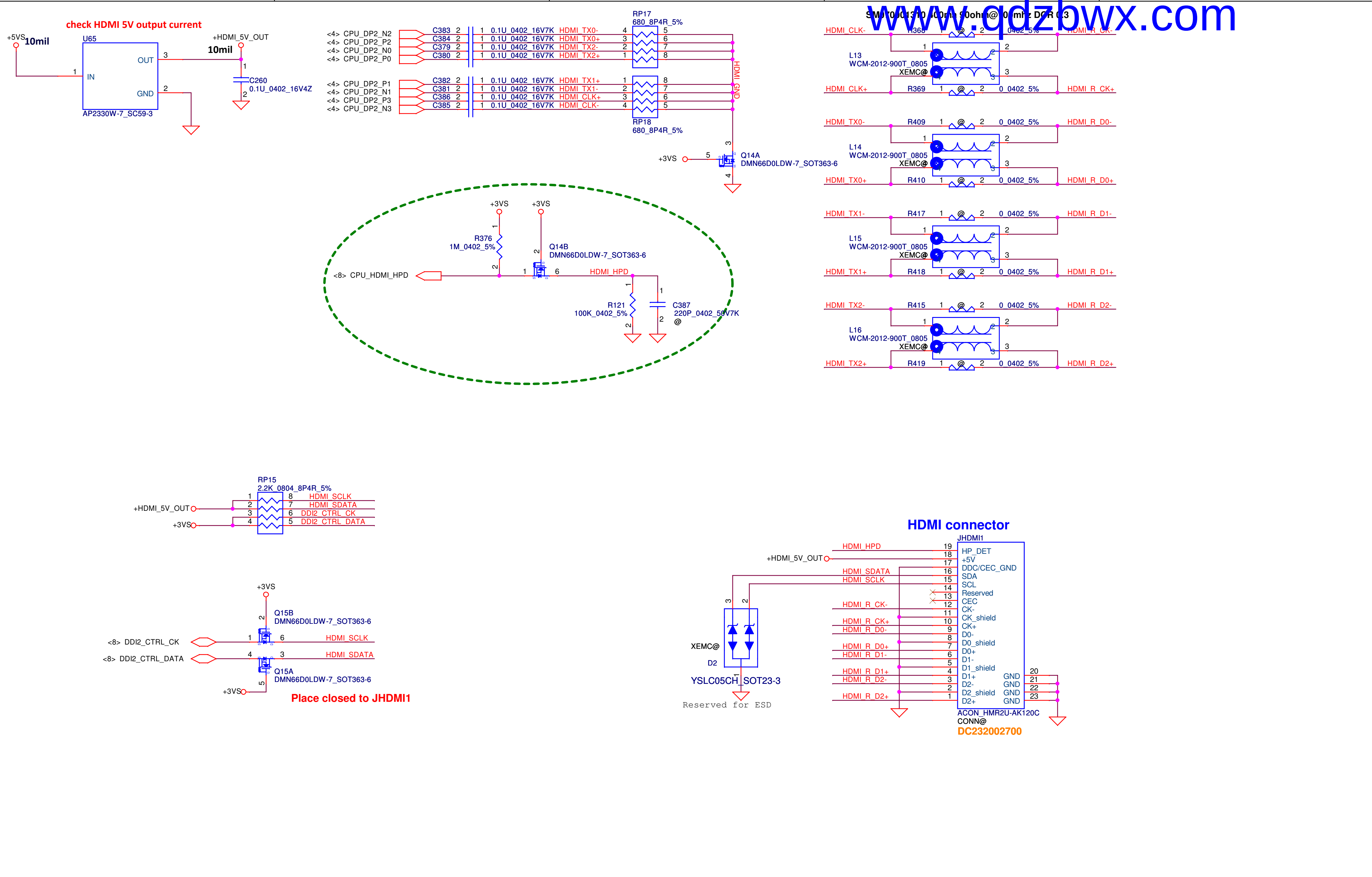
check HDMI 5V output current
+5VS
10mil
U65
AP2330W-7_SC59-3
IN
OUT
GND
+HDMI_5V_OUT
10mil
C260
0.1U_0402_16V4Z
<4> CPU_DP2_N2
<4> CPU_DP2_P2
<4> CPU_DP2_N0
<4> CPU_DP2_P0
<4> CPU_DP2_P1
<4> CPU_DP2_N1
<4> CPU_DP2_P3
<4> CPU_DP2_N3
C383 0.1U_0402_16V7K HDMI_TX0-
C384 0.1U_0402_16V7K HDMI_TX0+
C379 0.1U_0402_16V7K HDMI_TX2-
C380 0.1U_0402_16V7K HDMI_TX2+
C382 0.1U_0402_16V7K HDMI_TX1+
C381 0.1U_0402_16V7K HDMI_TX1-
C386 0.1U_0402_16V7K HDMI_CLK+
C385 0.1U_0402_16V7K HDMI_CLK-
RP17
680_8P4R_5%
RP18
680_8P4R_5%
HDMI_GND
+3VS
Q14A
DMN66D0LDW-7_SOT363-6
SM070001310 400ma 90ohm@100mhz DCR 0.3
HDMI_CLK- R368 0_0402_5% HDMI_R_CK-
L13
WCM-2012-900T_0805
XEMC@
HDMI_CLK+ R369 0_0402_5% HDMI_R_CK+
HDMI_TX0- R409 0_0402_5% HDMI_R_D0-
L14
WCM-2012-900T_0805
XEMC@
HDMI_TX0+ R410 0_0402_5% HDMI_R_D0+
HDMI_TX1- R417 0_0402_5% HDMI_R_D1-
L15
WCM-2012-900T_0805
XEMC@
HDMI_TX1+ R418 0_0402_5% HDMI_R_D1+
HDMI_TX2- R415 0_0402_5% HDMI_R_D2-
L16
WCM-2012-900T_0805
XEMC@
HDMI_TX2+ R419 0_0402_5% HDMI_R_D2+
+3VS
+3VS
R376
1M_0402_5%
Q14B
DMN66D0LDW-7_SOT363-6
<8> CPU_HDMI_HPD
HDMI_HPD
R121
100K_0402_5%
C387
220P_0402_50V7K
@
RP15
2.2K_0804_8P4R_5%
+HDMI_5V_OUT
+3VS
HDMI_SCLK
HDMI_SDATA
DDI2_CTRL_CK
DDI2_CTRL_DATA
+3VS
Q15B
DMN66D0LDW-7_SOT363-6
<8> DDI2_CTRL_CK
<8> DDI2_CTRL_DATA
HDMI_SCLK
HDMI_SDATA
Q15A
DMN66D0LDW-7_SOT363-6
+3VS
Place closed to JHDMI1
HDMI connector
JHDMI1
HDMI_HPD
+HDMI_5V_OUT
HDMI_SDATA
HDMI_SCLK
HDMI_R_CK-
HDMI_R_CK+
HDMI_R_D0-
HDMI_R_D0+
HDMI_R_D1-
HDMI_R_D1+
HDMI_R_D2-
HDMI_R_D2+
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK-
CK_shield
CK+
D0-
D0_shield
D0+
D1-
D1_shield
D1+
D2-
D2_shield
D2+
GND
ACON_HMR2U-AK120C
CONN@
DC232002700
XEMC@
D2
YSLC05CH_SOT23-3
Reserved for ESD

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/11/XX	Deciphered Date	EOP	Title: HDMI Conn

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Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev 1.0

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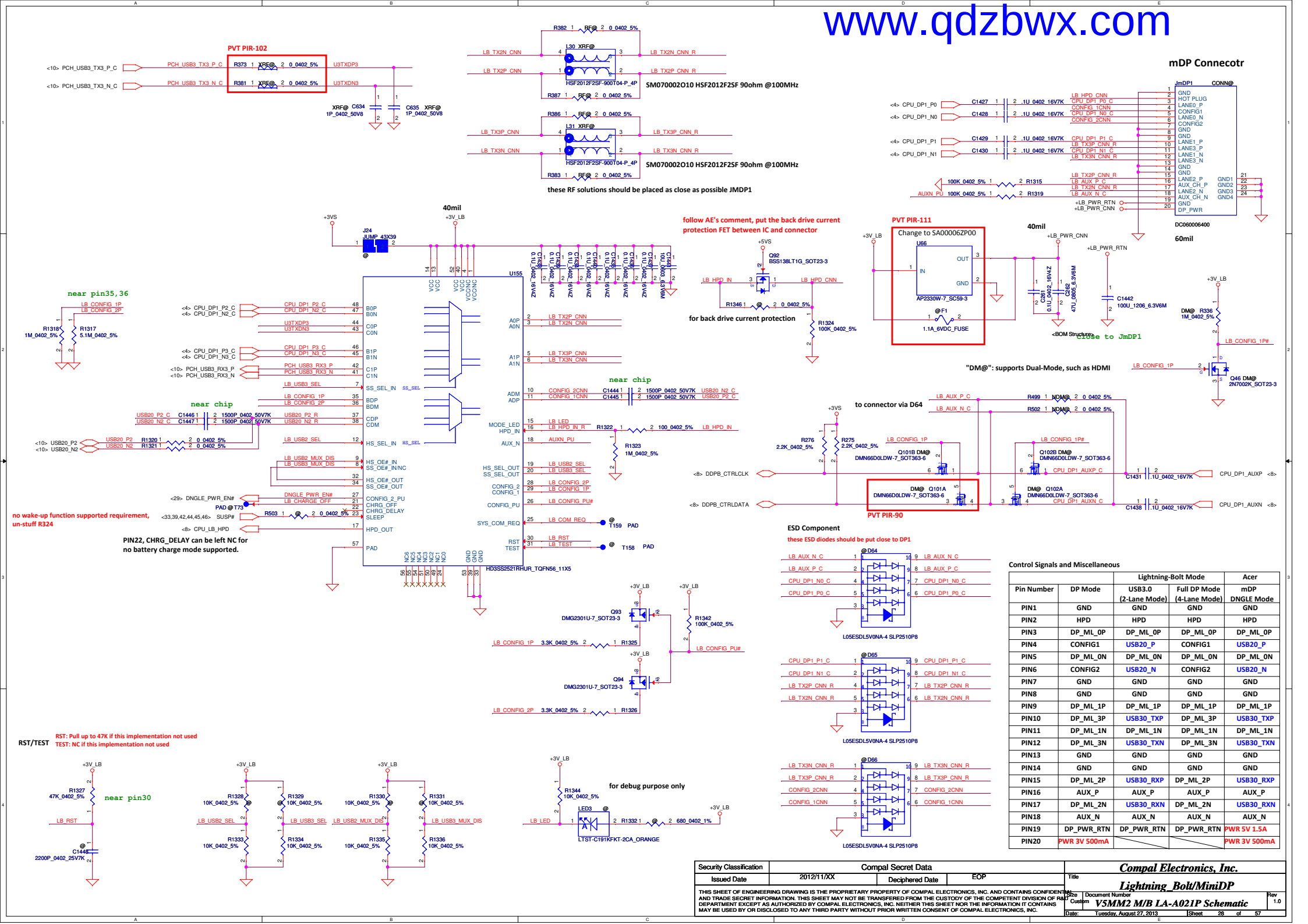

Control Signals and Miscellaneous

		Lightning-Bolt Mode		Acer
Pin Number	DP Mode	USB3.0 (2-Lane Mode)	Full DP Mode (4-Lane Mode)	mDP DNGLE Mode
PIN1	GND	GND	GND	GND
PIN2	HPD	HPD	HPD	HPD
PIN3	DP_ML_0P	DP_ML_0P	DP_ML_0P	DP_ML_0P
PIN4	CONFIG1	USB20_P	CONFIG1	USB20_P
PIN5	DP_ML_0N	DP_ML_0N	DP_ML_0N	DP_ML_0N
PIN6	CONFIG2	USB20_N	CONFIG2	USB20_N
PIN7	GND	GND	GND	GND
PIN8	GND	GND	GND	GND
PIN9	DP_ML_1P	DP_ML_1P	DP_ML_1P	DP_ML_1P
PIN10	DP_ML_3P	USB30_TXP	DP_ML_3P	USB30_TXP
PIN11	DP_ML_1N	DP_ML_1N	DP_ML_1N	DP_ML_1N
PIN12	DP_ML_3N	USB30_TXN	DP_ML_3N	USB30_TXN
PIN13	GND	GND	GND	GND
PIN14	GND	GND	GND	GND
PIN15	DP_ML_2P	USB30_RXP	DP_ML_2P	USB30_RXP
PIN16	AUX_P	AUX_P	AUX_P	AUX_P
PIN17	DP_ML_2N	USB30_RXN	DP_ML_2N	USB30_RXN
PIN18	AUX_N	AUX_N	AUX_N	AUX_N
PIN19	DP_PWR_RTN	DP_PWR_RTN	DP_PWR_RTN	PWR 5V 1.5A
PIN20	PWR 3V 500mA			PWR 3V 500mA

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Compal Electronics, Inc.

Title: Lightning_Bolt/MiniDP

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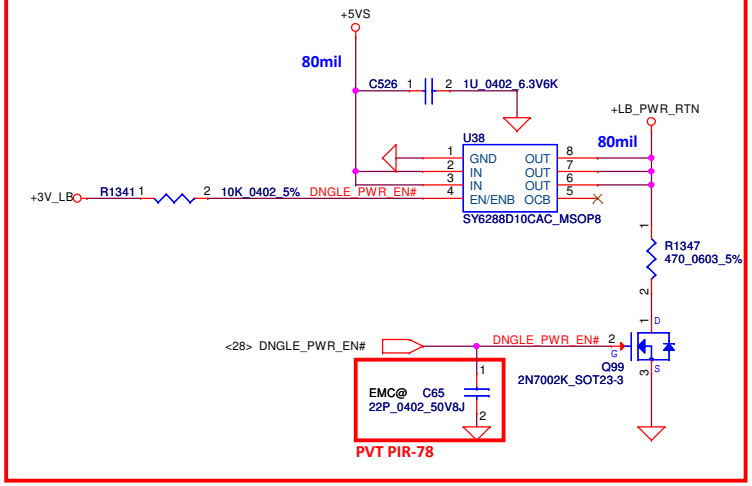
PVT PIR-63

mDP Power Control Circuit for 5V Power Supply



Preliminary Power Output for mDP		
DNGLE_PWR_EN#	LB_PWR_RTN	LB_PWR_CNN
1	GND	3.3V
0	5V	3.3V

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Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: mDP Power

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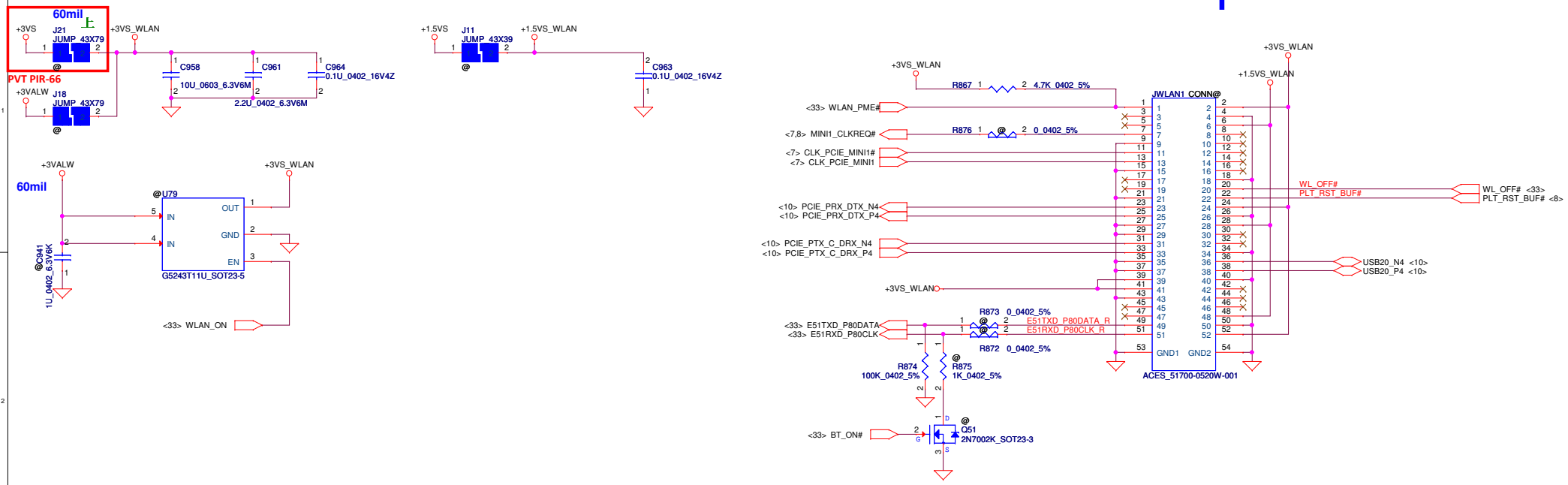
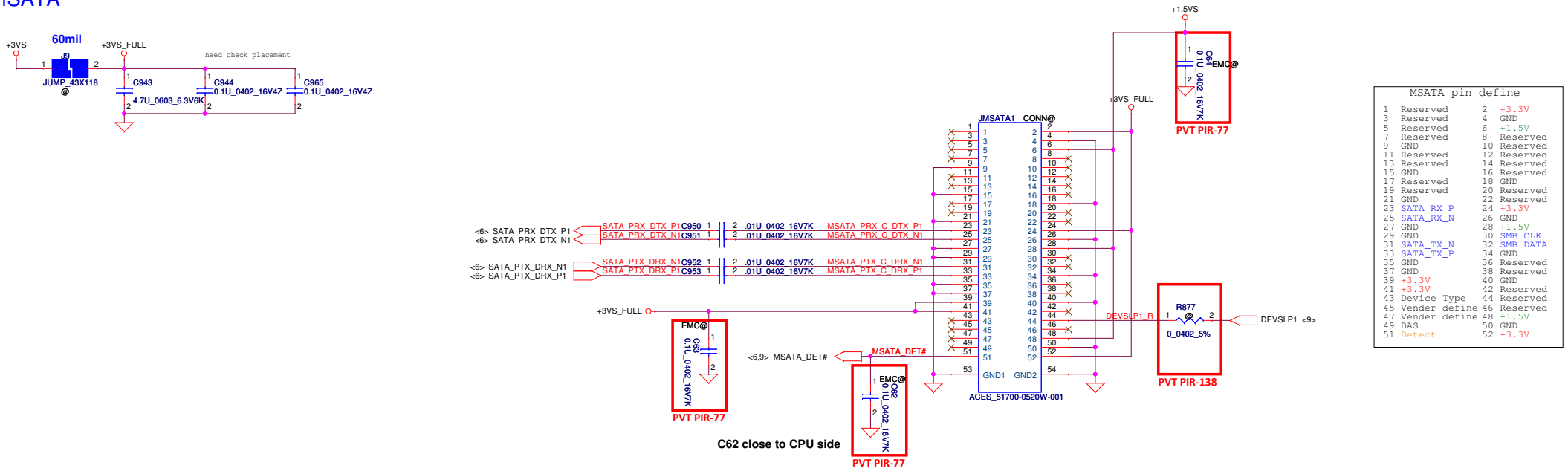
Wireless LAN



mSATA



MSATA pin define

1	Reserved	2	+3.3V
3	Reserved	4	GND
5	Reserved	6	+1.5V
7	Reserved	8	Reserved
9	GND	10	Reserved
11	Reserved	12	Reserved
13	Reserved	14	Reserved
15	GND	16	Reserved
17	Reserved	18	GND
19	Reserved	20	Reserved
21	GND	22	Reserved
23	SATA_RX_P	24	+3.3V
25	SATA_RX_N	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	SATA_TX_N	32	SMB_DATA
33	SATA_TX_P	34	GND
35	GND	36	Reserved
37	GND	38	Reserved
39	+3.3V	40	GND
41	+3.3V	42	Reserved
43	Device Type	44	Reserved
45	Vender define	46	Reserved
47	Vender define	48	+1.5V
49	DAS	50	GND
51	Detect	52	+3.3V

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Compal Electronics, Inc.

Title: MINI CARD/mSATA Connector

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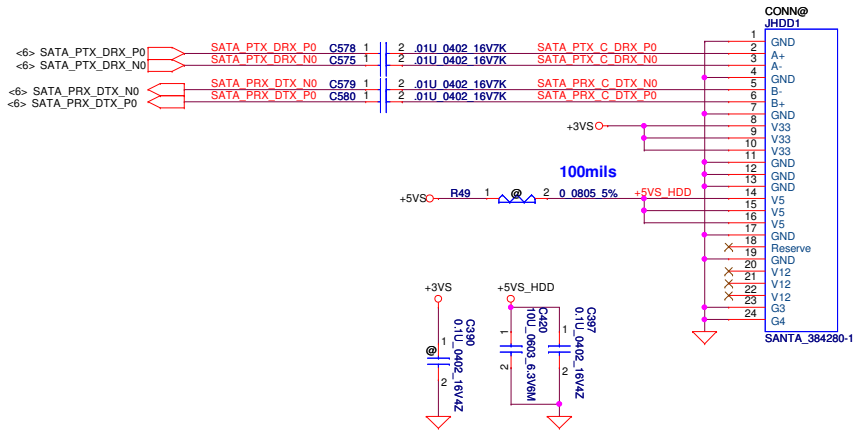
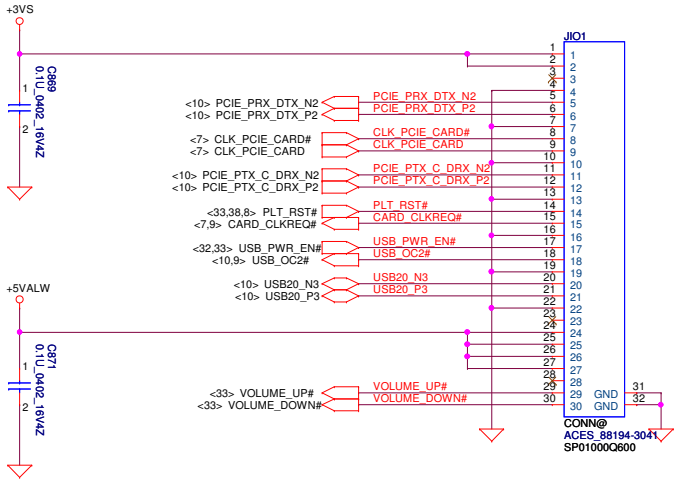
SATA HDD Connector(DIP Type)



IO/B Connector



LAN/B Connector
(Place near JPWR1)

PVT PIR-97

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: HDD/ODD/Debug Board

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

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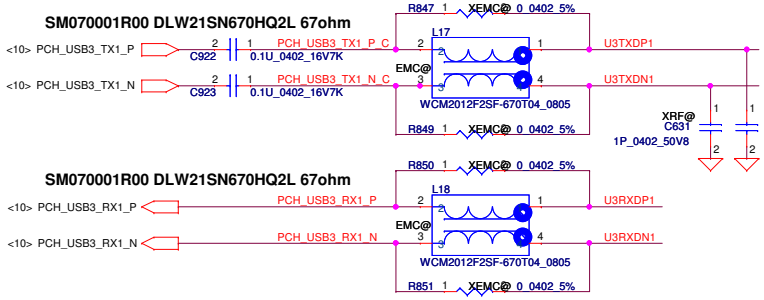
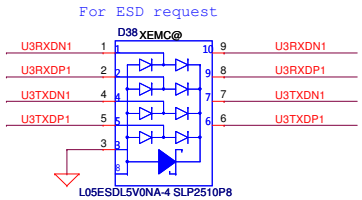
SM070001R00 DLW21SN670HQ2L 67ohm



SM070001R00 DLW21SN670HQ2L 67ohm

For ESD request

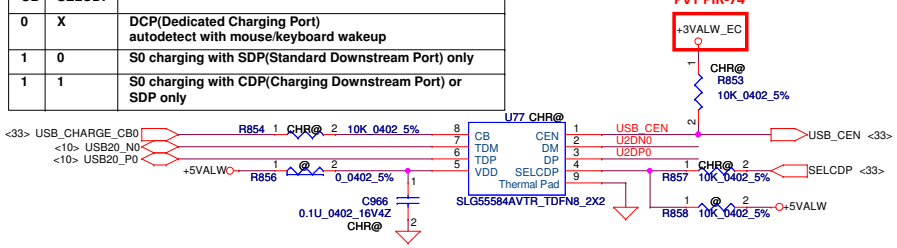


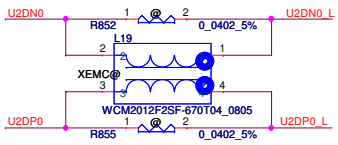
Change to SA00003TV00 on DVT only

USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

PVT PIR-74



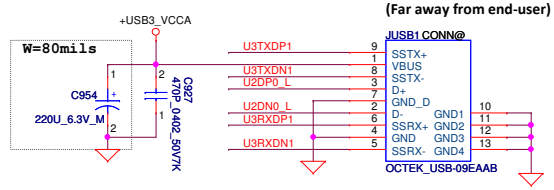


SM070000S80 WCM2012F2SF-670T04 67ohm

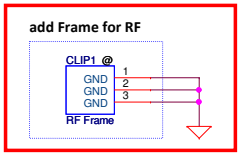
Change PCB footprint to J-L_TNBNRAC70003009_9P-T

USB 3.0 External Connector (Far away from end-user)

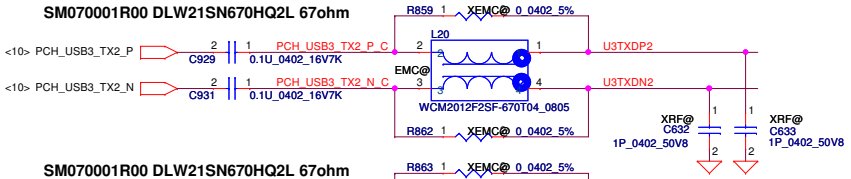
SF000002Y00
220U 6.3V OSCON
ESR 17mohm@100Khz



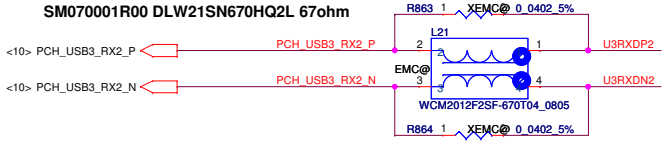
PVT PIR-60



SM070001R00 DLW21SN670HQ2L 67ohm

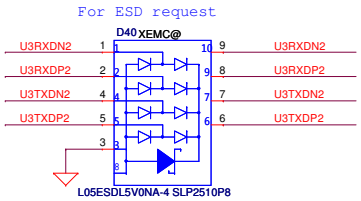


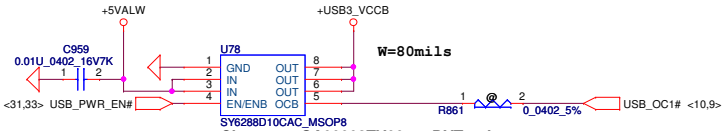
SM070001R00 DLW21SN670HQ2L 67ohm



L20,L21 change to SM070001R00 for EMI request

For ESD request



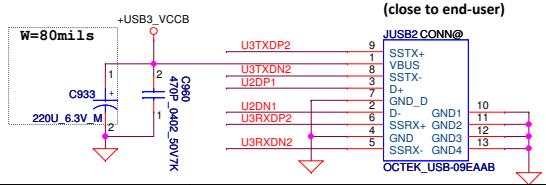


Change to SA00003TV00 on DVT only

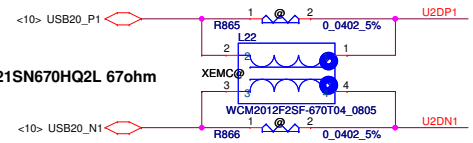
Change PCB footprint to J-L_TNBNRAC70003009_9P-T

USB 3.0 Exteranl Connector (close to end-user)

SF000002Y00
220U 6.3V OSCON
ESR 17mohm@100Khz



SM070001R00 DLW21SN670HQ2L 67ohm



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Title: *USB3.0 External Ports*

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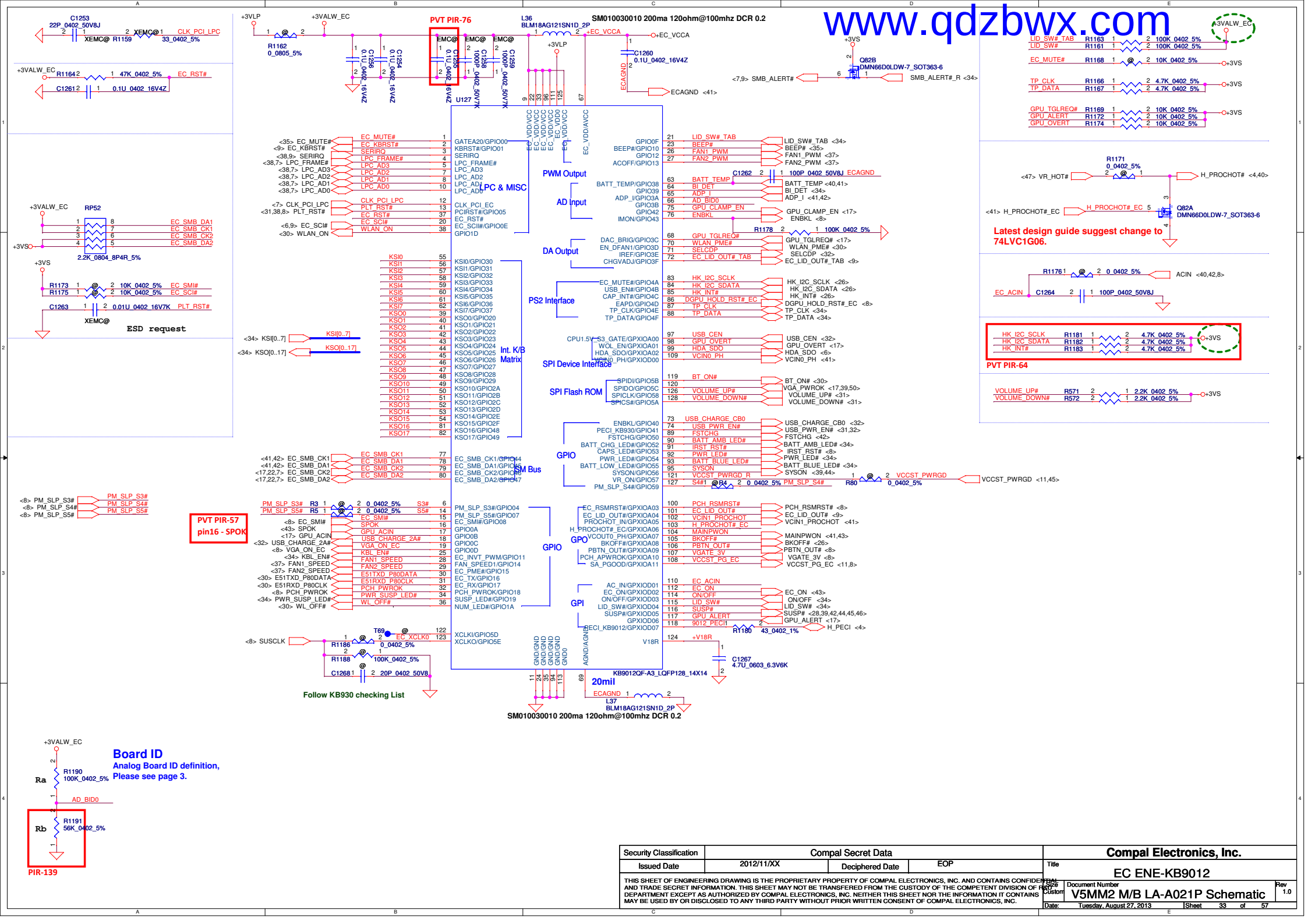

Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

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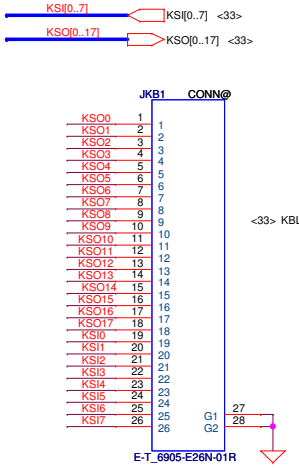
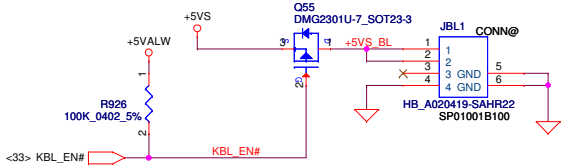
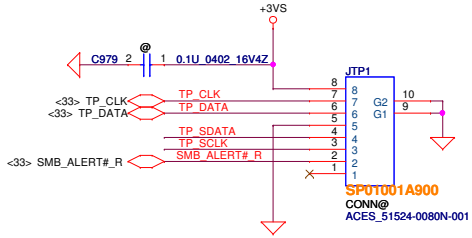
KB Conn.



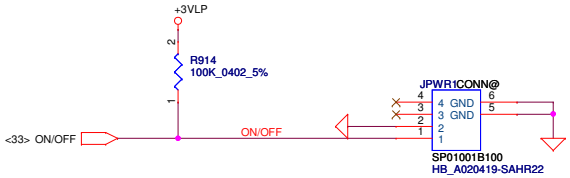
KB backlight Conn.



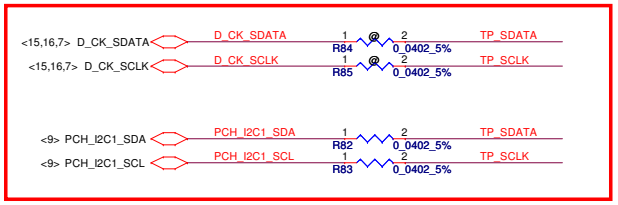
TP Conn.

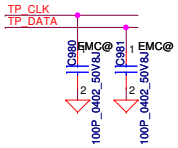


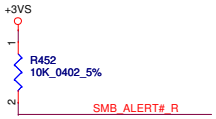
ON/OFF BTN

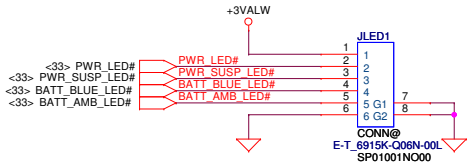


PVT PIR-89







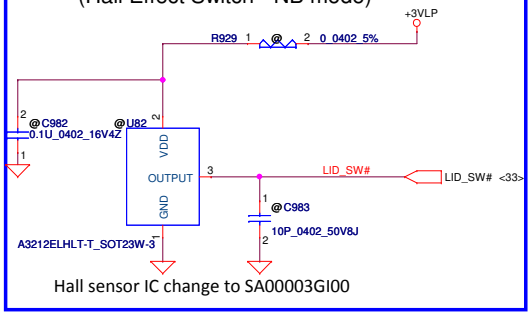


Lid Switch solution	
Solution-1	EVT , DVT , PVT-1
Solution-2	PVT-2

Lid switch power source need same as EC power

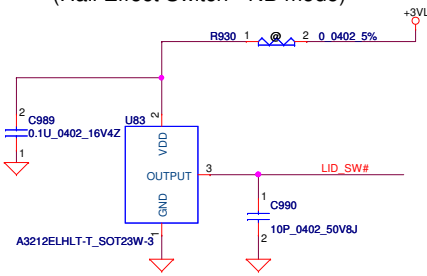
Lid Switch Solution-1

(Hall Effect Switch - NB mode)

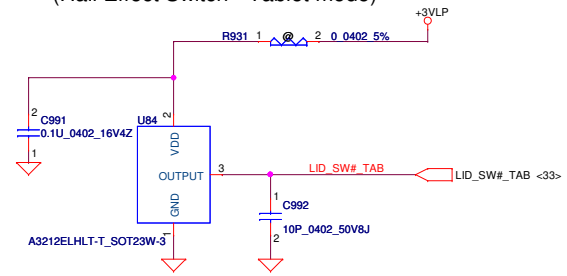


Lid Switch Solution-2

(Hall Effect Switch - NB mode)

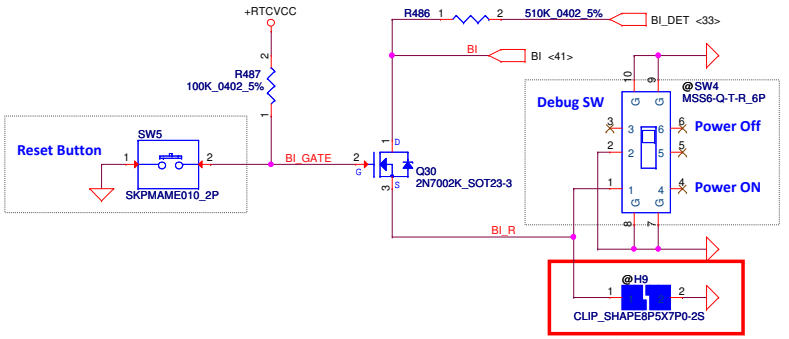


(Hall Effect Switch - Tablet mode)



Reset Button and Debug Switch for Polymer Battery

Debug switch will be removed after MP.



PVT PIR-59,95

PVT PIR-137 for 2nd BI_GATE

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Title: User Interface

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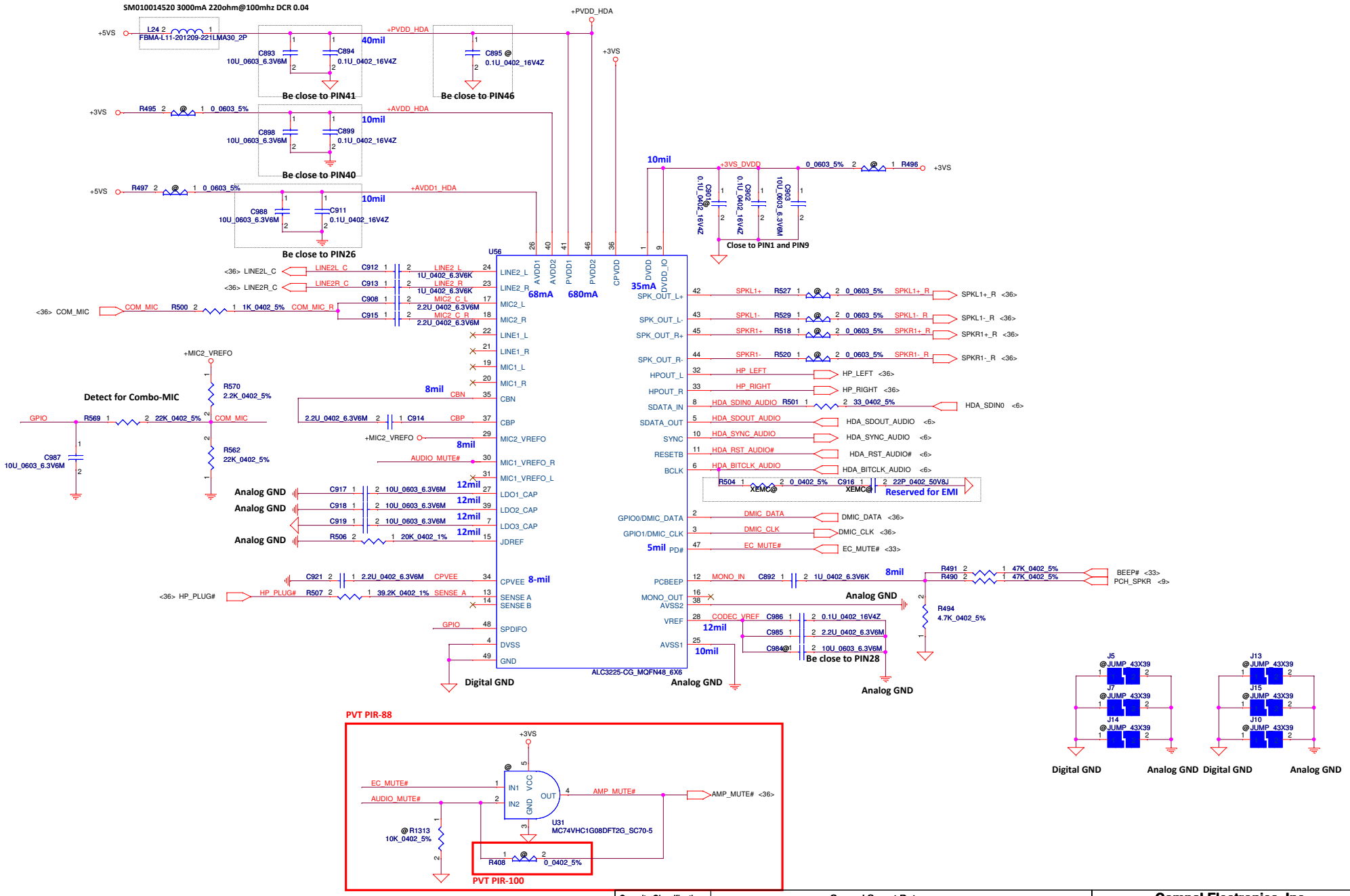
HD Audio Codec- ALC3225 with Embedded Speaker Amplifier



Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title	HD Audio Codec ALC3225X + ALC1001
Size / Custom	Document Number: V5MM2 M/B LA-A021P Schematic
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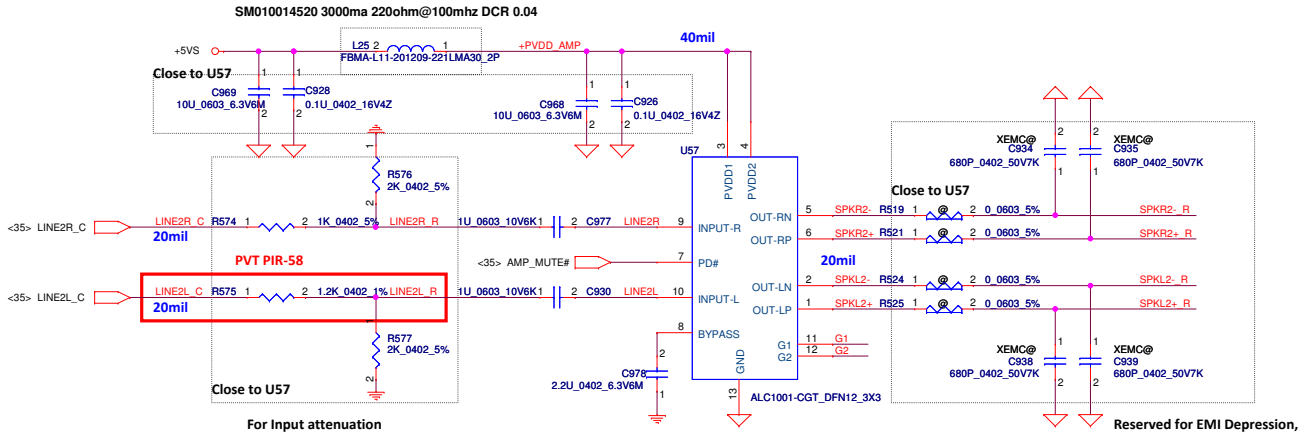
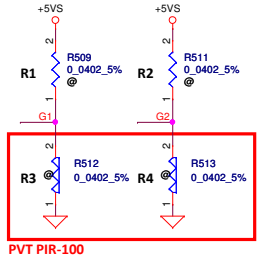
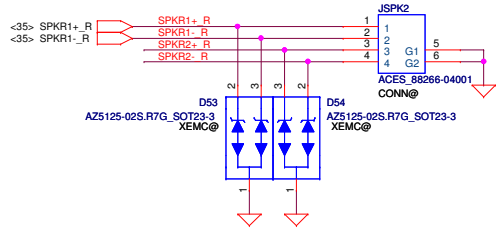


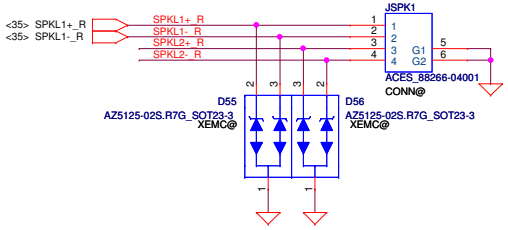
R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



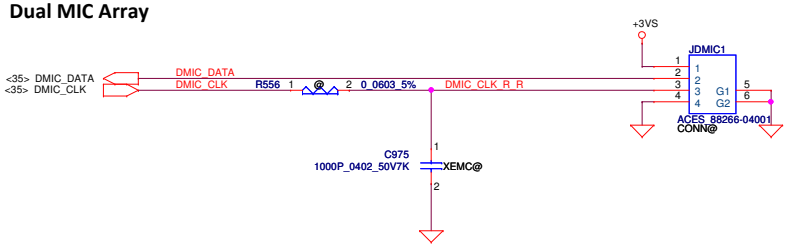
Speaker Connector (Right)



Speaker Connector (Left)

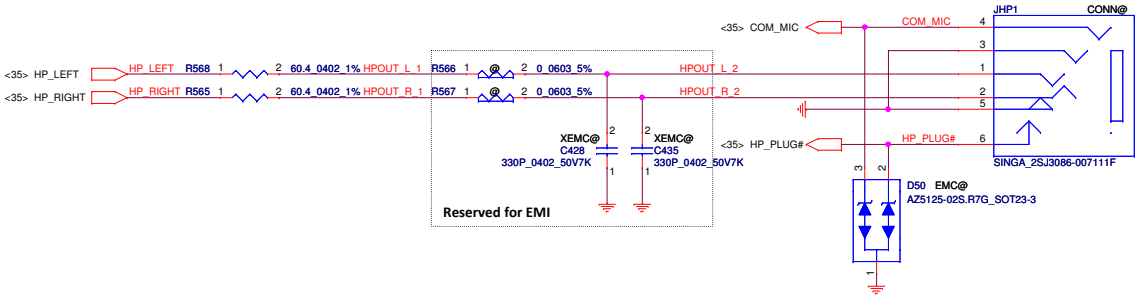


Dual MIC Array



Headphone Out/Mic Combo

JACK TYPE is the same as MA51



Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: Amplifier & I/O Ports

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

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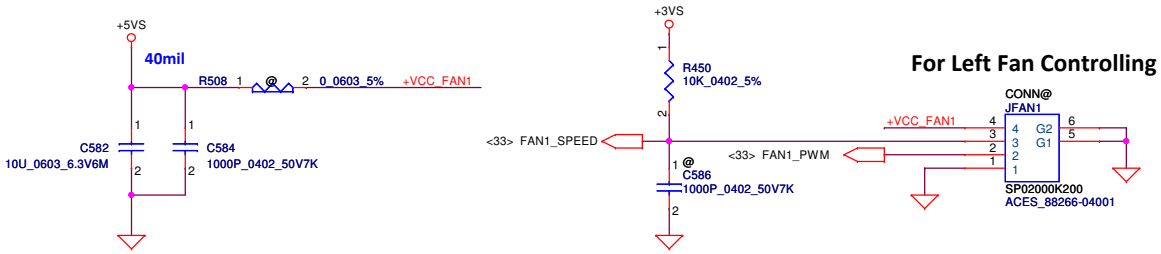
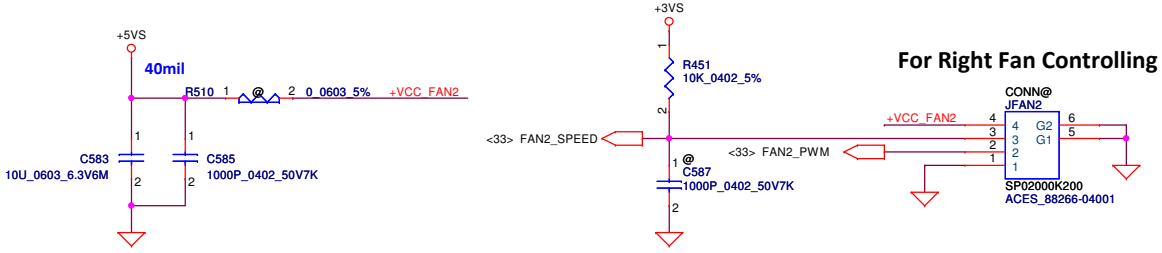
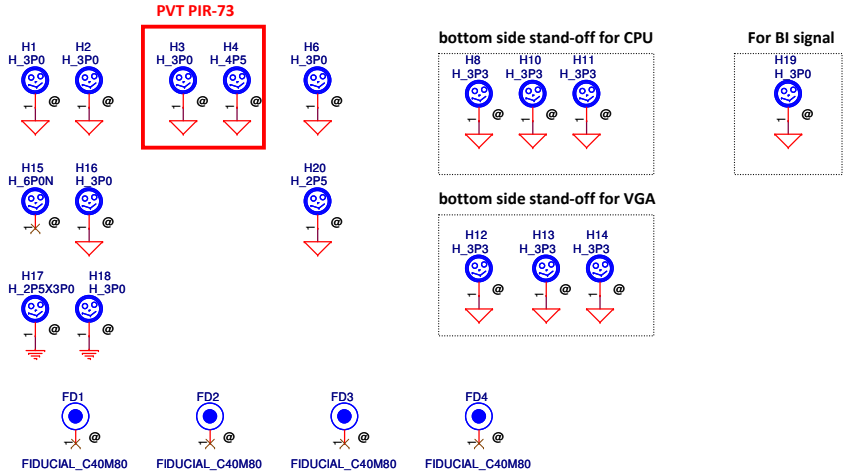






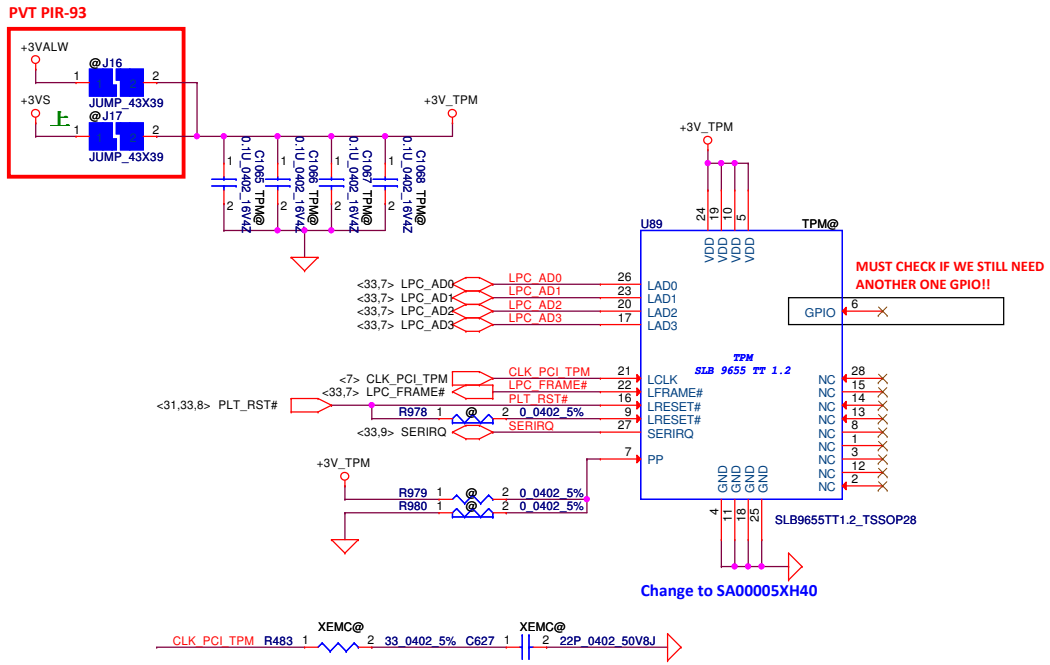
Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

Date: Tuesday, August 27, 2013 | Sheet 37 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

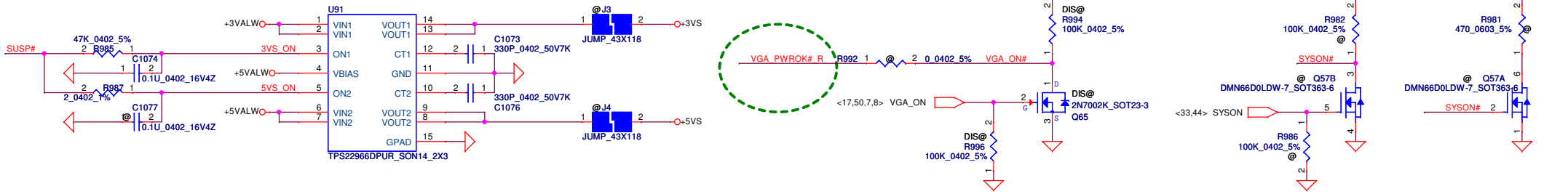
Compal Electronics, Inc.

Title: MINI CARD/mSATA Connector

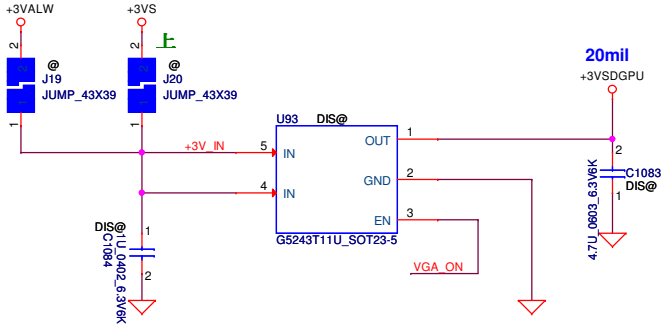
Size: Custom | Document Number: V5MM2 M/B LA-A021P Schematic | Rev: 1.0

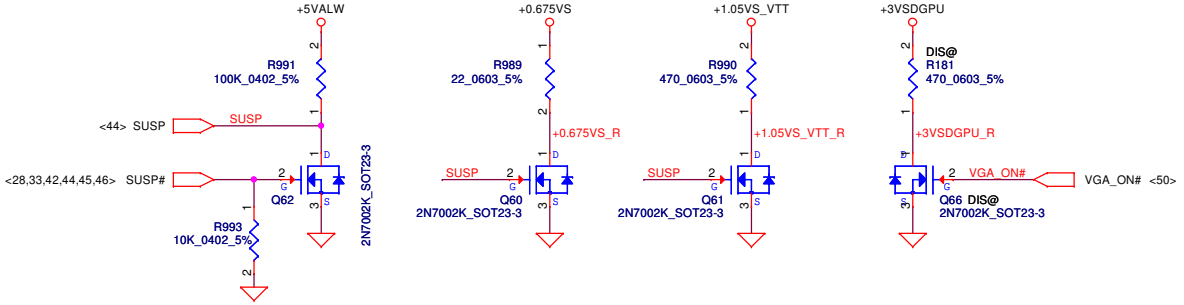
Date: Tuesday, August 27, 2013 | Sheet 38 of 57

Use Dual Load Switch for +3VS/+5VS Power Supply

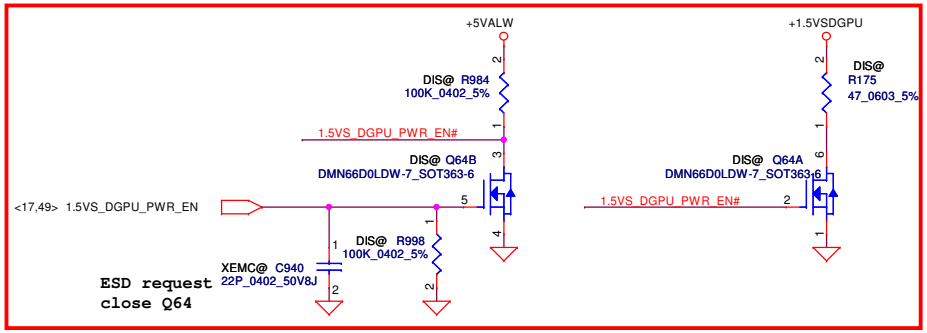


+3V source to +3VSDGPU for GPU

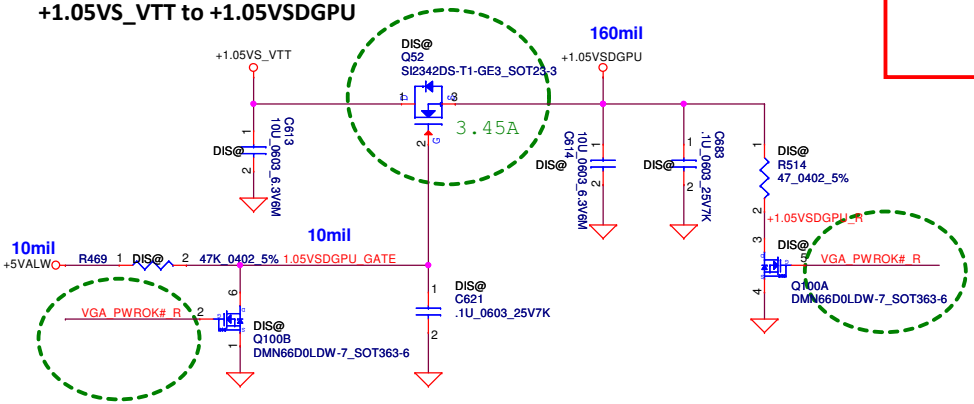


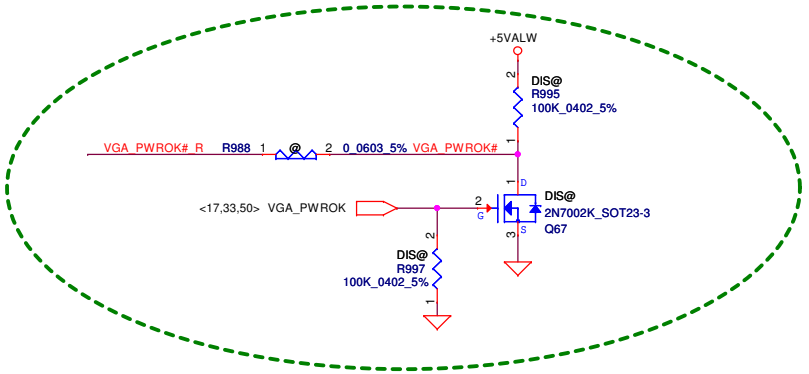


PVT PIR-56



+1.05VS_VTT to +1.05VSDGPU





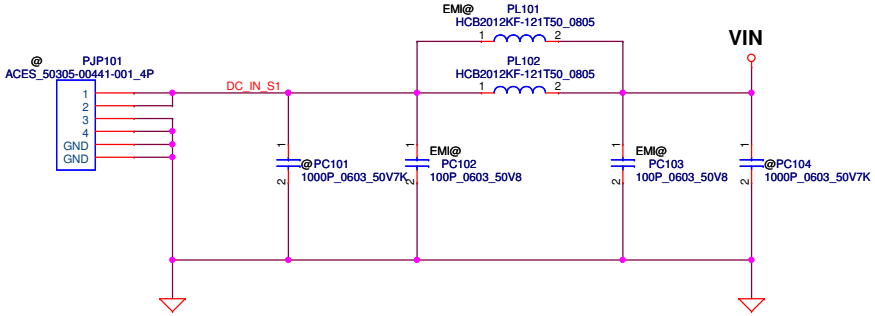
Security Classification	Compal Secret Data		
Issued Date	2012/11/XX	Deciphered Date	EOP

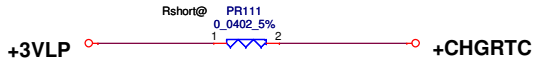
Compal Electronics, Inc.

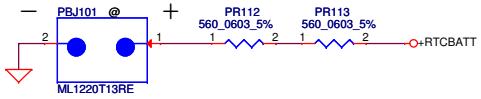
Title: DC Interface

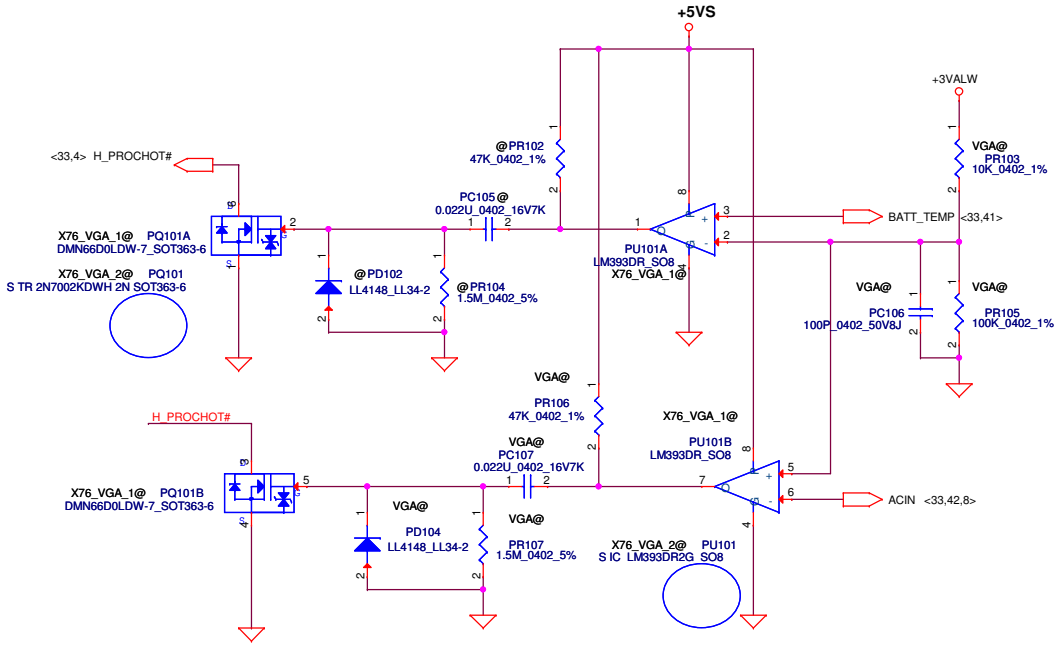
Size	Document Number	Rev
Custom	V5MM2 M/B LA-A021P Schematic	1.0

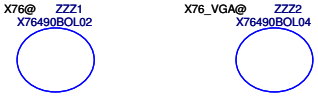
Date: Tuesday, August 27, 2013 Sheet 39 of 57











UMA Only :ZZZ1

DIS: ZZZ2

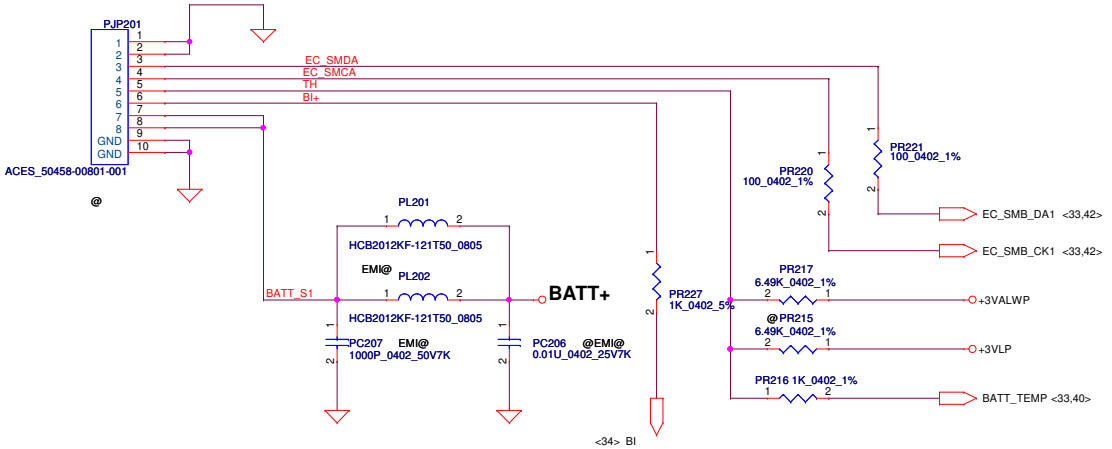
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

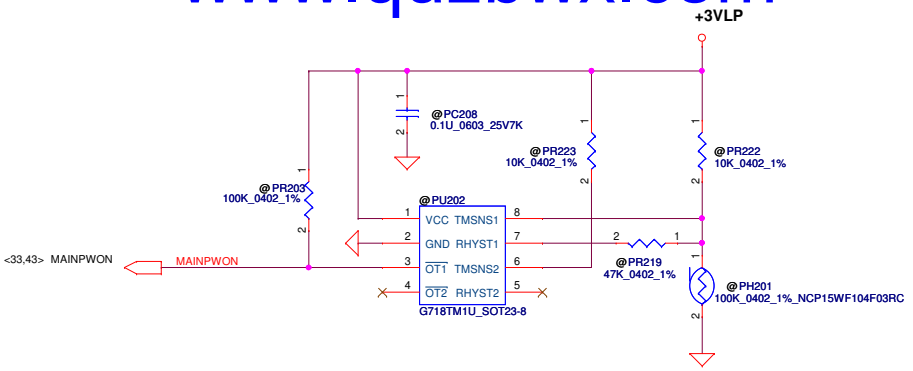
Compal Electronics, Inc.

Title: DCIN

Size: Custom | Document Number: V5MM2_SB | Rev: 1.0

Date: Tuesday, August 27, 2013 | Sheet 40 of 57



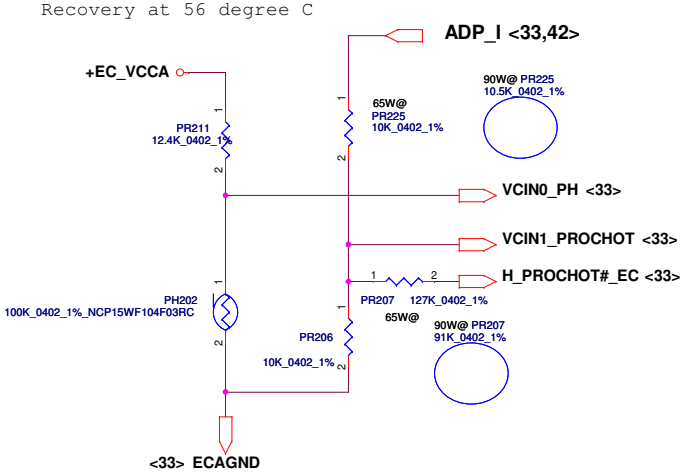


VCIN1 Recovery 85% chang to 100% _2013/06/27

VCIN0	For KB9012 OTP
92℃	1.2V, Active
56℃	2.255V, Recovery

VCIN1 For KB9012 sense 10mΩ	Active	Recovery
65W	85W,0.42V	65W,0.42V
90W	117W,0.56V	90W,0.56V
120W		

PH202 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	BATTERY CONN / OTP
Size: Custom	Document Number: V5MM2_SB
Rev	1.0
Date: Tuesday, August 27, 2013	Sheet 41 of 57

Protection for reverse input

X76_1@ PQ301 2N7002KW_SOT323-3 Vgs = 20V Vds = 60V Id = 250mA

X76_2@ PQ301 L2N7002WT1G 1N SC-70-3

PR302 1M_0402_5%

PR303 3M_0402_5%

Rds(on) typ = 35mohm max Vgs = 20V Vds = 30V ID = 7.7A (Ta=70C)

max Power loss 0.22W for 90W;0.12W for 65W system CSR rating: 1W VACP-VACN spec < 80.64mV

VIN

AON6414AL_DFN8-5 X76_1@ PQ302

P1 P2

PC302 2200P_0402_50V7K @EMI@

PR305 0_0402_5%

PC303 0.1U_0402_25V6

BQ24725A_ACDRV_1

X76_1@PQ303 AO4466L_SO8

X76_2@ PQ303 FDS8884 1N SO8

PR304 0.01_1206_1%

B+

PL301 EMI@ 1UH_NRS4018T1R0NDGJ_3.2A_30% Isat: 4A DCR: 27mohm

CHG_B+

PC304 10U_0805_25V6K

PC305 10U_0805_25V6K

PC306 2200P_0402_50V7K @EMI@

PC307 0.1U_0402_25V6 @EMI@

X76_2@ PQ304 FDS8884 1N SO8

Rds(on) typ = 35mohm max Vgs = 20V Vds = 30V ID = 7.7A (Ta=70C)

X76_1@ PQ304 AO4466L_SO8

PC308 0.01U_0402_50V7K

BQ24725A_BATDRV

PR306 4.12K_0603_1%

BQ24725A_BATDRV_1

Need check the SOA for inrush

X76_2@ PQ302 TPCA8065-H 1N PPAK56-8

PC309 0.1U_0402_25V6

PC310 0.1U_0402_25V6

PC311 0.1U_0402_25V6

VIN

VF = 0.5V

PD301 BAS40CW_SOT323-3

PC312 0.047U_0402_25V7K

PR301 10_1206_1%

PR307 2.2_0603_5%

VF = 0.37V

PD302 RB751V-40_SOD323-2

X76_2@ PQ305 MDV1528URH 1N PDFN33-8

PQ305 SIS412DN-T1-GE3_POWERPAK8-5

X76_1@

X76_2@ PL302 10UH +-20% PCMB063T-100MS 4A

Support max charge 4A Power loss: 0.32W CSR rating: 1W VSRP-VSRN spec < 81.28mV

BATT+

DH_CHG

PR325 0_0603_5%

DH_CHG-1

X76_1@ PL302 10UH_FDSD0630-H-100M-P3_3.8A_20%

BQ24725A_LX

CHG

7X7X3 Isat: 5.1A DCR: 74mohm

PR310 0.01_1206_1%

PR308 4.12K_0603_1%

PR309 4.12K_0603_1%

PC301 1U_0603_25V6K

PC313 1U_0603_25V6K

PU301

BQ24735RGRR_QFN20_3P5X3P5

PAD VCC PHASE HIDRV BTST REGN

ACN ACP CMSRC ACDRV ACOK

LODRV GND SRP SRN BATDRV

ACDET IOUT SDA SCL ILIM

PQ306 SIS412DN-T1-GE3_POWERPAK8-5

X76_1@

X76_2@ PQ306 MDV1528URH 1N PDFN33-8

PR311 4.7_1206_5%

@EMI@

PC320 680P_0402_50V7K @EMI@

CSOP1 CSON1

PC318 0.1U_0402_25V6

PC319 0.1U_0402_25V6

PC314 10U_0805_25V6K

PC315 10U_0805_25V6K

PC316 2200P_0402_50V7K @EMI@

BQ24725A_CMSRC

BQ24725A_ACDRV

PR312 10_0603_1%

PR313 6.8_0603_1%

PC321 0.1U_0603_16V7K

+3VLP

PR314 100K_0402_1%

BQ24725A_ACOK

<33,40,8> ACIN

BQ24725A_BATDRV

BQ24725A_ILIM

PR316 316K_0402_1%

PR317 100K_0402_1%

PC322 0.01U_0402_25V7K

PR318 499K_0402_1%

EC_SMB_CK1 <33,41>

EC_SMB_DA1 <33,41>

ADP_I <33,41>

PC323 0.22U_0402_16V7K

PR322 78.7K_0402_1%

PC324 100P_0402_50V8J

Rshort@ PR323 0_0402_5%

PC325 @ 100P_0402_50V8J

Close EC chip

Vin Dectector

	Min.	Typ	Max.
L-->H	17.28V	17.62V	17.96V
H-->L	16.91V	17.21V	17.53V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

For 4S per cell 4.35V battery

ACDET

@ PR319 2M_0402_1%

@ PR321 2M_0402_1%

@ PQ307 PDTC115EU_SOT323-3

@ PR324 100K_0402_1%

<33> FSTCHG

@ PQ308 2N7002KW_SOT323-3

<28,33,39,44,45,46> SUSP#

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

Design Notes

Range : 65 - 90W system, Support 3S and 4S battery
Battery discharge power support to 65W for 3S
Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

Circuit Design
1. ACOK,ILIM pull high voltage need base on EC VCC
2. Use 7X7 choke and 3X3 MOSFET
   Charge current 2A, for 4S1P (16650)
   Power loss : 0.67W
   Power density : 0.65

Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout :
No communication within 175s(default)
3. ACOC : 3.3 X Input current DAC setting
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (Default)
9. IFAULT LOW : 150mV (Default)

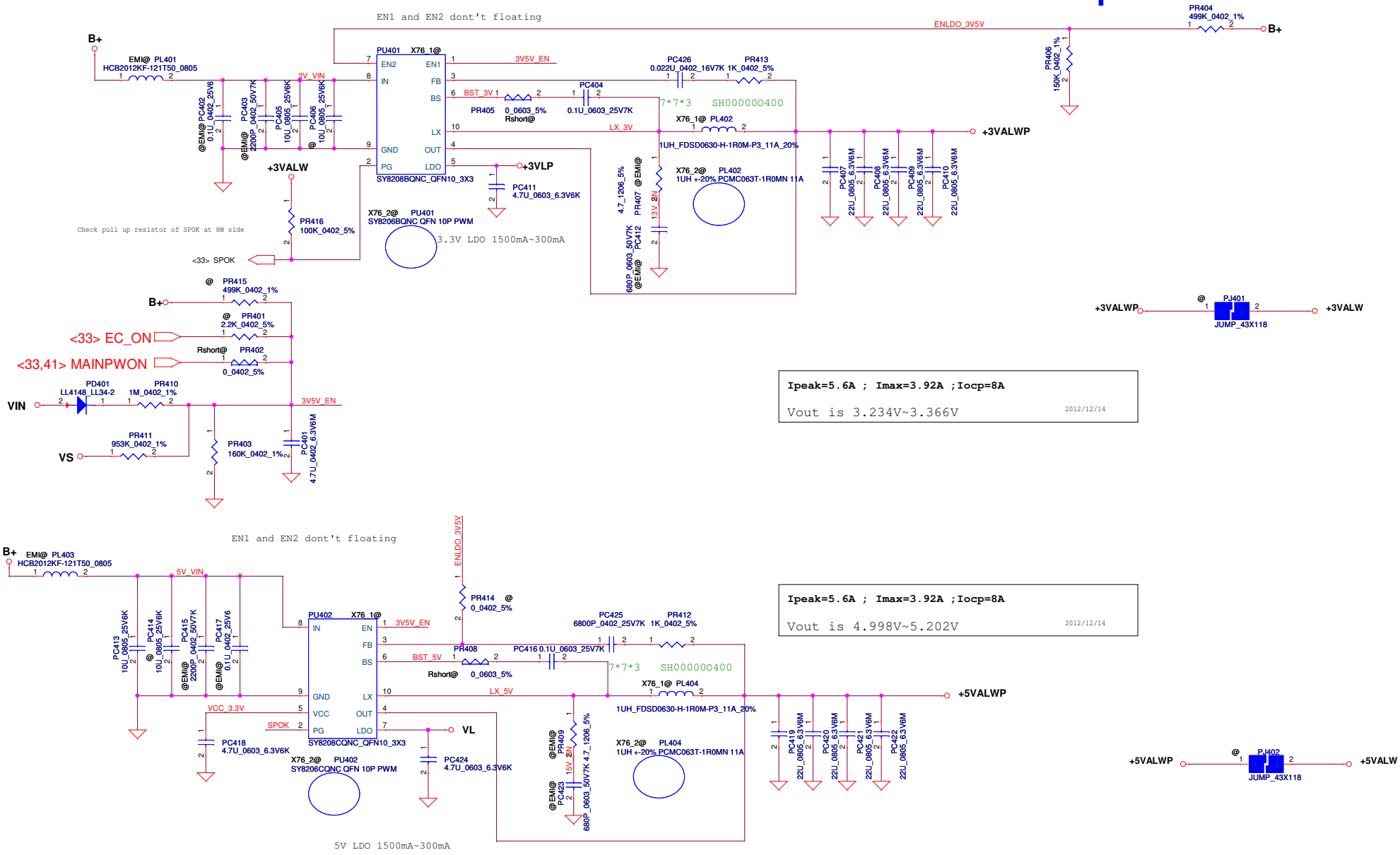
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: V5MM2_SB | Rev: 1.0

Date: | Sheet 42 of 57



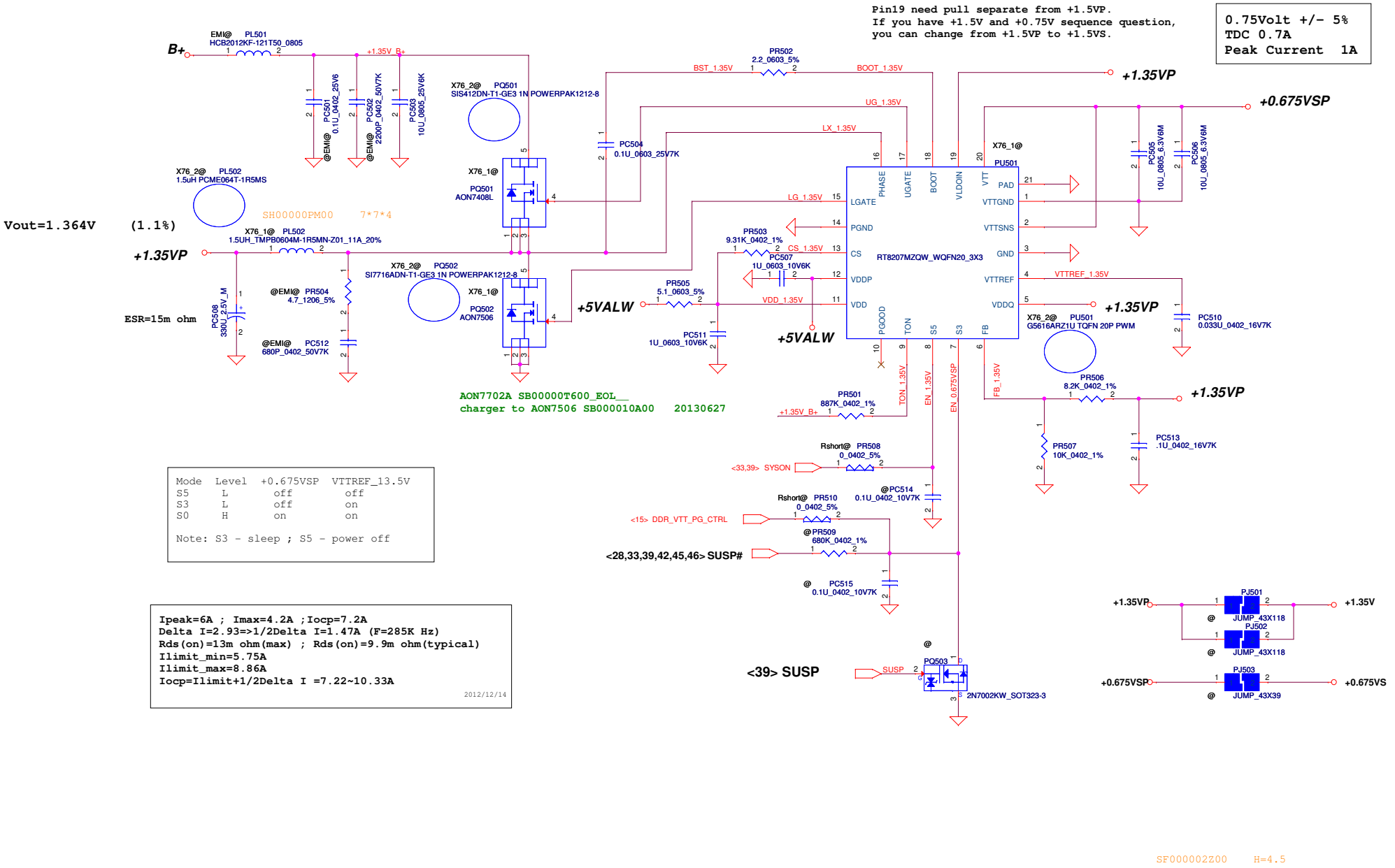
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, August 27, 2013 | Sheet 43 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

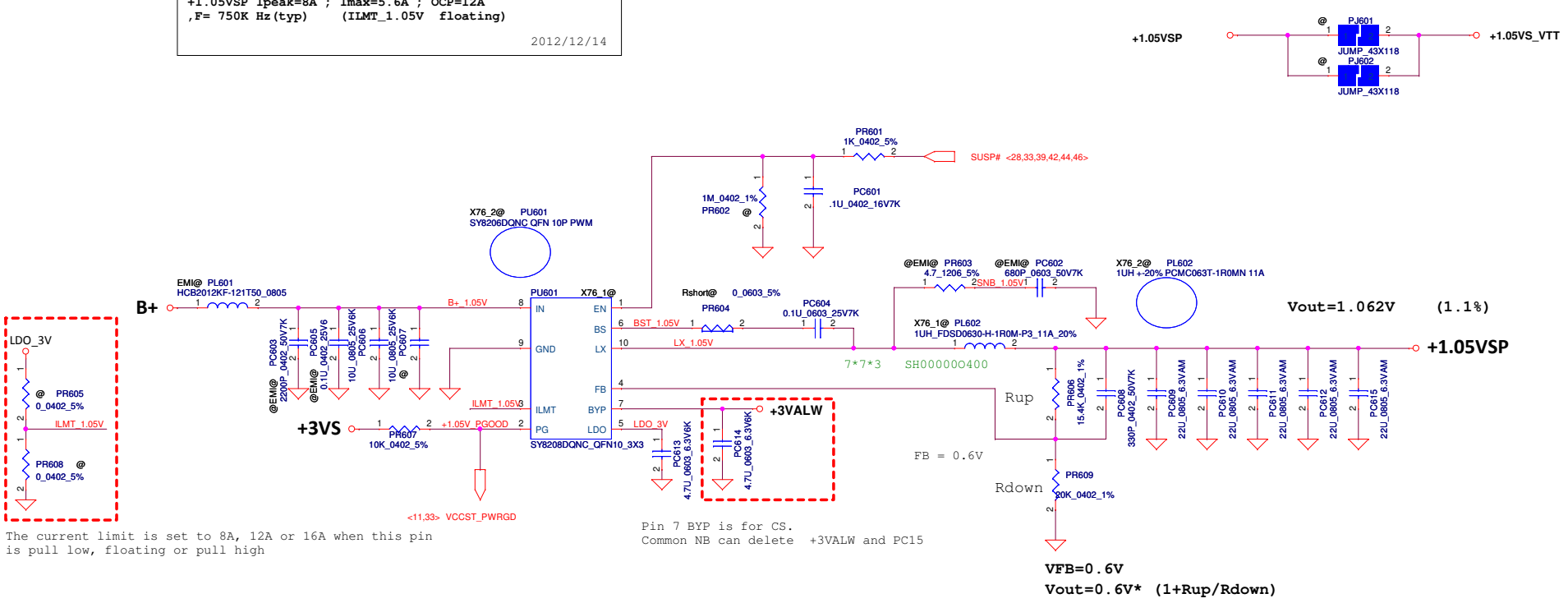
Title: *1.35VP/0.675VSP*

Size: Custom | Document Number: *V5MM2_SB* | Rev: 1.0

Date: | Sheet 44 of 57

+1.05VSP Ipeak=8A ; Imax=5.6A ; OCP=12A
,F= 750K Hz(typ) (ILMT_1.05V floating)

2012/12/14



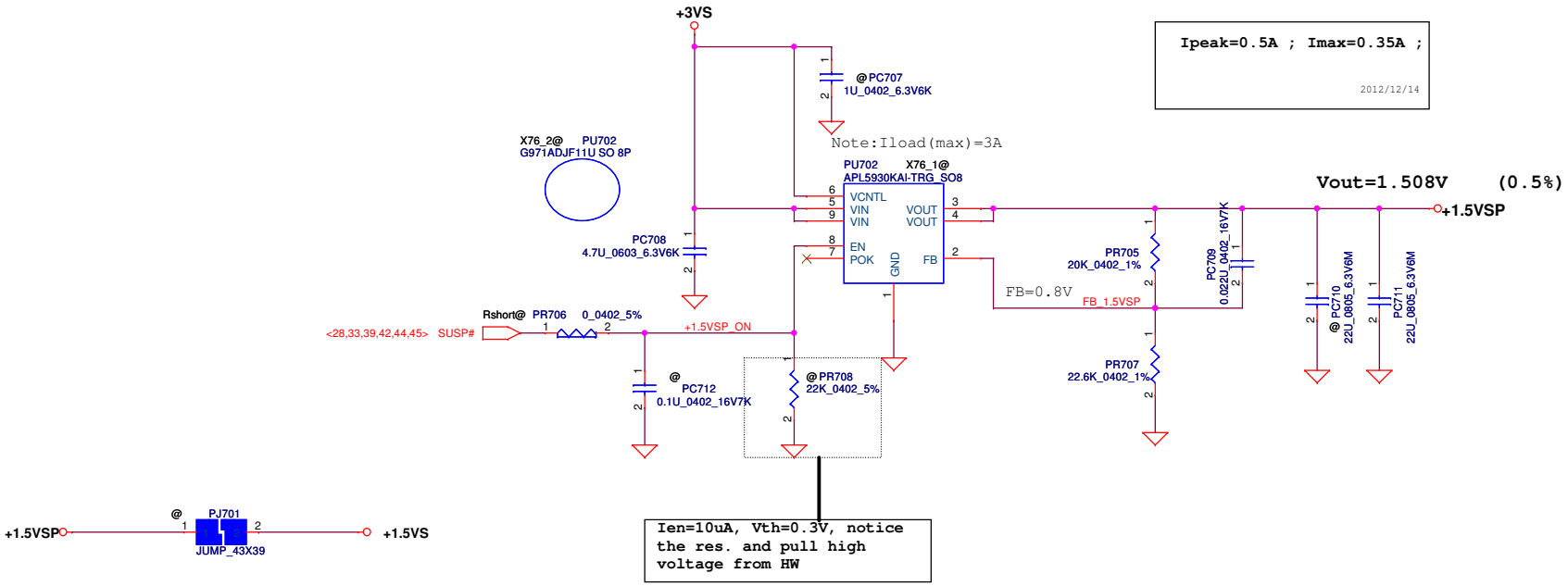
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: +1.05VSP

Size: Custom | Document Number: V5MM2_SB | Rev: 1.0

Date: Tuesday, August 27, 2013 | Sheet 45 of 57



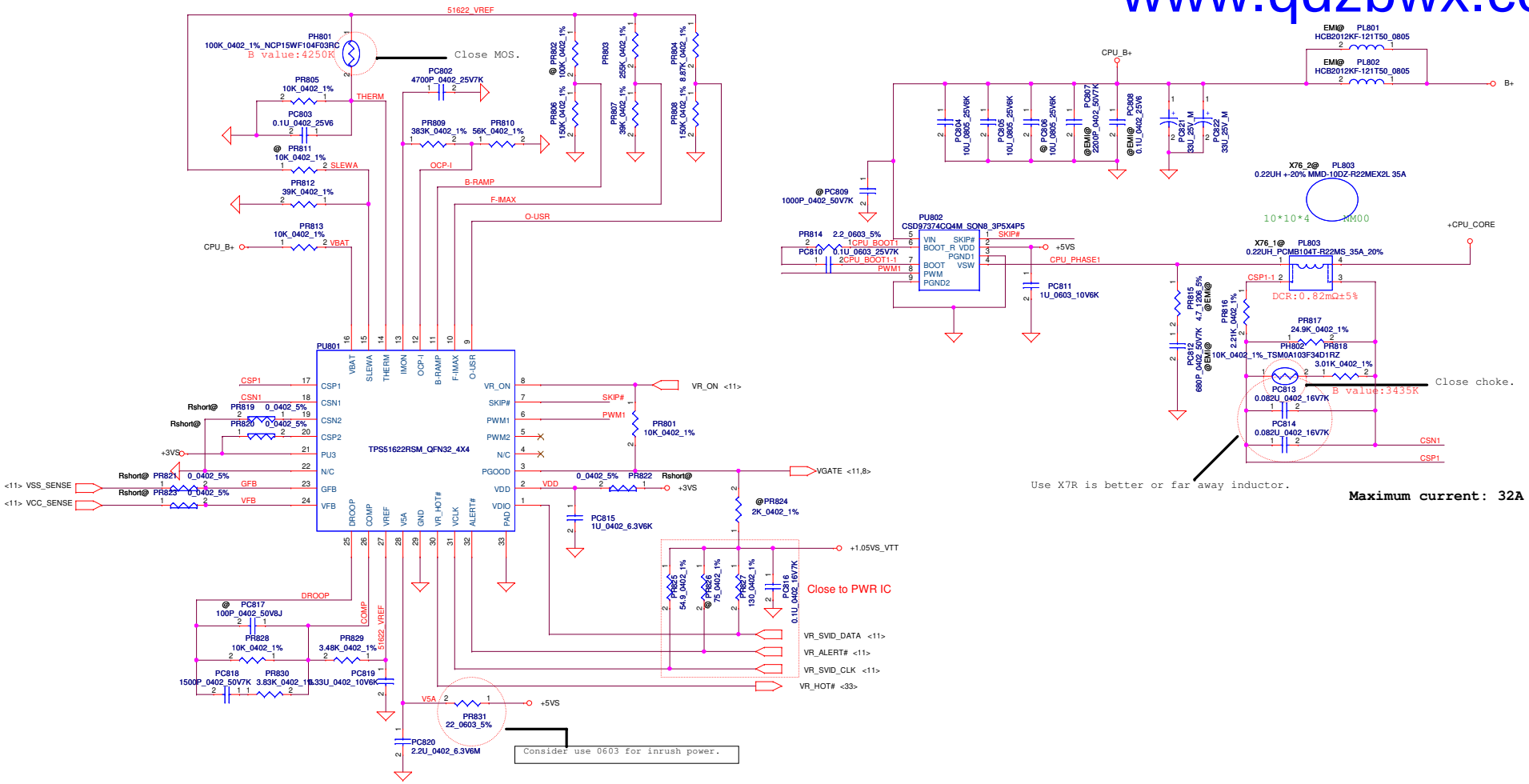
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: *+1.5VSP*

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, August 27, 2013 Sheet 46 of 57



VIN	12V-20V
MAX current	32A
Thermal current	10A
Dynamic current	27A
Over current level	45A
Switching frequency	600KHz
Boot voltage	1.7V
DC Load- line	2m Ohm

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

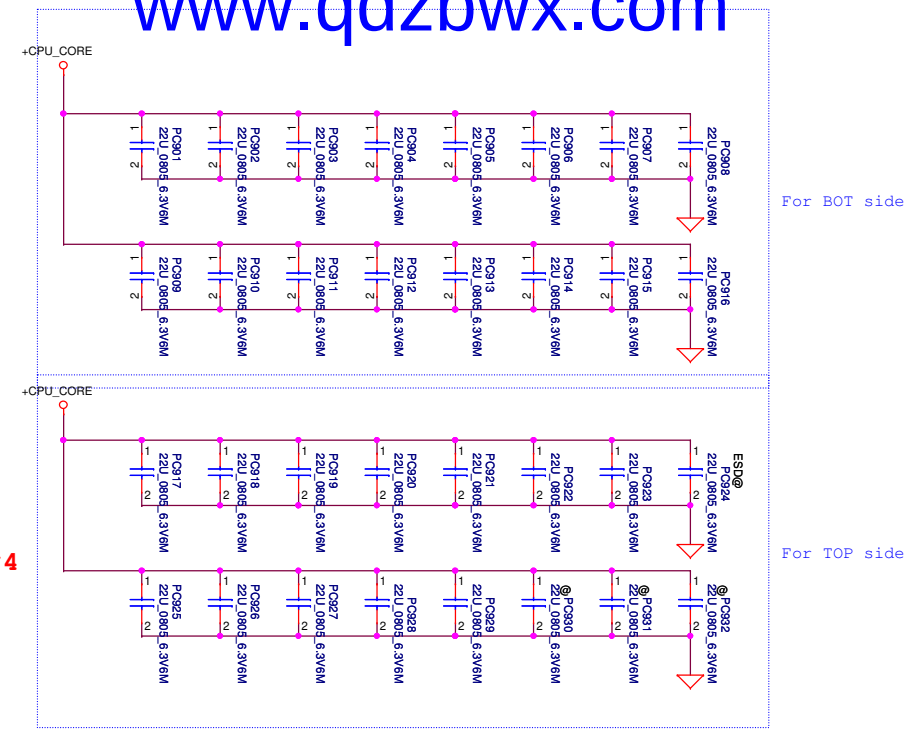
Title: +CPU_CORE

Size	Document Number	Rev
Custom	V5MM2_SB	1.0

Date: Tuesday, August 27, 2013 | Sheet 47 of 57

PWR Rule

CPU DCLL=1.5m ohm dedign 330uF/9m *0, 22uF *30



22u *28, @*4

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

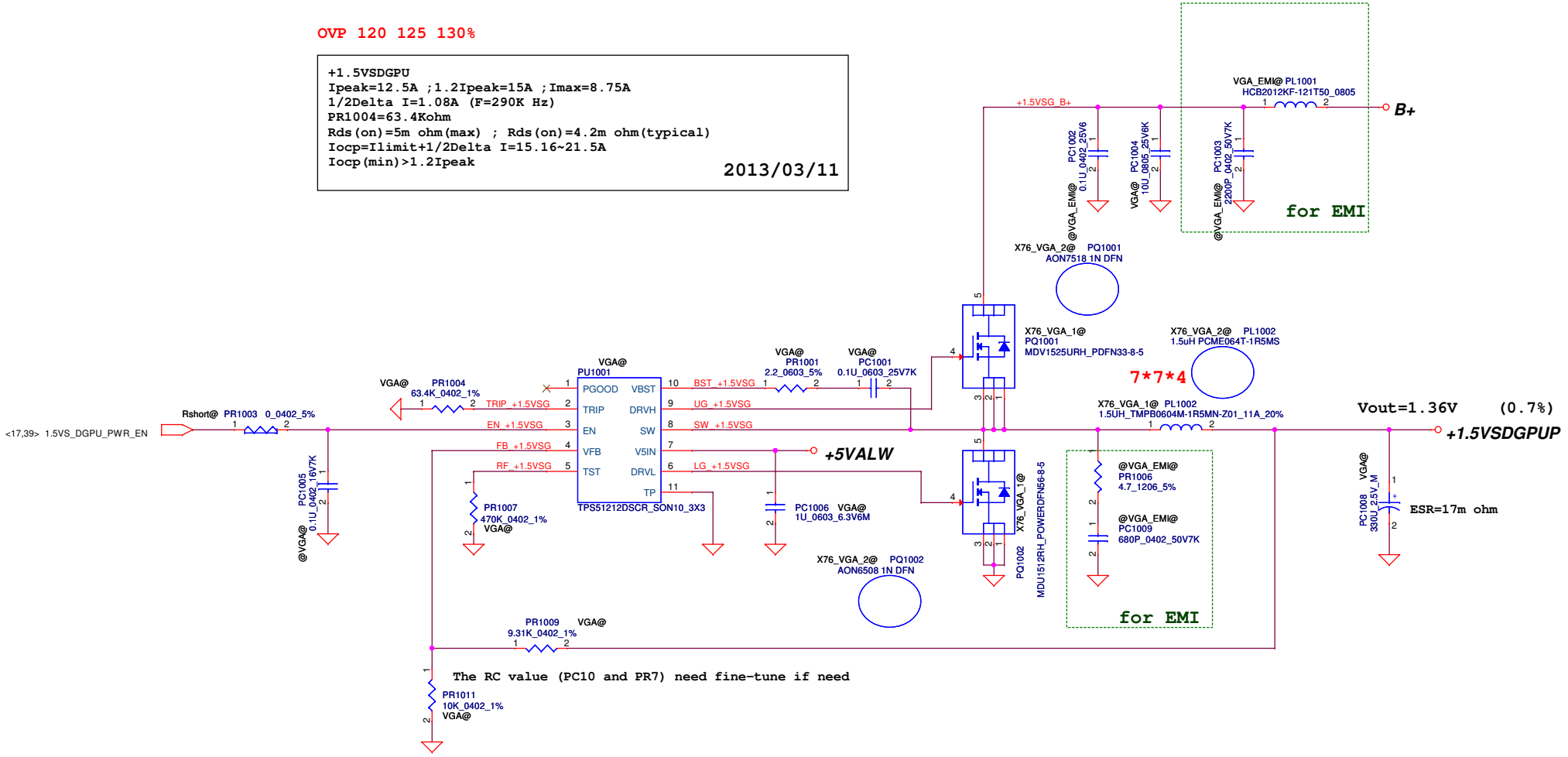
Title: CPU_CORE_CAP

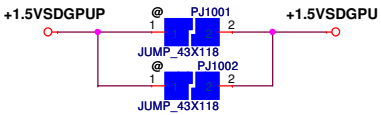
Size: Custom | Document Number: V5MM2_SB | Rev: 1.0

Date: Tuesday, August 27, 2013 | Sheet 48 of 57

OVP 120 125 130%

```
+1.5VSDGPU
Ipeak=12.5A ;1.2Ipeak=15A ;Imax=8.75A
1/2Delta I=1.08A (F=290K Hz)
PR1004=63.4Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=15.16~21.5A
Iocp(min)>1.2Ipeak
                                        2013/03/11
```





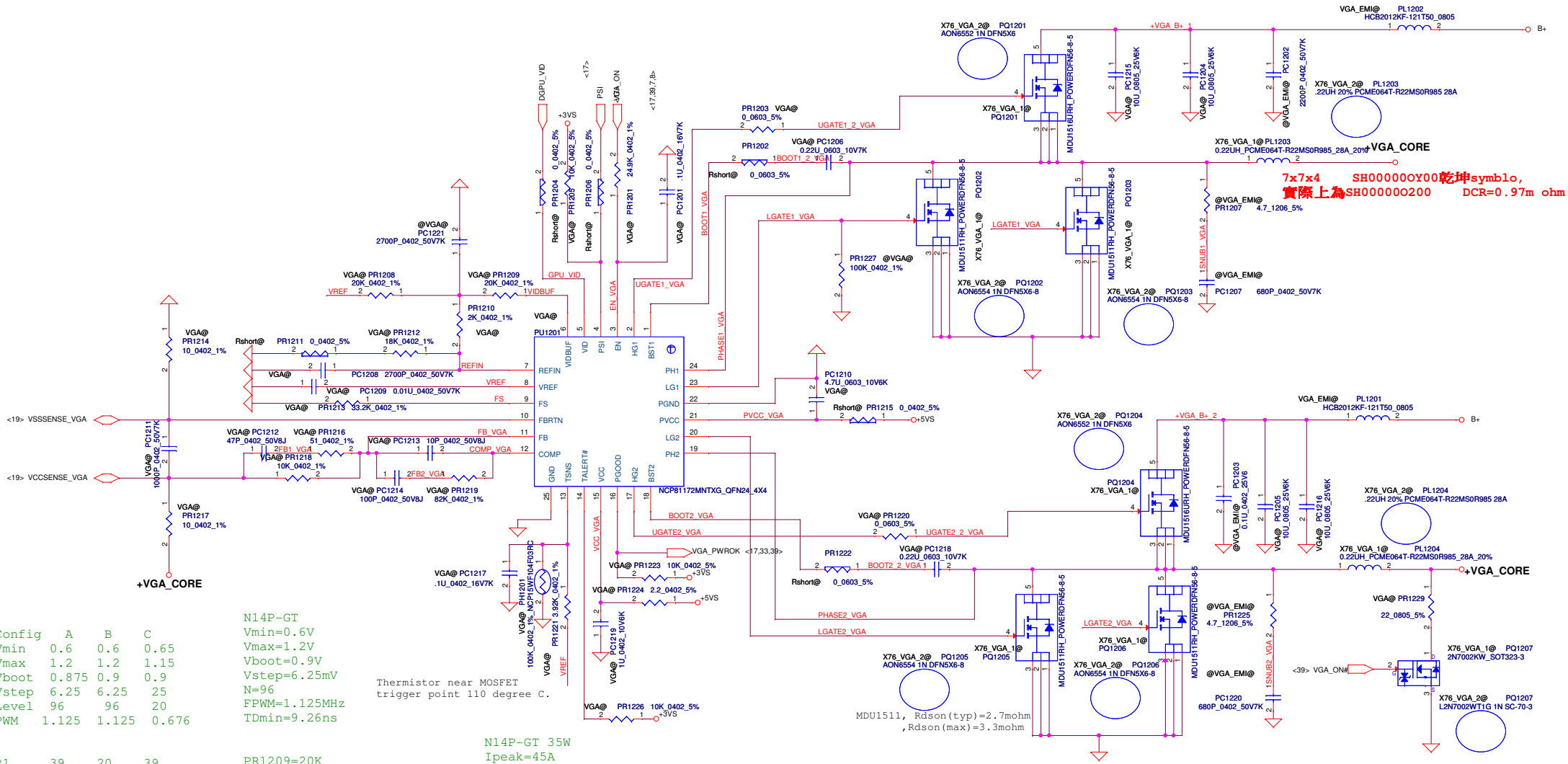
Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: *+1.5VSDGPUP*

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, August 27, 2013 Sheet 49 of 57



Config	A	B	C
Vmin	0.6	0.6	0.65
Vmax	1.2	1.2	1.15
Vboot	0.875	0.9	0.9
Vstep	6.25	6.25	25
Level	96	96	20
PWM	1.125	1.125	0.676

R1	39	20	39
R2	39	20	30
R3	1.5	2	3
R4	30	18	24
R5	1.5	0	3
C	1.5	2.7	1.8

N14P-GT
Vmin=0.6V
Vmax=1.2V
Vboot=0.9V
Vstep=6.25mV
N=96
FPWM=1.125MHz
TDmin=9.26ns

PR1209=20K
PR1208=20K
PR1210=2K
PR1212=18K
PR1211=0K
PC1208=2.7nF

Thermistor near MOSFET
trigger point 110 degree C.

N14P-GT 35W
Ipeak=45A
Imax=31.5A
Iocp=80A
Fsw=450KHz
bulk cap 330uF 9m *3 560uF*1

Security Classification	Compal Secret Data		
Issued Date	2011/12/05	Deciphered Date	Date of EOP

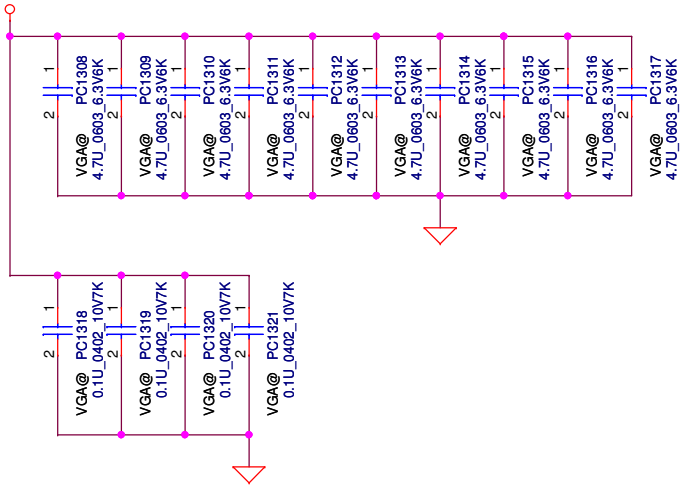
Compal Electronics, Inc.

Title: VGA_COREP

Size | Document Number | Rev 1.0

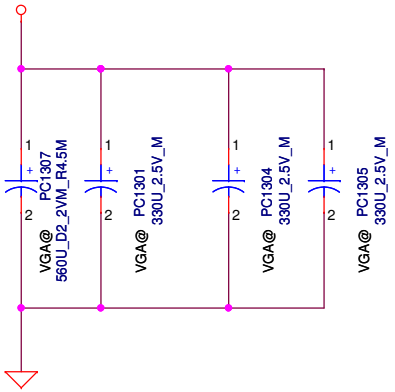
Date: Tuesday, August 27, 2013 | Sheet 50 of 57

+VGA_CORE Under VGA Core

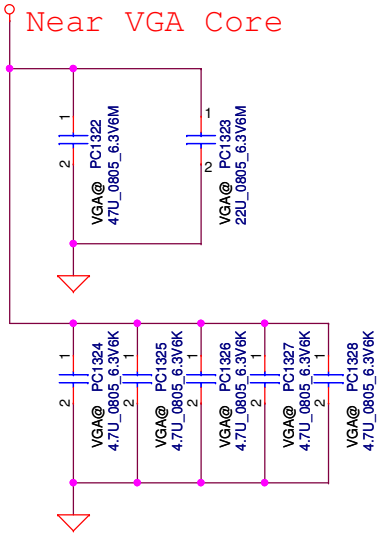


GB4-128
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

+VGA_CORE



+VGA_CORE Near VGA Core



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: VGA_CORE CAP

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, August 27, 2013 | Sheet 51 of 57

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Acoustic noise	3V 5V light load efficiency improvement		3V/5V	1.Add 2pcs 1K_0402_5% (PR412 PR413) 1pcs 4700P_0402_25V7K (PC425) 1pcs 0.047U_0402_25V7K (PC426) 2.Add 4.7u_0402_6.3V6M (PC401)	01/15	EVT
2	Silergy update revision	3V 5V enable control for Rev0.3. But un-pop.		3V/5V	1.Add un-pop 2pcs 0402 resistors(PR415 PR414) 2.remove (PR207)	01/15	EVT
3		Reduce part count		VGA/CPU	Change to R-short (PR1211 PR1204 PR1206 PR1215 PR822)	01/15	EVT
4		modify charger current to meet battery charge time.		Charger	0.02_1206_1%_SD00000S110 charger to 0.01_1206_1%_SD00000K820 (PR310)	01/15	EVT
5		The modify values for CPU transition test		CPU	1.PR803 270K_0402_1%_SD00000G280 change to255K_0402_1%_SD034255380 2.PR809 392K_0402_1%_SD034392380 change to383K_0402_1%_SD034383380 3.PR831 10_0603_5%_SD013100A80 change to22_0603_5%_SD000001R80 4.PC820 1U_0603_10V6K_SE080105K80 change to2.2U_0402_6.3V6M_SE000008880	01/15	EVT
6		BI_GATE remove		3V/5V	PQ401 2N7002KW_SOT323-3_SB000009Q80 remove.	01/16	EVT
7		HW VGA_sequence test		VGA	1.PC1201un-pop charger to 0.1U_0402_16V7K_SE076104K80 2.PR1201un-pop charger to 24.9K_0402_1%_SD034249280 3.PR12280_0402_5% charger to un-pop	01/21	EVT
8		When pwm IC shutdown on S0, EC could detect SLP_S5#, but cannot detect PCH was no power.		3V/5V	PR416 add 100K_0402_5%_SD028100380	3/11	DVT
9		The 5VALW will fast than 3VALW and the rising time will under 2mS.		3V/5V	PC426 4700P_0402_25V7K_SE075472K80 change to 0.01U_0402_25V7K_SE075103K80 PC425 0.047U_0402_25V7K_SE00000MJ00 change to 6800P_0402_25V7K_SE075682K80	3/11	DVT
10		VRAM efficiency improvement		1.5VDGPU	1.PQ1002 AON7702A_SB00000T600 change to MDU1512RH_POWERDFN56-8-5_SB00000SY00 2.PQ1001 AON7408L 1N DFN_SB00000H800 change to MDV1525URH 1N PDFN33-8_SB00000S600 3. PL1002 2.2uH_7*7*3_SH00000MR00 charger to 1.5uH_7*7*4_SH00000PM00	3/11	DVT
11		The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail.		VGA	PR1229 add un-pop 22_0805_5%_SD002220A80 PQ1207 add un-pop 2N7002KW_SOT323-3_SB000009Q80	3/11	DVT

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		remove VGA enable for +3VSDGPU		VGA_COREP	remove PR1228_0_0402_5%	3/11	DVT
2		VRAM voltage change to 1.35V.		+1.5VSDGPUP	PR1009 11.5K_0402_1%_SD034115280 change to 9.31K_0402_1%_SD034931180 PR1004 137K_0402_1%_SD034137380 change to 63.4K_0402_1%_SD03463K280		DVT
3		ESD request		CPU capacitor	Add PC924 22U_0805_6.3V6M_SE000000I10	3/11	DVT
4		VCIN1 function		BATTERY CONN/OTP	PR225 5.1K_0402_1%_SD034510180 change to 9.76K_0402_1%_SD034976180_90W@ 1.02K_0402_1%_SD034102180 change to 9.76K_0402_1%_SD034976180_65W@ PR207 UN-pop-0K_0402_1%_SD034100280 change to 47.5K_0402_1%_SD034475280_90W@ UN-pop-0K_0402_1%_SD034100280 change to 71.5K_0402_1%_SD034715280_65W@		
5				CHARGER	PR318 499K_0402_0.1%_SD00000U380 change to 499K_0402_1%_SD034499380	3/11	DVT
6		Material change		CPU_CORE 1.05V	PH801 SL200000U00 change to SL200000V00 PL602 SH00000PJ00 change to SH00000O400	4/16	PVT-1
7		The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail.		VGA	Add PR1229 22_0805_5%_SD002220A80 Add PQ1207 2N7002KW_SOT323-3_SB000009Q80	5/14	PVT-1
8		Reduce part count		1.35V/1.5VSP /1.5VSDGPU	SD028000080 Change to 0402_R-short (PR510 PR706 PR1003)	5/14	PVT-1
9		Reduce part count		3V/5V/ 1.05V/VGA	SD013000080 Change to 0603 R-short (PR405 PR408 PR604 PR1202 PR1222)	5/14	PVT-1
10		follow ON solution for VGA		VGA	1. PC1221_SE074272K00_2700P charger to un-pop. 2. PC1208_SE071101J80_100P charger to SE074272K00_2700P		PVT-1
11		Adjust the FB voltage for 1.35V		1.35V	PR506_8.2K_0402_1%_SD000004100 charger to 8.06K_SD034806180.		PVT-1
12		Material EOL		1.35V	PQ502 AON7702A SB00000T600 change to AON7506 SB000010A00		PVT-2
13		VCIN1 Recovery 85% chang to 100%		3V/5V BATTERY CONN /OTP	PR411 316K_0402_1%_SD034316380 change to 953K_0402_1%_SD00000X100 PR403 402K_0402_1%_SD034402380 change to 160K_0402_1%_SD034160380 PR225 9.76K_0402_1%_SD034976180 change to 10K_0402_1%_SD034100280(65W@) change to 10.5K_0402_1%_SD034105280 (90W@) PR207 71.5K_0402_1%_SD034715280 change to 127K_0402_1%_SD034127380(65W@) change to 91K_0402_1%_SD034910280 (90W@)		PVT-2 PVT-2
14		Adjust the FB voltage for 1.35V		1.35V	PR506_8.06K_SD034806180 charger to 8.2K_0402_1%_SD000004100.		PVT-2
15		Fixed system can't power on. (HW suggest delay the 3V power on sequency.)		3V/5V	PC426 0.01U_25V_K_X7R_0402_SE075103K80 change to 0.022U_16V_K_X7R_0402_SE076223K80	8/7	PVT-3
16		ACER must not GC6 function.		VGA	1.PR1229 22_0805_5%_SD002220A80 =>un-pop 2.PQ1207 2N7002KW_SOT323-3_SB000009Q80 =>un-pop	8/7	PVT-3
17		Cancel ->ACER must not GC6 function.		VGA	1.PR1229 un-pop =>22_0805_5%_SD002220A80 2.PQ1207 un-pop =>2N7002KW_SOT323-3_SB000009Q80	8/12	PVT-3

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Item	Page #	Date	Issue Description	Solution Description	Stage
1	28	2013/1/8	Add DP++ Schematic	Add Q101,Q102,Q46,R336 , reserve R499,R502	DVT
2	28	2013/1/8	Add DP++ config	Add DM@ , NDM@	DVT
3	28	2013/1/8	Change mDP HPD Schematic from Before-IC to After-IC		DVT
4	28	2013/1/8	for LB_RST no use	pop R1327 for LB_RST no use	DVT
5	28	2013/1/8	LB HPD issue	Change R1344 from 100K to 10K	DVT
6	28	2013/1/8	for not support LB wake function	Add R503 and unpop it	DVT
7	28	2013/1/8	for not support LB wake function	Add J24	DVT
8	31,34	2013/1/8	Remove LAN/B from Acer request	Remove JLAN1 , Add JPWR1 (same as JBL1)	DVT
9	31,33	2013/1/8	Remove LAN/B from Acer request	1. LAN_CLKREQ# pull-high to +3VS (R131,後面remove) 2. Remove C530,R312,R1170 3. reserve R234,R236,R237 for differential pair route space	DVT
10	31	2013/1/8	EC Board ID for Rev0.2	Change R1191 to 8.2K pop R1190,R1191	DVT
11	7	2013/1/8	Change SPI ROM from 4M+2M to 8M	Remove U14,RP20,R109,R402,C67,C453	DVT
12	26	2013/1/8	1.abnormal display via re-driver board 2. to solve the problem without any gauge increased	1. Connect JEDP1_pin27 to +3VS, this solution is only for cable which need to pass via re-driver board 2. Add R522,C140 , unpop R421,R424 3. Change Q43 to 2N7002K	DVT
13	8	2013/1/8	incorrect gpio define	unpop R214 ,pop R205	DVT
14	28	2013/1/8	For LightningBolt debug , will unpop in PVT	pop SW7(後面remove)	DVT
15	38	2013/1/8	Change TPM IC P/N	Change U89 from SA00005XH00 to SA00005XH40	DVT
16	26,32	2013/1/8	For EMI request , change EMI part P/N	Change L26 to SM01000EJ00 Change L17,L18,L20,L21,L22 to SM070001R00	DVT
17	30	2013/1/9	some risk for OPs on factory side	Change JMINI1 and JMINI2 to JWLAN1 and JMSATA1	DVT
18	34	2013/1/9	Pull-high 10K to +3VS for SMB_ALERT#_R	Add R452	DVT
19	34	2013/1/9	Update KB backlight schematic	Remove Q56,R928	DVT
20	34	2013/1/9	Battery can't detect issue (BI_GATE)	Add R530 , unpop Q30	DVT
21	33	2013/1/9	GC6 schematic update	connect VGA_PWROK to EC_pin120	DVT
22	7	2013/1/9	Change SPI serial resistor value	Change RP19,R108 from 22ohm to 15ohm	DVT
23	37	2013/1/9	For BI signal screw hole	Add H19	DVT
24	7	2013/1/9	Change SPI ROM from dual to single	Remove U14,RP20,R109,R402,C67,C453 (多餘)	DVT
25	7	2013/1/14	LAN_CLKREQ# already pull-up on CPU side	Remove R313(已有R52 pull-up)	DVT
26	8	2013/1/15	For Cost/Part count	Remove R66 unpop R67,U30 Change R403 from 0ohm to 2ohm	DVT
27	28	2013/1/15	For Cost/Part count	Remove SW7,C1443 unpop D64,D65,D66	DVT
28	33	2013/1/15	For Cost/Part count	Remove R1160	DVT
29	34	2013/1/15	For Cost/Part count	Remove R930,SW1	DVT
30	34	2013/1/15	Update BI_GATE schematic	Remove D43,Q34,R489,R530,C888,C890 Q30 change from P-MOS to N-MOS R486,R487 change to 100K ohm	DVT
31	39	2013/1/15	For Cost/Part count	Change R987 to 2ohm	DVT
32	7	2013/1/15	For Cost/Part count	Change R111 to R-short 0402	DVT
33	27	2013/1/15	For Cost/Part count	Change R368,R369,R409,R410,R417,R418,R415,R419 to R-short 0402	DVT
34	30	2013/1/15	For Cost/Part count	Change R876,R877 to R-short 0402	DVT
35	31	2013/1/15	For Cost/Part count	Change R49 to R-short 0805	

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36	33	2013/1/15	For Cost/Part count	Change R1162 to R-short 0805	DVT
37	34	2013/1/15	For Cost/Part count	Change R929 to R-short 0402	DVT
38	35	2013/1/15	For Cost/Part count	Change R495,R496,R497 to R-short 0603	DVT
39	37	2013/1/15	For Cost/Part count	Change R508,R510 to R-short 0603	DVT
40	39	2013/1/15	For Cost/Part count	Change R988 to R-short 0402	DVT
41	26	2013/1/16	For ESD request	Add C803	DVT
42	34	2013/1/16	Update BI_GATE schematic	Change R486 to 510K , BI_GATE power change to +RTCVCC	DVT
43	8	2013/1/17	For ESD request	Add C932,C936,C937	DVT
44	11	2013/1/17	For ESD request	Add C920,C925	DVT
43	39	2013/1/17	For ESD request	Add C940	DVT
44	6	2013/1/21	Change main source on DVT only	Y1 change to SJ100004Z00	DVT
45	32	2013/1/21	Change main source on DVT only	U76,U78 change to SA00003TV00	DVT
46	29	2013/1/21	Change main source for AP-code	Q95,Q96 change to SB966750010	DVT
47	8,39	2013/1/21	Update GC6 schematic	Pop R404,R405 unpop R406,R407 R469 change from 330k to 47k	DVT
48	29	2013/1/21	Update LB schematic	R1347 change from 100k to 100 ohm	DVT
49	34	2013/1/21	unpop debug switch	unpop SW4	DVT
50	40-53	2013/1/22	update Power schematic 0121A		DVT
51	34	2013/1/22	For X1 code	Change U82 from SA00001TC00 to SA000057Z00	DVT
52	26	2013/1/22	For SMT 統一料	Change L26 back to SM010014520	DVT
53	26	2013/1/23	eDP HPD issue	Pop R421,R424 ; unpop R522 , C140	DVT
54	26	2013/2/7	eDP HPD issue	Remove Q43	PVT
55	20	2013/2/7	VGA schematic mistake	Change R1245 from 42.2ohm to 40.2ohm	PVT
56	39	2013/2/19	Change EN pin for +1.5VSDGPU off-current	Q64 change to Dual-N and gate pin change to 1.5VS_DGPU_PWR_EN , add R984,R998	PVT
57	33	2013/2/19	Add SPOK to turn on/off +3,5VALW	Add EC pin_16 named SPOK	PVT
58	36	2013/2/19	Audio SPK sound not balance issue	Change R575 from 1k ohm to 1.2k ohm	PVT
59	34	2013/2/19	BI_GATE issue	Change H9 symbol	PVT
60	32	2013/2/19	Add RF frame	Add CLIP1	PVT
61	26	2013/2/19	ESD issue	C803 change from 0.1u to 22p	PVT
62	33	2013/2/19	Board ID for Rev 0.3 PCB	R1191 change from 8.2k to 18k	PVT
63	29	2013/2/19	Change LBT 5V switch schematic	Add U38(USB power switch),C526 Remove Q95,Q96,Q97,U156,R1337,R1338,R1343,R1339.R1340 Change R1347 from 100_0402 to 470_0603 for discharge Change R1341 from 100k to 10k (follow CR)	PVT
64	26,33	2013/2/19	No need support wake by Home-Key	Change power to home key from +3VALW to +3VS (JSNSR1.pin12) Change Pull-up domain from +3VALW to +3VS (R1181,R1182,R1183)	PVT
65	9	2013/2/19	Add GPIO pin for TPM/no-TPM sku	Add R312,R313 and unpop R312	PVT
66	30	2013/2/27	AOAC on/AOAC off co-lay	Add J21 from +3VS unpop U79,C941	
67	20	2013/2/27	VGA part count and unpop reduce	Remove C1316,C1317	
68	22	2013/2/27	VGA part count and unpop reduce	Remove C1341,C1342,C1327 unpop C1345,C1346,C1348,C1350,C1329,C1331,C1334,C1336	
69	23	2013/2/27	VGA part count and unpop reduce	Remove C1366,C1367,C1355 unpop C1369,C1371,C1372,C1374,C1357,C1358,C1362,C1363	
70	24	2013/2/27	VGA part count and unpop reduce	Remove C1392,C1393,C1378 unpop C1394,C1397,C1399,C1401,C1380,C1382,C1385,C1387	
71	25	2013/2/27	VGA part count and unpop reduce	Remove C1417,C1418,C1404 unpop C1421,C1422,C1423,C1426,C1405,C1407,C1413,C1415	
72	26	2013/2/27	For Cost/Part count	R424 change to R-short 0402 Remove R522,C140	

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73	37	2013/3/4	ME screw change	H4 change from 3P0 to 4P5 , H3 from 2P5 to 3P0	PVT
74	32	2013/3/5	USB charger schematic update	R853 pull-up power rail change from +3VALW to +3VALW_EC	
75	31	2013/3/5	Remove JHDD2	Remove JHDD2	
76	11,15,33	2013/3/5	For ESD request	pop C6,C117,C1255 (Page11,Page15,Page33)	
77	30	2013/3/5	For ESD request	Add C62,C63,C64	
78	29	2013/3/5	For ESD request	Add C65	
79	11	2013/3/6	For Cost/Part count	Change R167,R168 to R-short 0402	
80	26	2013/3/6	For Cost/Part count	Change R355,R359,R366,R367,R413,R414,R335 to R-short 0402	
81	32	2013/3/6	For Cost/Part count	Change R852,R855,R865,R866 to R-short 0402	
82	33	2013/3/6	For Cost/Part count	Change R80 to R-short 0402	
83	38	2013/3/6	For Cost/Part count	Change R978,R980 to R-short 0402	
84	20	2013/3/6	For Cost/Part count	Change R1241 to R-short 0603	
85	35	2013/3/6	For Cost/Part count	Change R518,R520,R527,R529 to R-short 0603	
86	36	2013/3/6	For Cost/Part count	Change R519,R521,R524,R525,R556,R566,R567 to R-short 0603	
87	17	2013/3/6	Update GC6 schematic	Add D3,Q95 Remove Q84,,Q90,R1204 Change R1201 from 10k to 1k Reserve R1205	
88	35,36	2013/3/6	Audio PoPo issue	Add U31,R1313 and un-pop Add R408 Amp PD pin change from EC_MUSE# to AMP_MUTE#	
89	9,34	2013/3/6	Add I2C for touchpad	Add R84,R85 and unpop Add R82,R83,R1337,R1338	
90	28	2013/3/8	Update LBT schematic (TI request)	Swap Q101A pin3 and pin4	
91	19	2013/3/8	Change VRAM power from 1.5V to 1.35V	Change R1229 from 24.9k to 34.8k	
92	ALL	2013/3/11	Combine power schematic 0311A	Combine power schematic 0311A	
93	38	2013/3/13	Change TPM power from +3VALW to +3VS	pop J17 , unpop J16	
94	28	2013/4/1	Add F1 for LBT fuse	Add F1	PVT2
95	34	2013/4/1	Update H9 symbol	Update H9 footprint	
96	ALL	2013/4/1	Update All RC*NEW footprint		
97	7,10,31	2013/5/9	Remove LAN	Remove C168,C169,R234,R,236,R237	
98	34	2013/5/9	Reserve one/two Lid-switch funtion	Add U83,U84,R930.R931,C989,C990,C991,C992	
99	6,11	2013/5/9	For Cost/Part count	Change R76,R180 to R-short 0402	
100	35,36	2013/5/9	For Cost/Part count	Change R408,R512,R513 to R-short 0402	
101	6,10	2013/5/9	For Cost/Part count	Change R75,R155 to R-short 0603	
102	28	2013/5/9	For Cost/Part count	Change R373,R381 to R-short 0402	
103	9	2013/5/10	Add net for 2nd hall sensor Lid-out	Change PCH_GPIO14 for EC LID_OUT_TAB (LID_OUT need place between GPIO1 to GPIO15)	
104	7,9	2013/5/10	Change Card-Reader CLK from Port5 to Port1	modify net name : GPIO19 -> CARD_CLKREQ# CARD_CLKREQ# -> GPIO23	
105	33	2013/5/16	Add Pull-up for LID_SW#_TAB	Add R1163	
106	9	2013/5/16	reserve Pull-up for EC_LID_OUT#_TAB	Add R249 and reserve it	
107	16	2013/5/22	pop C141	Pop C141	
108	15,16	2013/5/22	Change 1uF to 2.2uF	Change C108,C123,C130,C143 to 2.2uF	
109	22,23	2013/5/22	Change 1uF to 2.2uF	Change C1328,C1343,C1356,C1368 to 2.2uF	
110	24,25	2013/5/22	Change 1uF to 2.2uF	Change C1379,C1395,C1409,C1419 to 2.2uF	
111	28	2013/5/22	Co-lay LBT schematic	Remove D1 Add U66 and co-lay with F1	
112	12,15	2013/5/22	For Cost/Part count	Remove R210,C50,C34,C126	
113	15,16	2013/5/22	For Cost/Part count	Remove C107,C109,C121,C122,C129,C131,C144,C146	

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114	22	2013/5/22	For Cost/Part count	Remove C1346,C1350,C1331,C1336	PVT2
115	23	2013/5/22	For Cost/Part count	Remove C1371,C1374,C1358,C1363	
116	24	2013/5/22	For Cost/Part count	Remove C1397,C1401,C1382,C1387	
117	25	2013/5/22	For Cost/Part count	Remove C1422,C1426,C1407,C1415	
118	30,31	2013/5/22	For Cost/Part count	Remove C946,C961,R869,R870,C870,C872	
119	33	2013/5/22	For Cost/Part count	Remove C1269,C1257	
120	28,29	2013/5/23	Change LBT power rail to +3VS/+5VS	U38 change from +5VALW to +5VS Remove J23 (+3VALW JUMP)	
121	22	2013/5/24	Pop VGA cap	Pop C1345,C1348,C1329,C1334	
122	23	2013/5/24	Pop VGA cap	Pop C1369,C1372,C1357,C1362	
123	24	2013/5/24	Pop VGA cap	Pop C1394,C1399,C1380,C1385	
124	25	2013/5/24	Pop VGA cap	Pop C1421,C1423,C1405,C1413	
125	33	2013/5/28	Change Board ID	Change R1191 from 18K to 33K	
126	28	2013/5/29	Add cap for Lightning Bolt 3V power	Add C262 (47uF)	
127	24	2013/5/30	Add cap for VGA_1.5V (debug)	Add C1401 (0.1uF)	
128	9	2013/5/30	Change LID_OUT GPIO from GPIO14 to GPIO8	Change GPIO8,GPIO14 net name	
129	34	2013/5/31	Update Part Number for PVT-2 SMT	Change U82,U83,U84 to SA00003GI00	
130	ALL	2013/6/4	Combine Power schematic 0603	Combine Power schematic 0603	
131	17	2013/6/4	Update Part Number for PVT-2 SMT	Change D62 to SCS00000Z00	
132	30	2013/7/2	Update WLAN schmatic	Change C958 from 4.7uF to 10uF Add C961	PVT3
133	6	2013/7/3	For layout spacing	Remove R74	
134	ALL	2013/7/5	Combine Power schematic 0627	Combine Power schematic 0627	
135	ALL	2013/7/29	Combine Power schematic 0729	Combine Power schematic 0729	
136	34	2013/7/31	Remove Buzzer schematic	Remove BUR1,Q53,R492,R493	Pre-MP
137	34	2013/7/31	Update BI GATE schematic (2nd BI_GATE)	Add R86 and unpop it	
138	30	2013/8/1	Update mSATA schematic for DEVSLP function	Change R877 from R-short to unpop	
139	33	2013/8/4	Change Board ID	Change R1191 from 33K to 56K	
140	ALL	2013/8/14	Combine Power schematic 0812A	Combine Power schematic 0812A	
141	ALL	2013/8/27	Combine Power schematic 0814	Combine Power schematic 0814	

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