SUZHOU-D

CPU : AMD Caspin
Chip Set : AMD RX881+SB710
Remarks : Tigris Platform

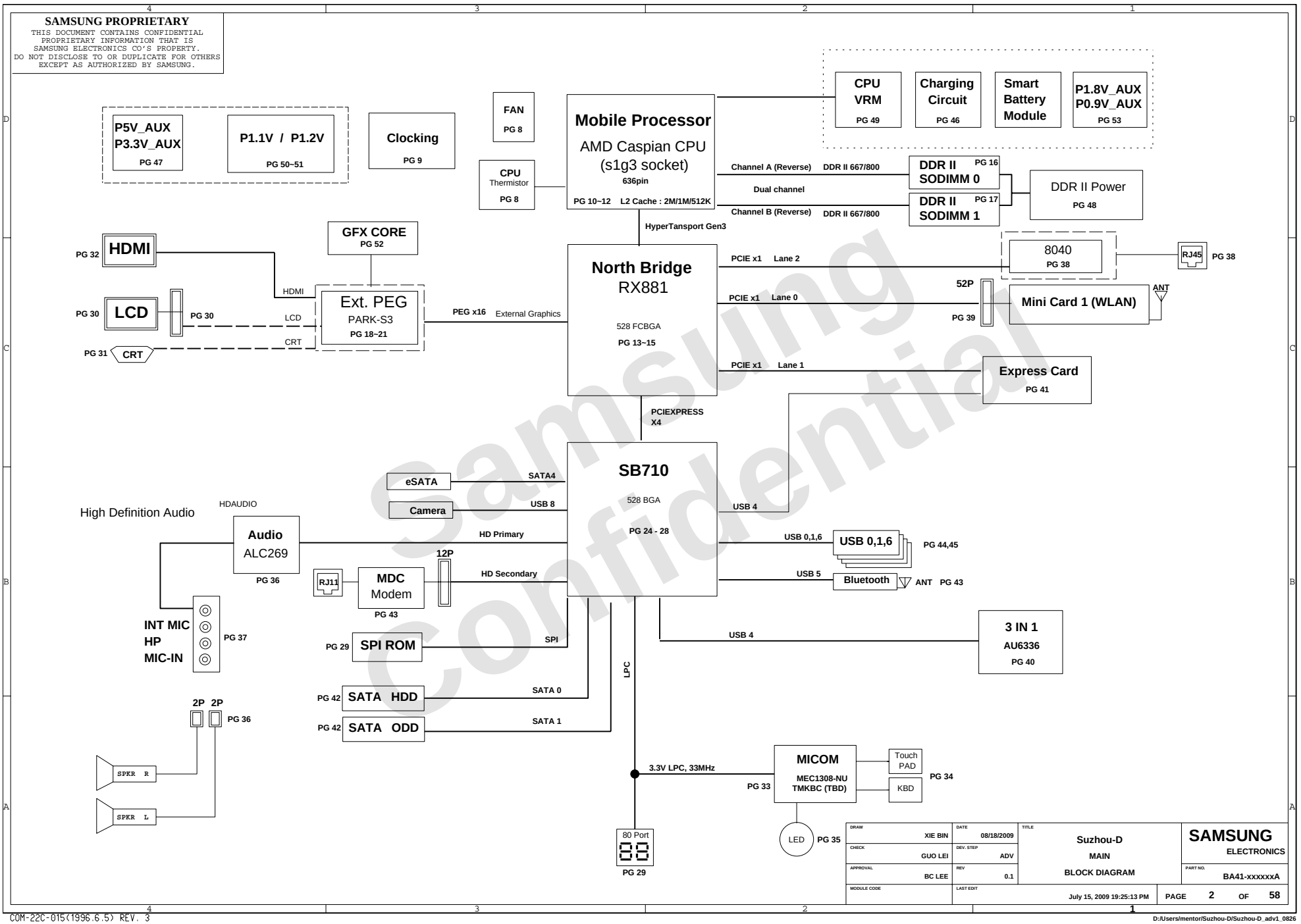
Model Name : Suzhou-D
PBA Name : MAIN
PCB Code : GCE :
NAN :
HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL
XIE BIN	GUO LEI	BC LEE

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

Table of Contents

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MAIN COVER	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 1 OF 58	



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 2 OF 58	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE0	Core Voltage for CPU
CPU_CORE1	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for M92,RX881
P1.2V	Core Voltage for SB710
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V_AUX	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MEC1308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

I²C / SMB Address

Devices	Address	Hex	Bus
SB710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	EXPRESS CARD

PCI Express Assign

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	EXPRESS CARD
2	LOM
3	NC
4	NC
5	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)

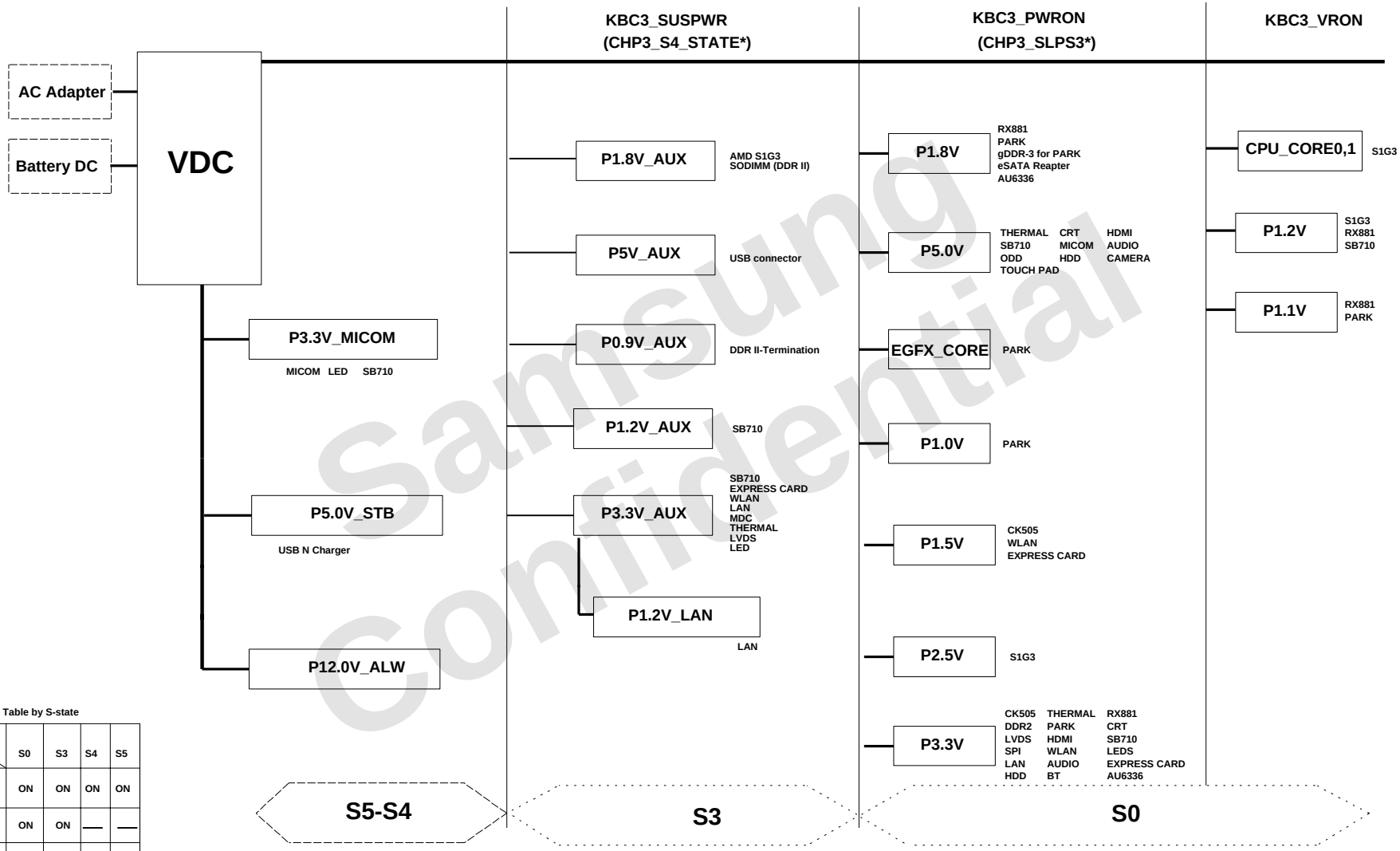
REVISION HISTORY

See rev notes for more information.

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 3 OF 58	

POWER DIAGRAM

Rev 0.1



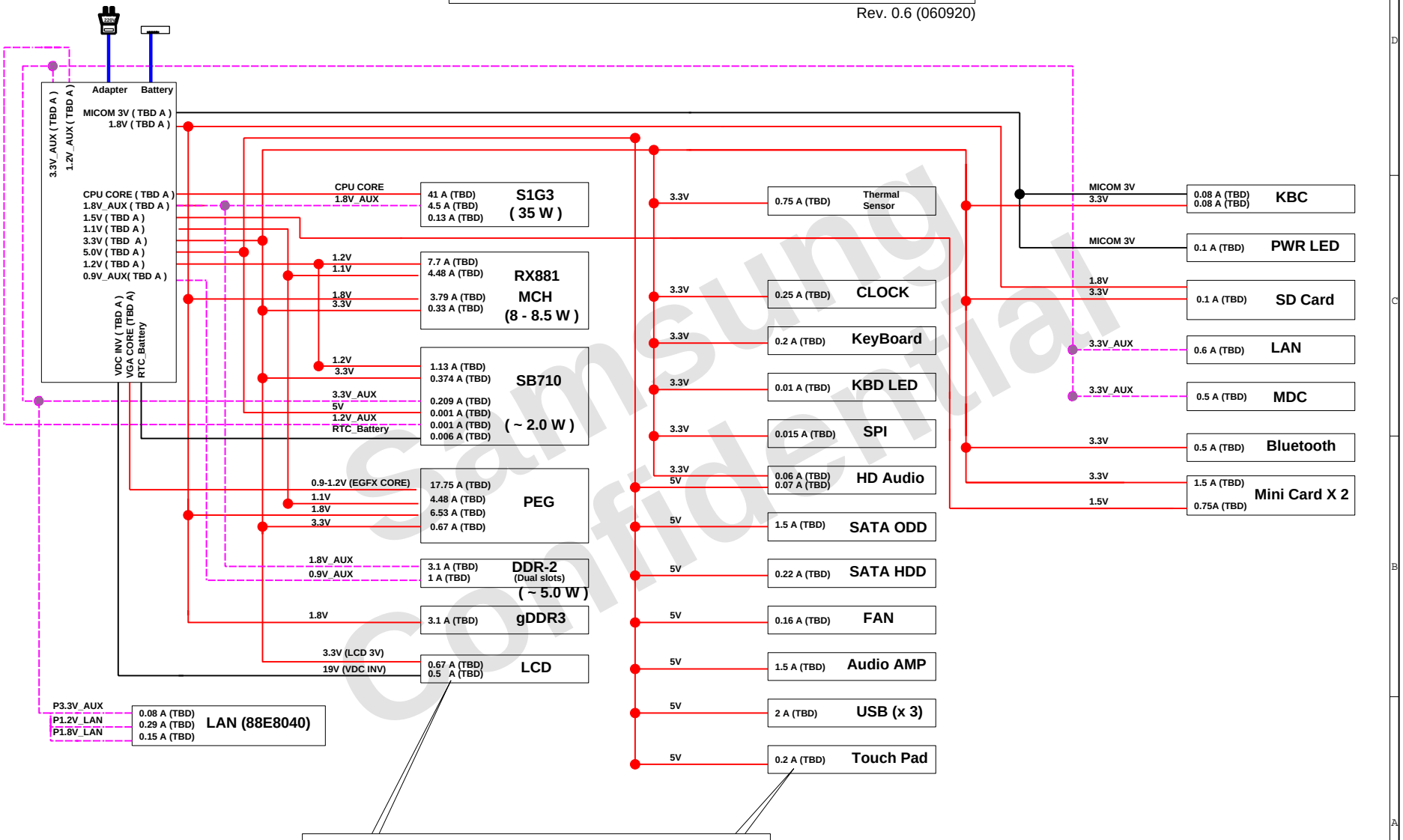
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 4 OF 58	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

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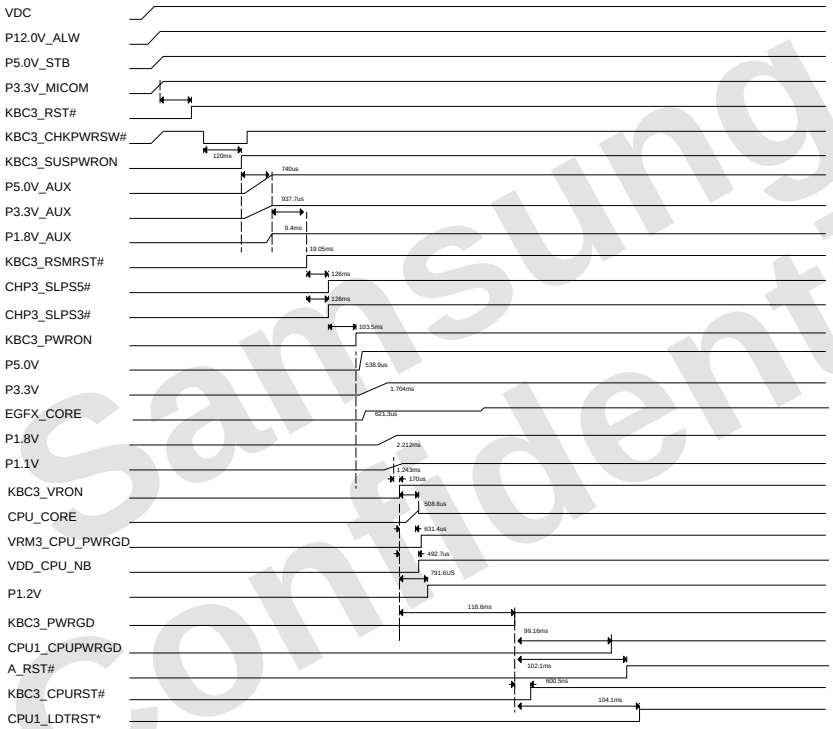
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 5 OF 58	

Timing Diagram, Power ON

Rev..1.0 2009-08-27



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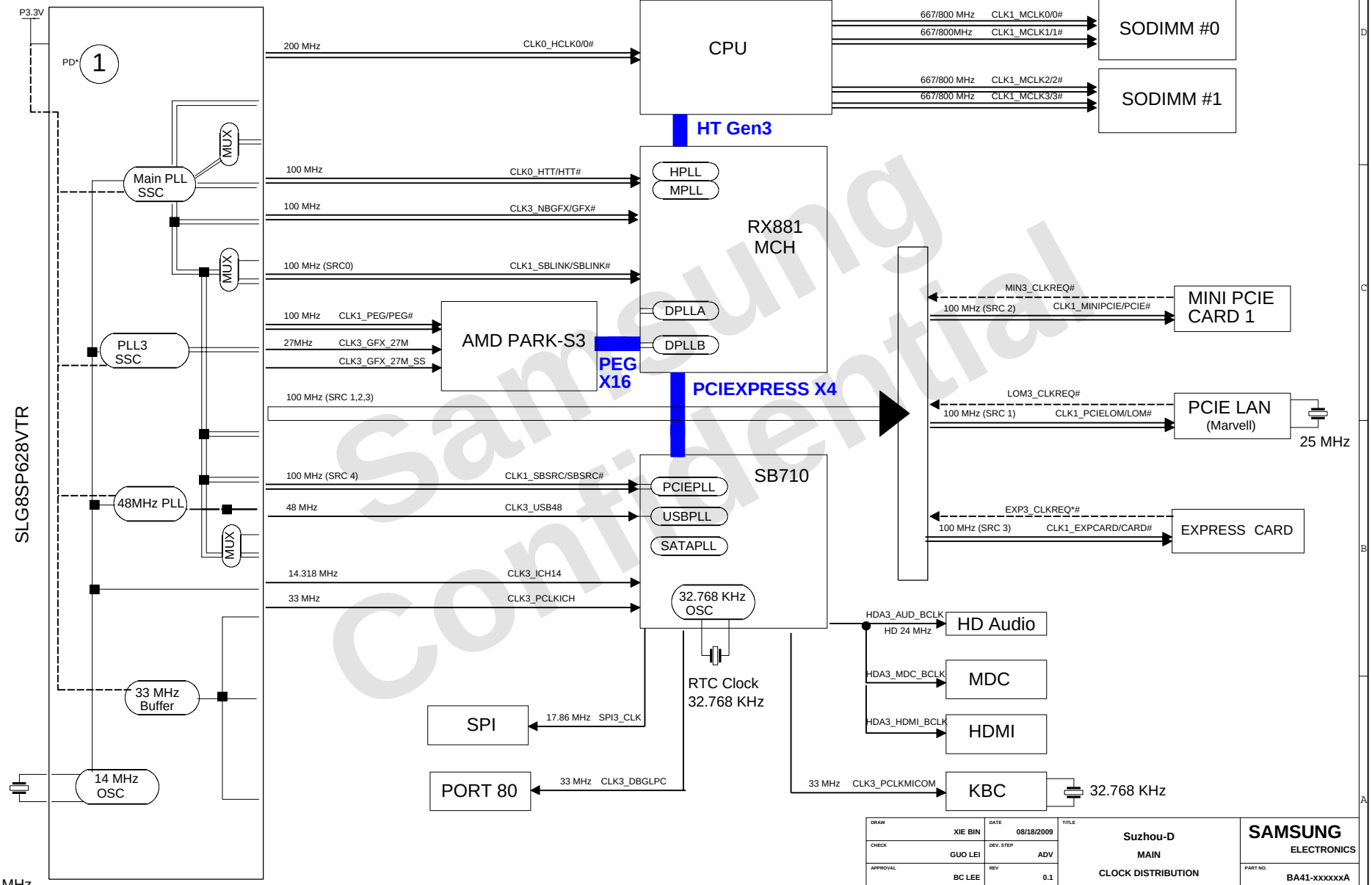
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 6 OF 58	

CLOCK DISTRIBUTION



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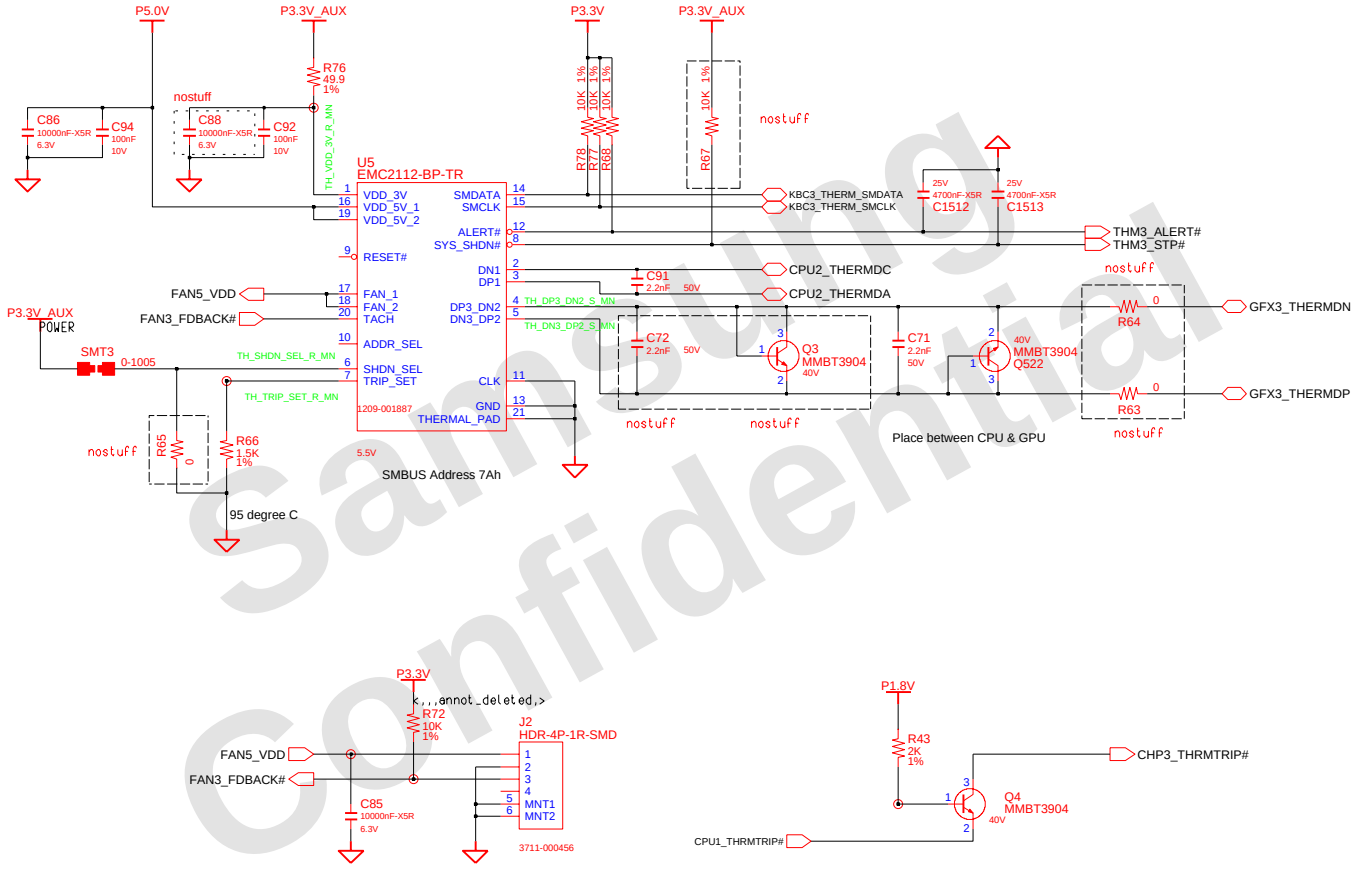
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 7 OF 58	

THERMAL SENSOR & FAN CONTROL

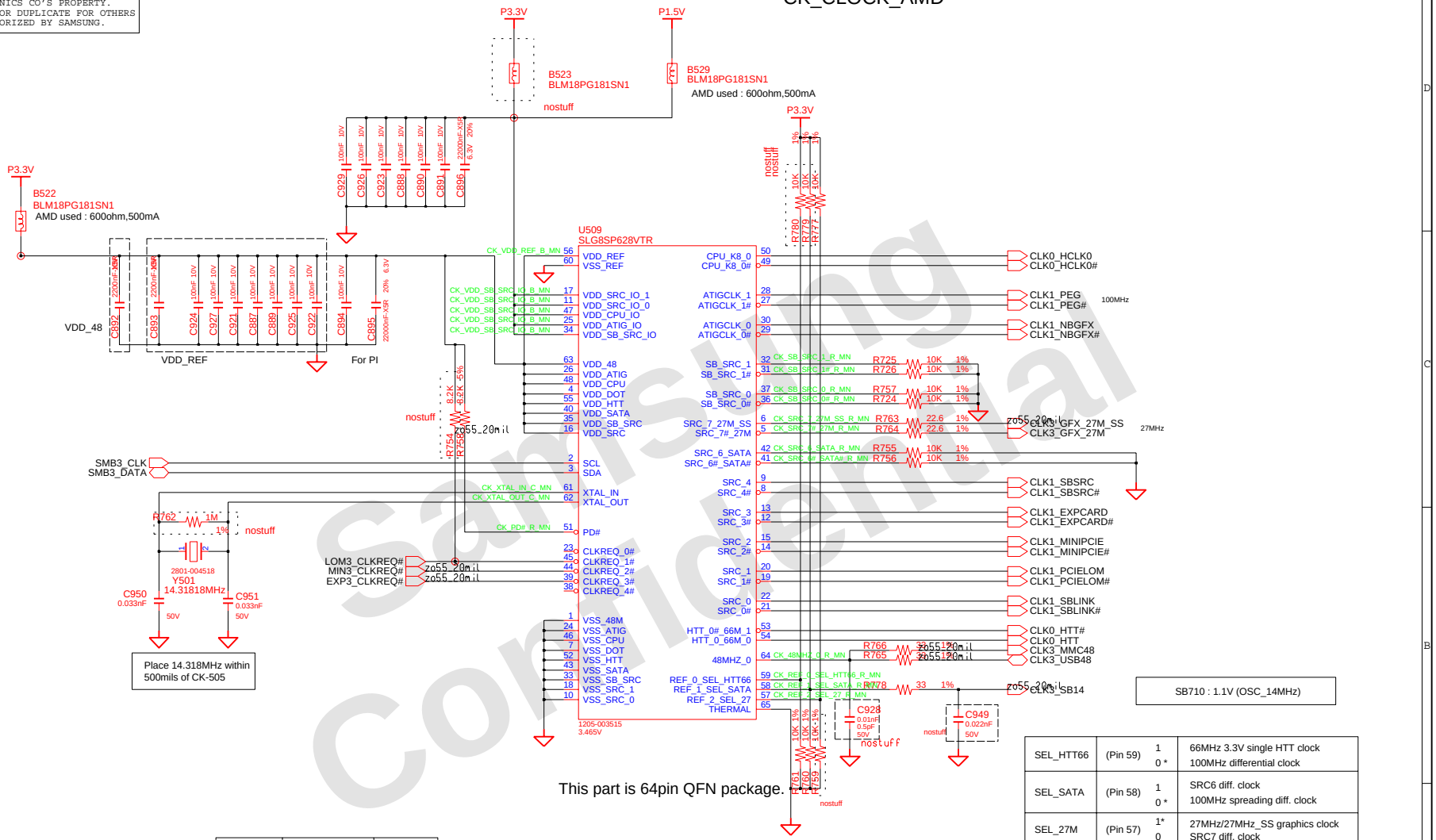


Line Width = 20 mil

SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D THERMAL SENSOR EMC2112	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 8 OF 58	

CK_CLOCK_AMD

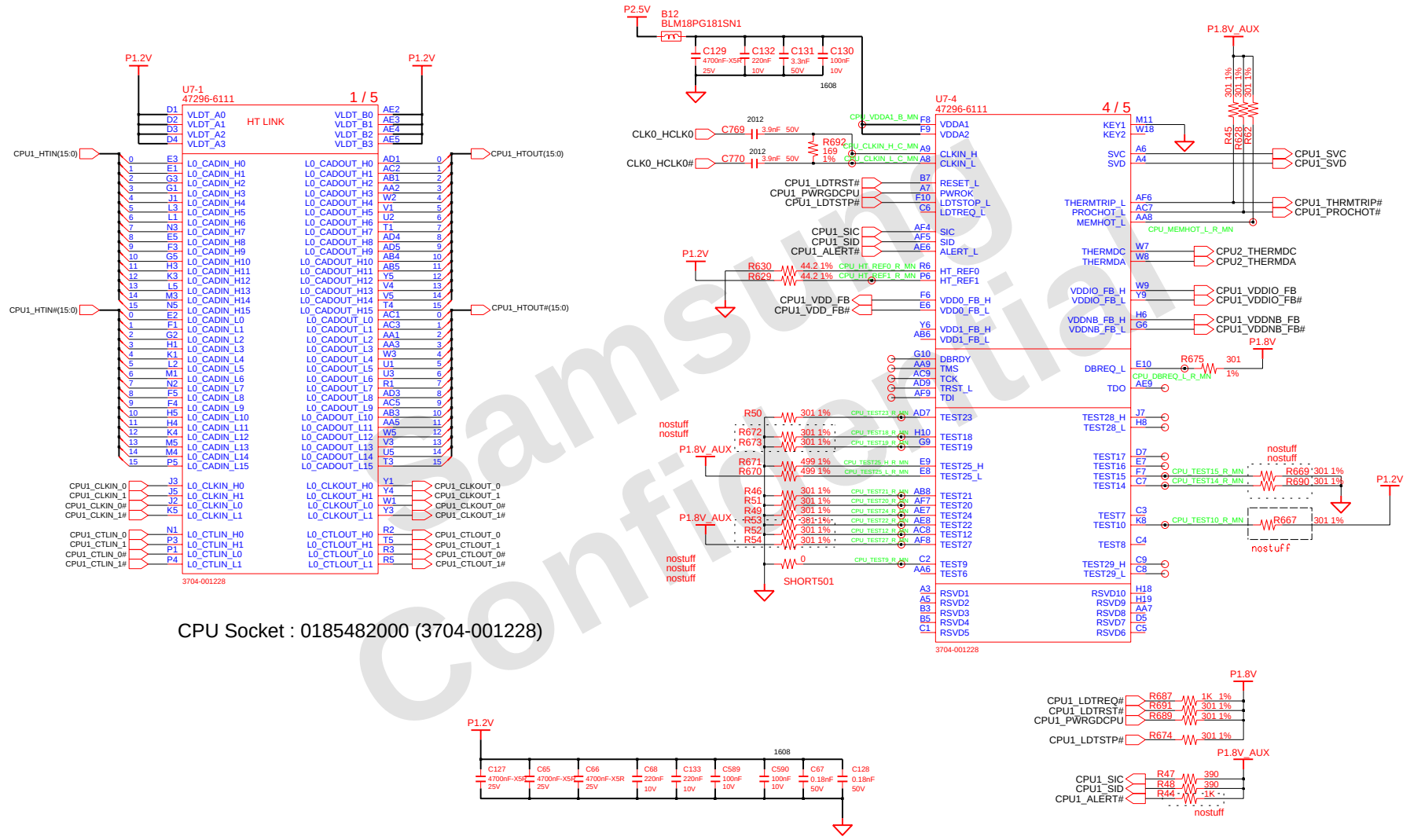


CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	EXP3_CLKREQ#	EXP CARD
CLK REQ 4	-	SB_SRC

SEL_HTT66	(Pin 59)	1 0 *	66MHz 3.3V single HTT clock 100MHz differential clock
SEL_SATA	(Pin 58)	1 0 *	SRC6 diff. clock 100MHz spreading diff. clock
SEL_27M	(Pin 57)	1* 0	27MHz/27MHz_SS graphics clock SRC7 diff. clock

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D Main_Clock_Circuit CK for AMD CPU	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 9 OF 58	

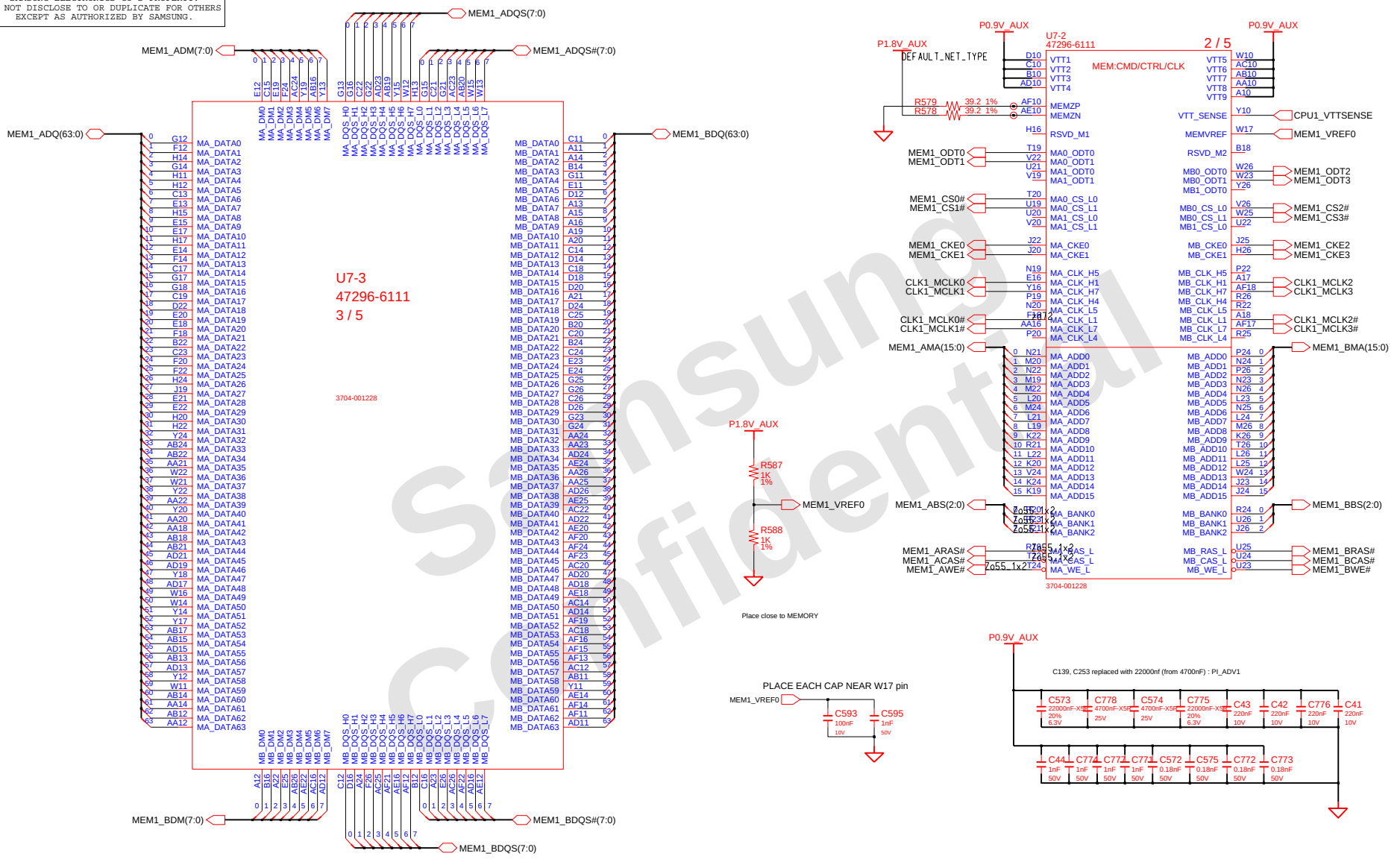
CPU_Caspian



CPU Socket : 0185482000 (3704-001228)

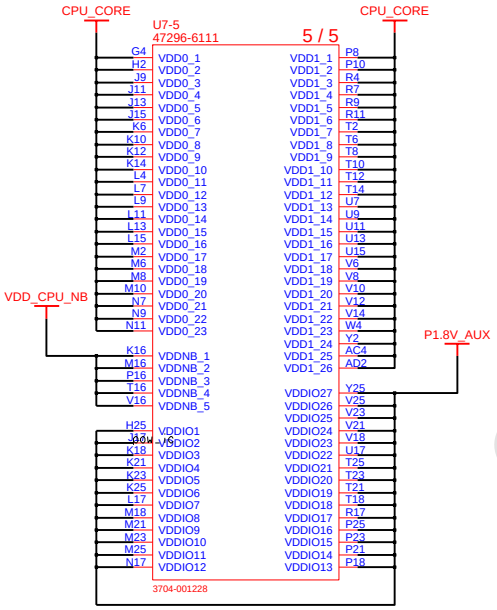
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D Caspian CPU S1G3 CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 10 OF 58	

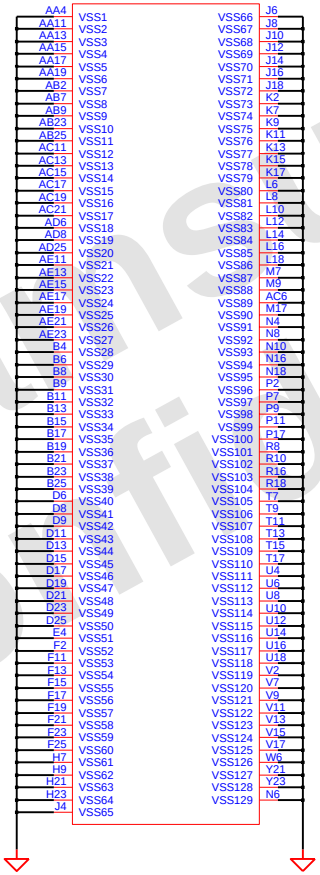
CPU_Caspian

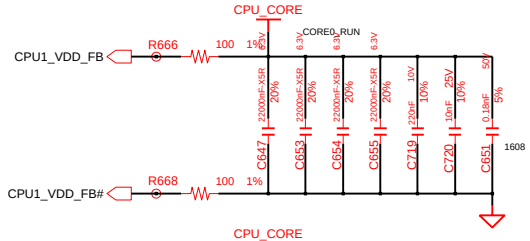


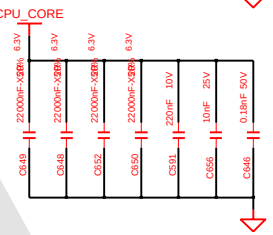
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / Caspian CPU / S1G3 CPU (2/3)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 11 OF 58	

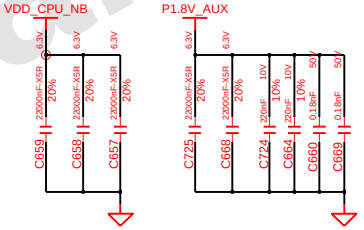
CPU_Caspian



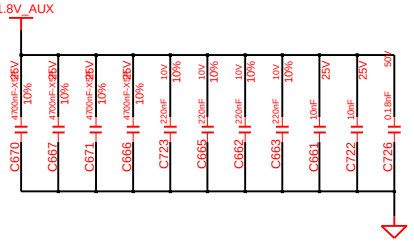






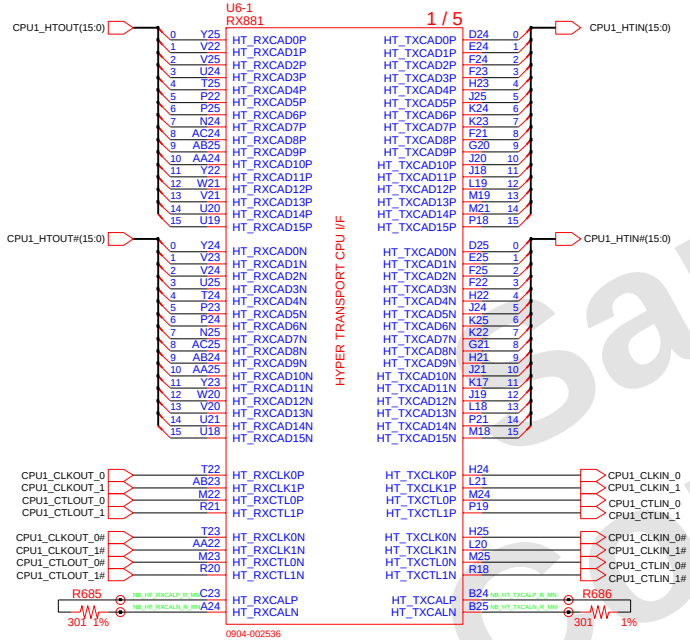


Decoupling between processor and Memory
Place close to processor as possible

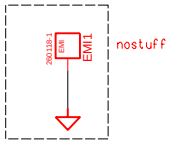


DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D Caspian CPU S1G3 CPU (3/3)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 12 OF 58	

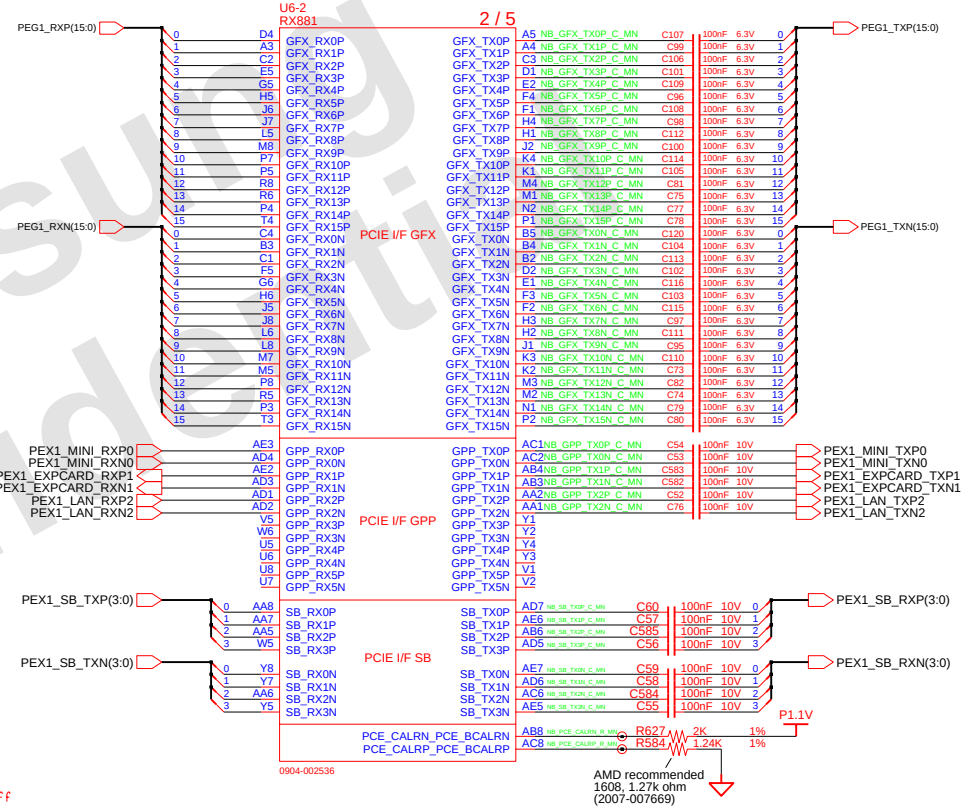
NB_ RX881_AMD



* Hyper Transport Calibration resistors
RS780M / RX781 : 301 ohm
RX780 / RD780 : 1.21K ohm (for S3 issue in D/T chipset)



Place near MCH & Heatsink



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MCH RX881 (1/3)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
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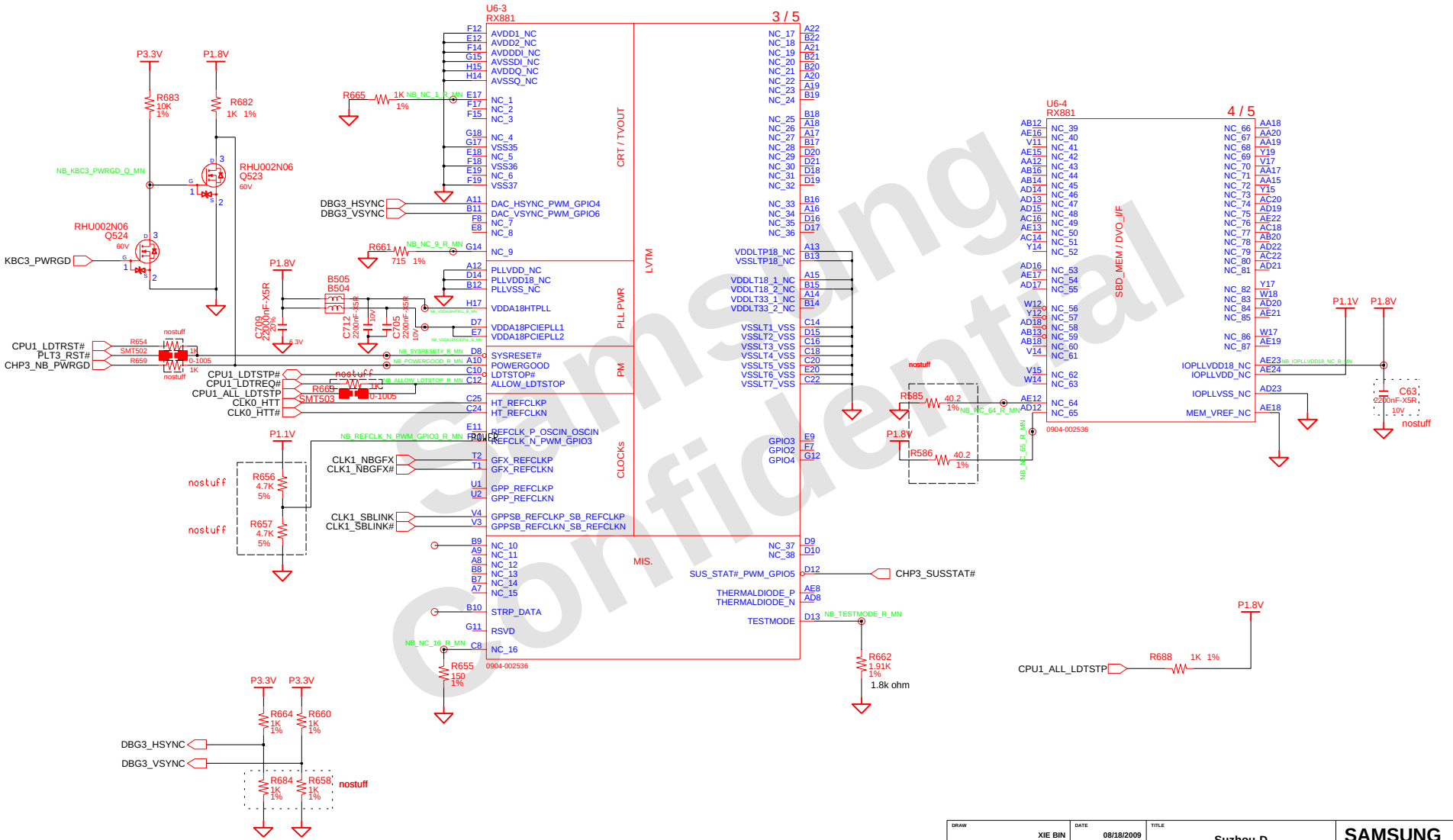
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 13 OF 58	

NB_ RX881_AMD



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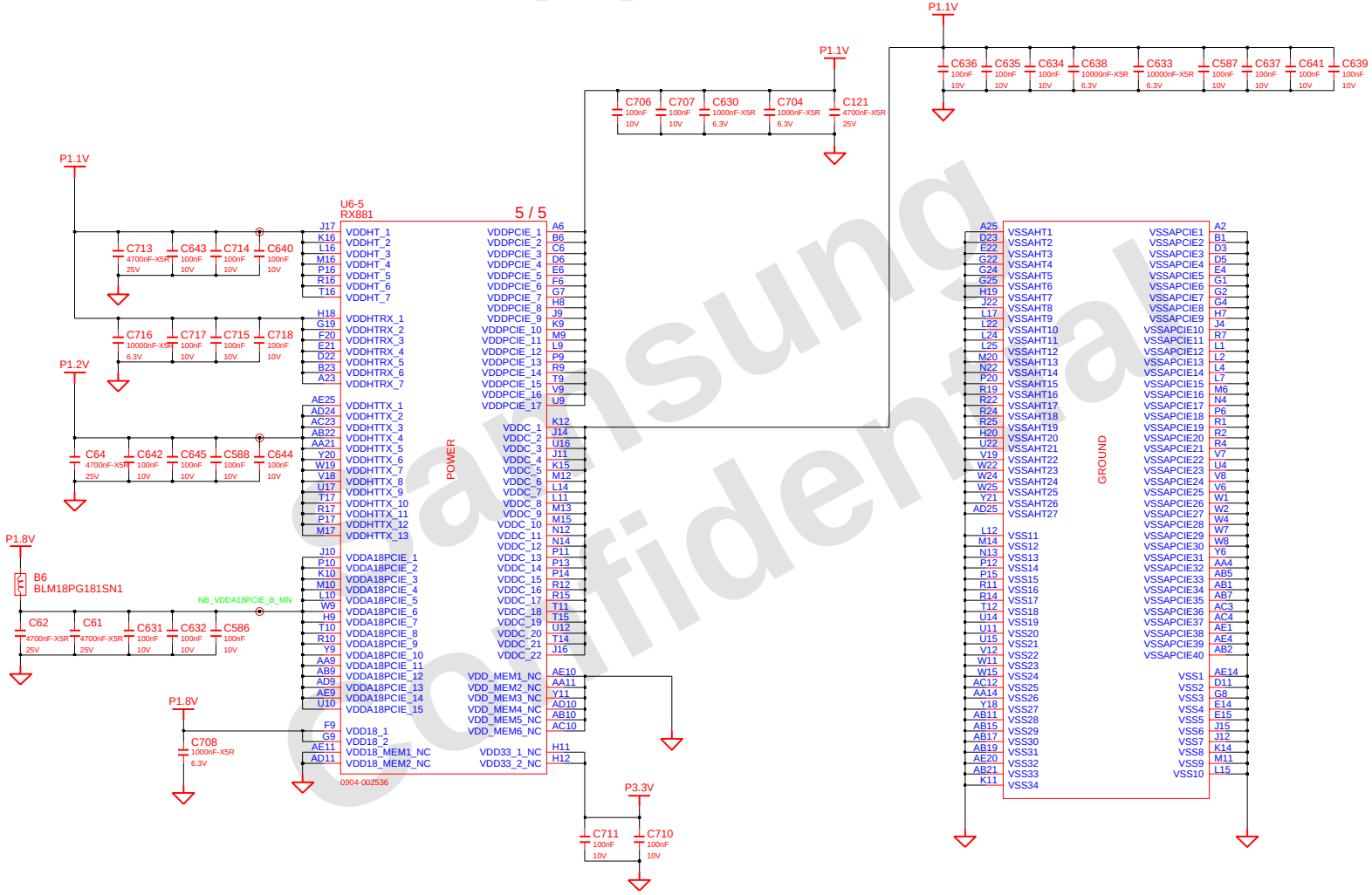
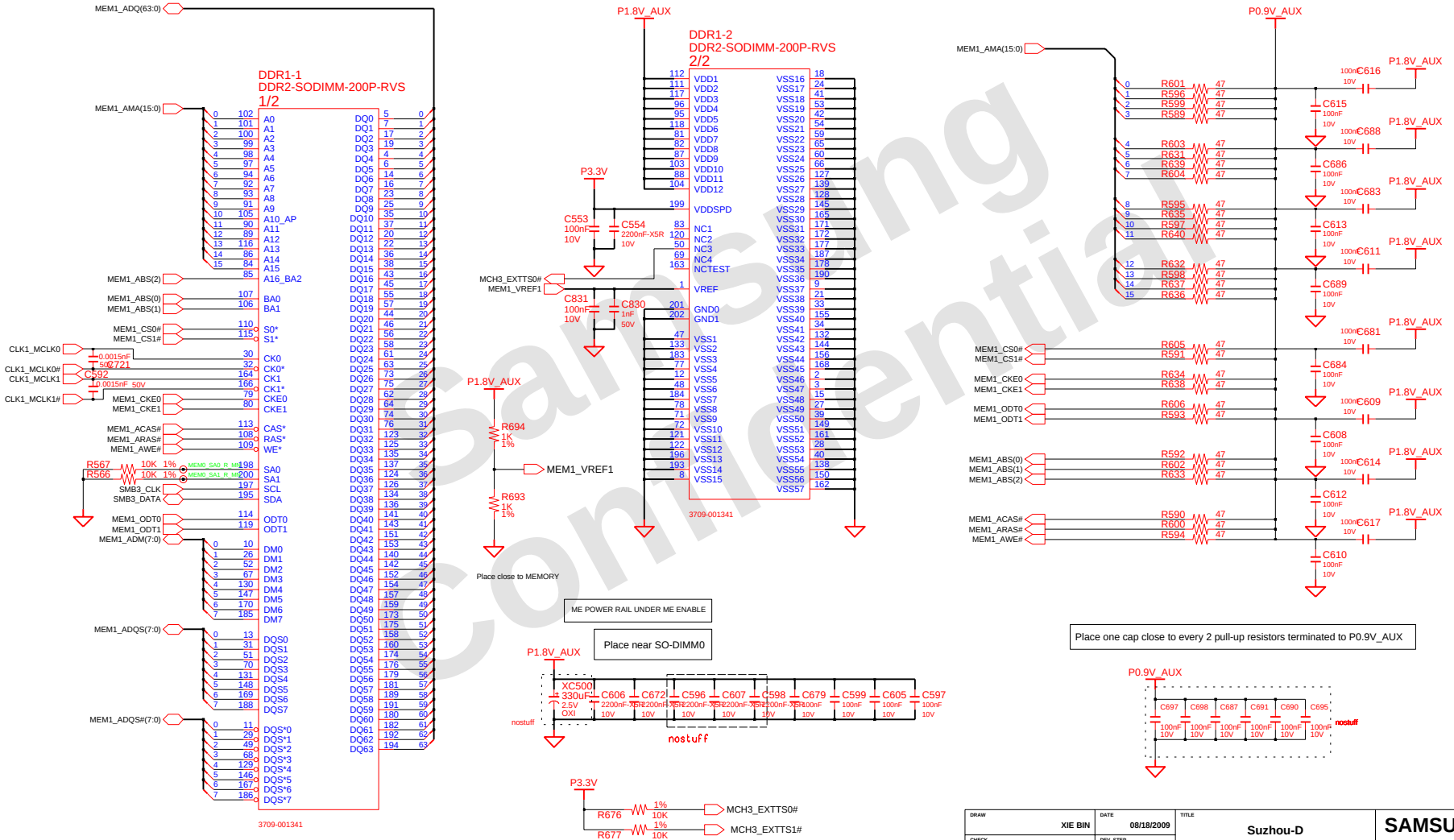
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 14 OF 58	

NB_ RX881_AMD



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / MCH / RX881 (3/3)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 15 OF 58	

DDR SO-DIMM #0



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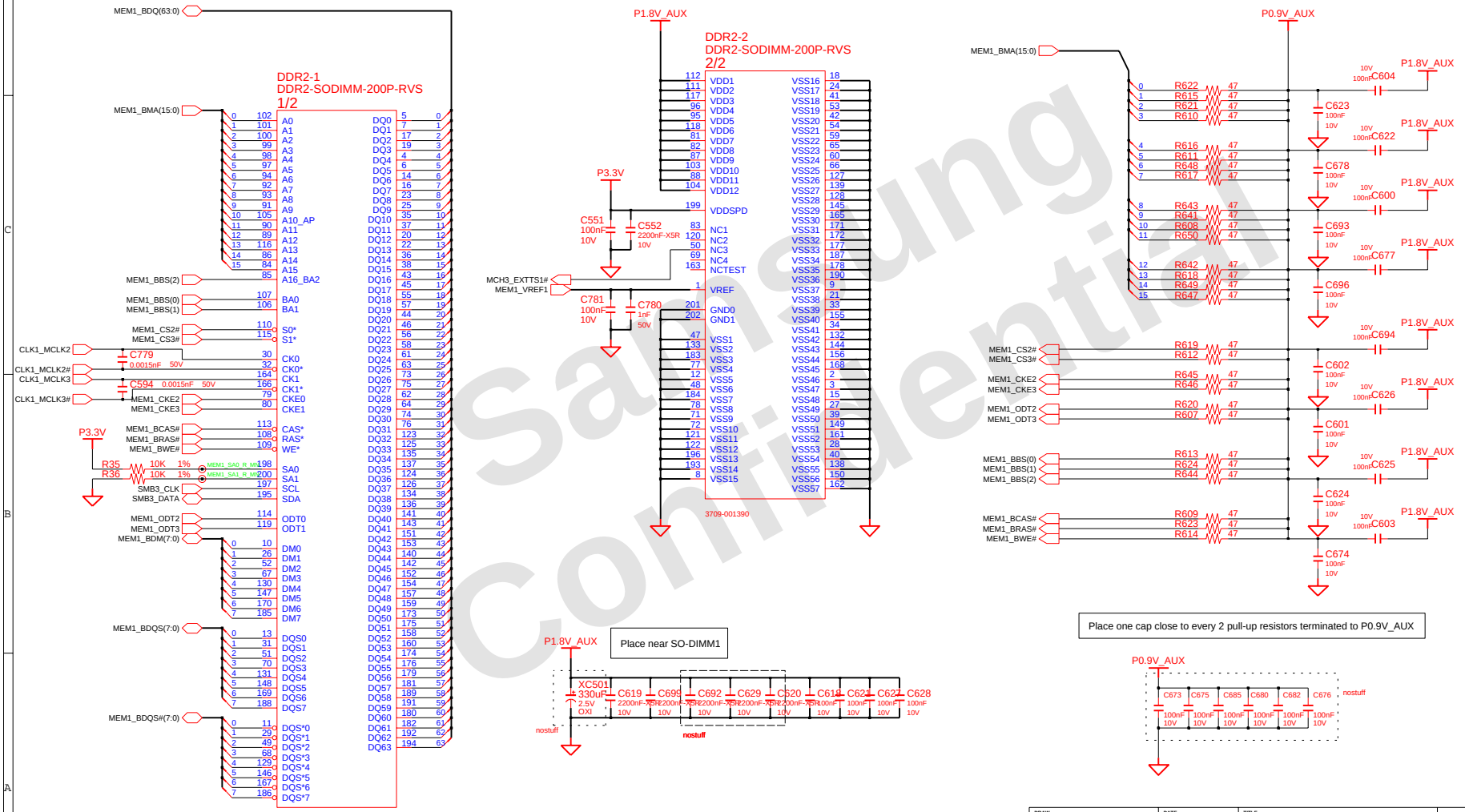
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 16 OF 58	

DDR SO-DIMM #1



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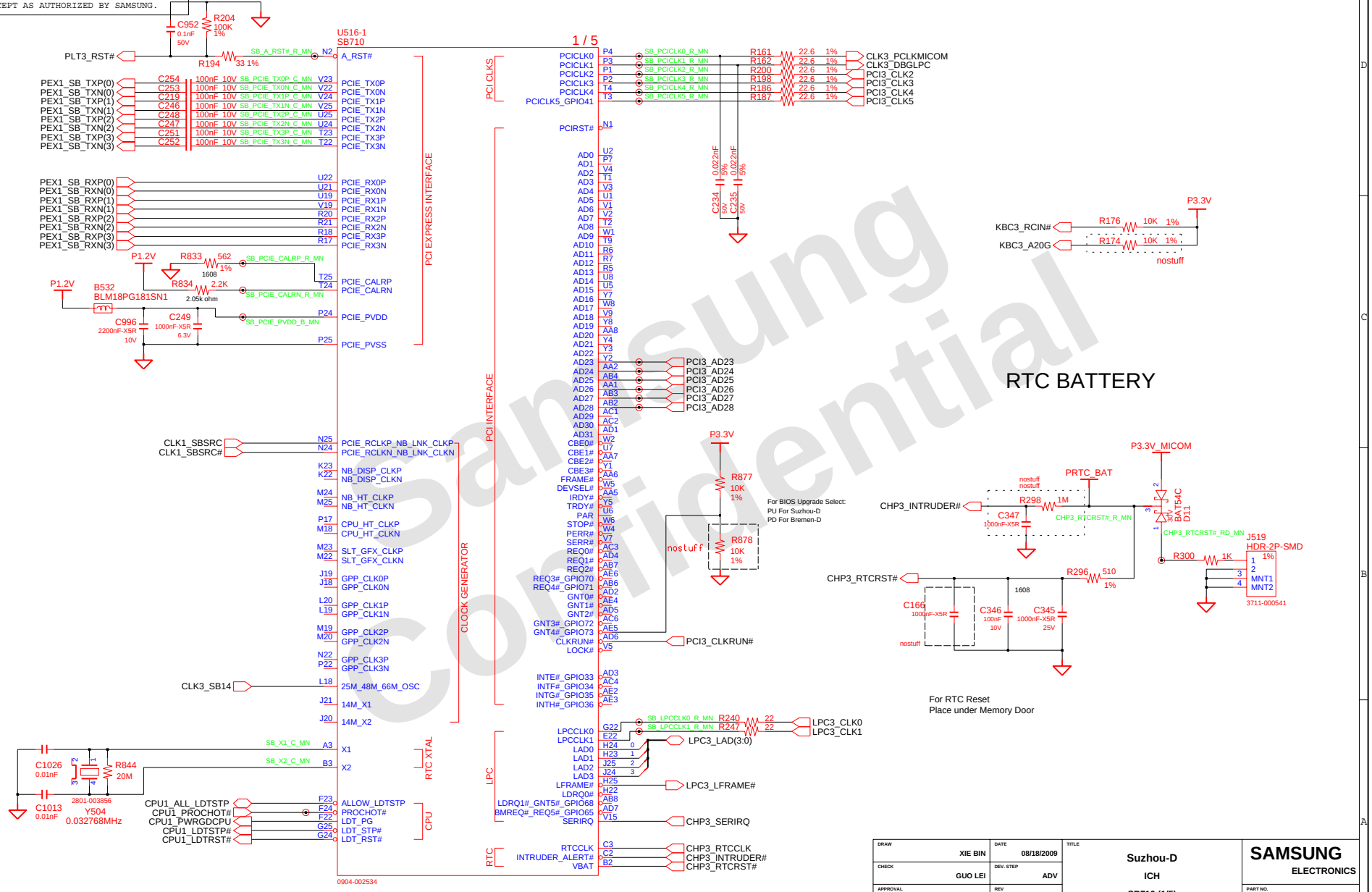
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 17 OF 58	

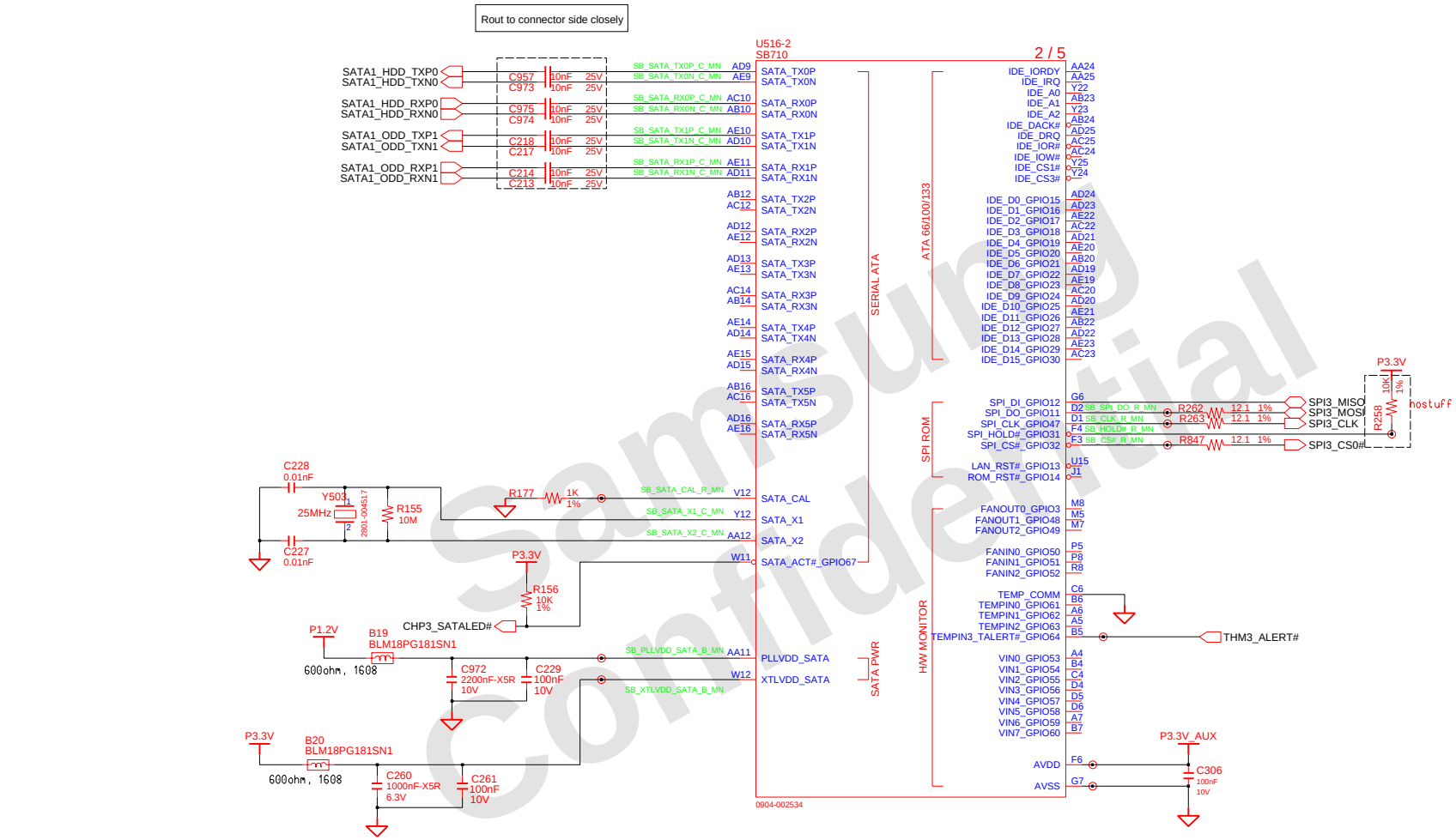
SB_710_AMD



RTC BATTERY

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D ICH SB710 (1/5)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 18 OF 58	

SB_710_AMD



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CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 19 OF 58	

SB_710_AMD

USB1, 6 : Right Port
USB0 : Left Port
USB5 : Bluetooth
USB8 : Camera
USB4 : 3-in-1
USB2 : eSATA

BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD
(Put it a debugger connector)

PU : No Reboot Mode

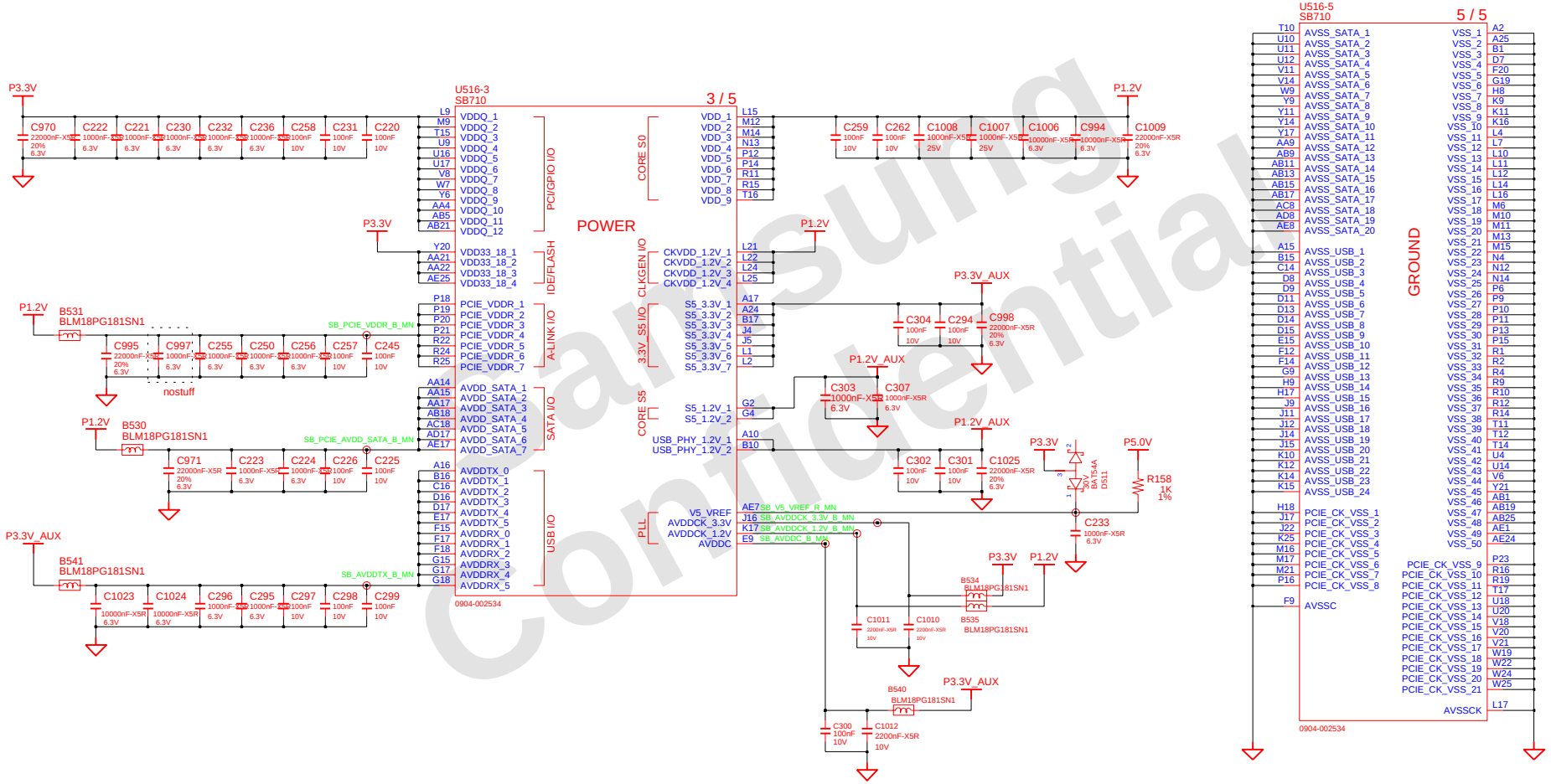
U516-4
SB710

4 / 5

DRAW	XIE BIN
DATE	08/18/2009
CHECK	GUO LEI
DEV. STEP	ADV
APPROVAL	BC LEE
REV	0.1
MODULE CODE	
LAST EDIT	July 15, 2009 19:25:13 PM
TITLE	Suzhou-D ICH SB710 (3/5)
	SAMSUNG ELECTRONICS
PART NO.	BA41-xxxxxxA
PAGE	20 OF 58

D:/Users/mentor/Suzhou-D/Suzhou-D_adv1_0826

SB_710_AMD



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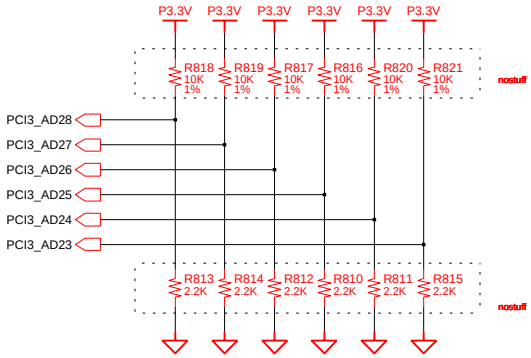
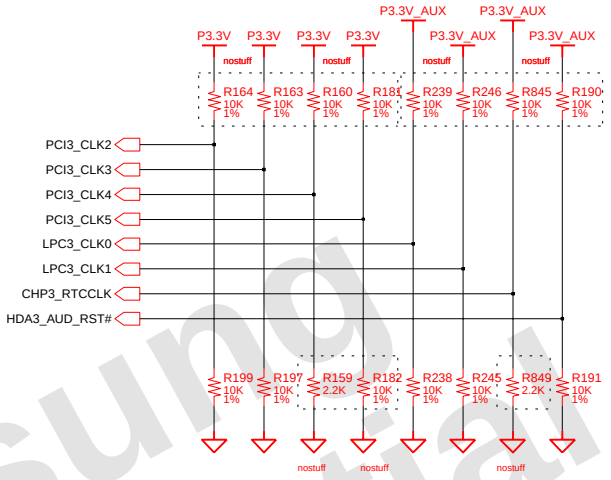
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 21 OF 58	

Strap

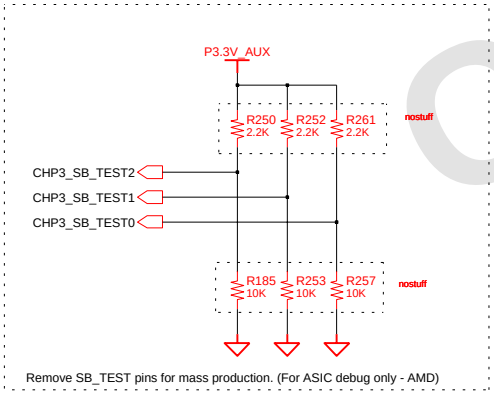


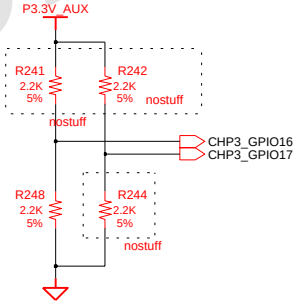


DEBUG STRAPS

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



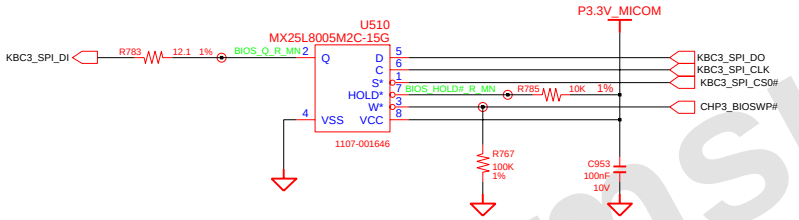


GPIO17	GPIO16

ROM TYPE
NC, NC = RSVD
NC, L = SPI ROM
L, NC = LPC ROM
L, L = FWH ROM

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / ICH / SB710 Strap(5/5)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 22 OF 58	

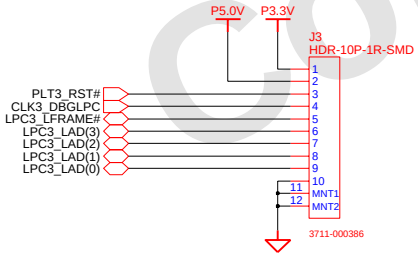
SPI_BIOS_ROM



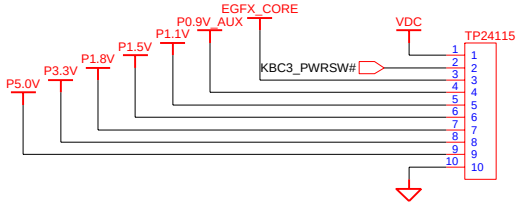
1MB(8MBit)

02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
WITH INITIAL POST VALUE	8A INIT.EXTENDED BIOS DATA AREA
14 INIT. KEYBOARD CONTROLLER	8C INIT. FDD CONTROLLER
16 CHECK CHECKSUM	9A SHADOW OPTION ROMS
18 8254 TIMER INIT.	9C SETUP POWER MANAGEMENT
1A 8237 DMA CONTROLLER INIT.	9E ENABLE H/W INTERRUPT
1C RESET INTERRUP CONTROLLER	A0 SET TIME OF DAY
20 TEST DRAM REFRESH	A4 INIT. TYPEMATIC RATE
22 TEST 8742 KEYBOARD CONTROLLER	A8 ERASE F2 PROMPT
24 SET ES SEGMENT REG. TO 4GB	AA SCAN FOR F2 KEY STROKE
26 ENABLE A20	AC ENTER SETUP
28 AUTO SIZING DRAM	AE CLEAR IN POST FLAG
32 COMPUTE THE CPU SPEED	B0 CHECK FOR ERRORS
34 TESET CMOS RAM	B2 POST DONE-PREPARE TO BOOT O/S
38 SHADOW SYSTEM BIOS ROM	B4 ONE BEEP
3A AUTO SIZING CACHE	B6 CHECK PASSWORD (OPTION)
3C CONFIGURE ADVANCED CHIPSET REG.	B7 ACPI INIT
3D LOAD ALTER REG. WITH CMOS VALUE	BA DMI INIT
42 INIT. INTERRUPT VECTOR	BE CLEAR SCREEN
44 INIT. BIOS INTERRUPT	C0 TRY BOOT WITH INT19
46 CHECK ROM COPYRIGHT NOTICE	D0 INTERRUPT HANDLER ERROR
47 INIT. I20 SUPPORT IF INSTALLED	D2 UNKNOWN INTERRUPT ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D4 PENDING INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D6 SHUTDOWN 5
4A INIT. ALL VIDEO BIOS ROM	D8 SHUTDOWN ERROR
4C SHADOW VIDEO BIOS ROM	DA EXTENDED BLOCK MOVE
50 DISPLAY CPU TYPE AND SPEED	DC SHUTDOWN 10
52 TEST KEYBOARD	89 ENABLE NMI
54 SET KEYCLICK IF ENABLED	90 INIT. HDD CONTROLLER
56 ENABLE KEYBOARD	91 INIT. LOCAL BUS HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	92 JUMP TO USER PATCH 2
5A DISPLAY " PRESS ..... SETUP"	94 DISABLE A20 ADDRESS LINE
5C TEST RAM GETWEEN 512K AND 640K	96 CLEAR HUGE ES SEGMENT REG.
60 TEST EXTENDED MEMORY	98 SEARCH FOR OPTION ROMS
62 TEST EXTENDED MEMORY ADDRESS LINE	
64 JUMP TO USER PATCH 1	

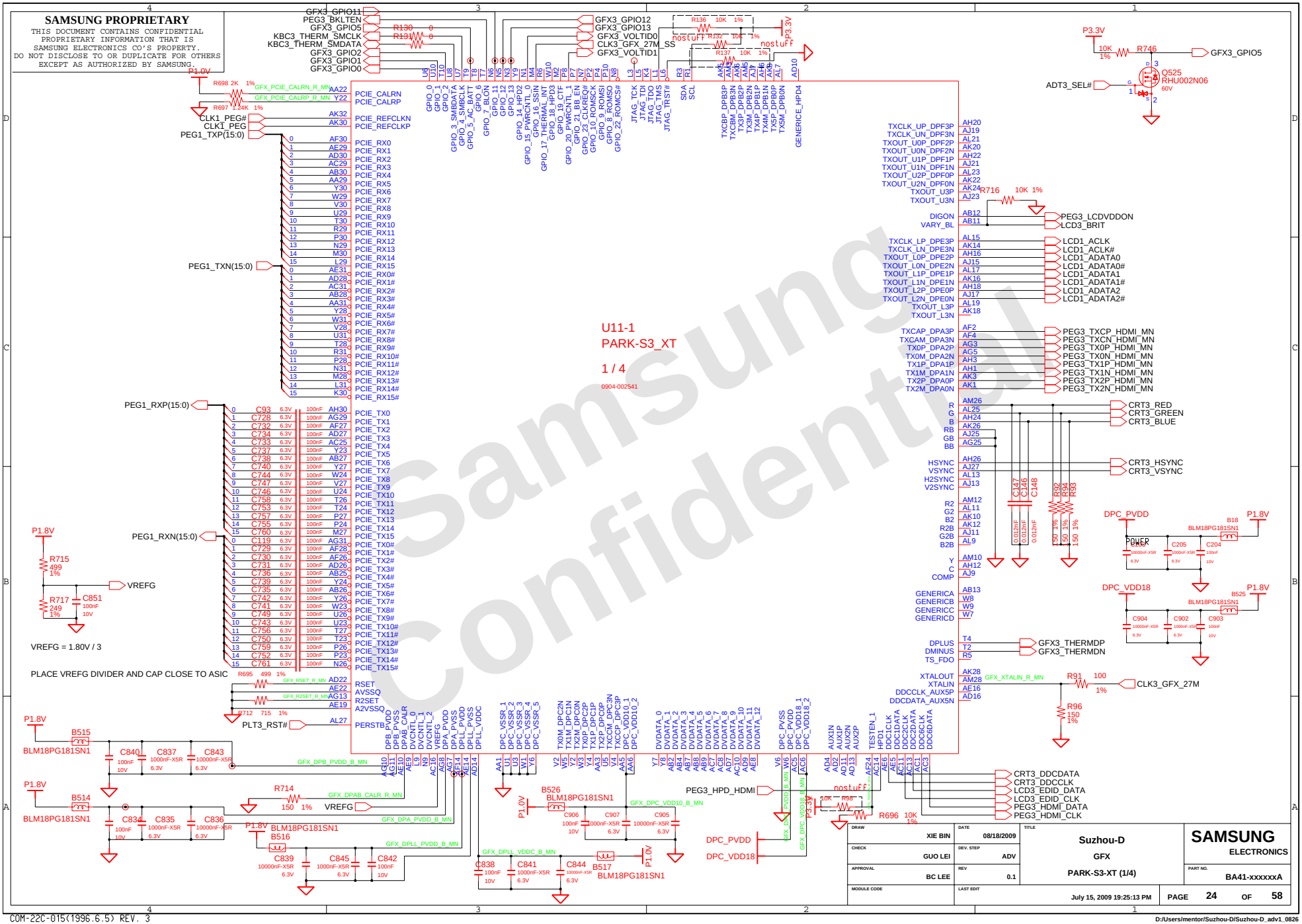
80H DECODER CONNECTOR

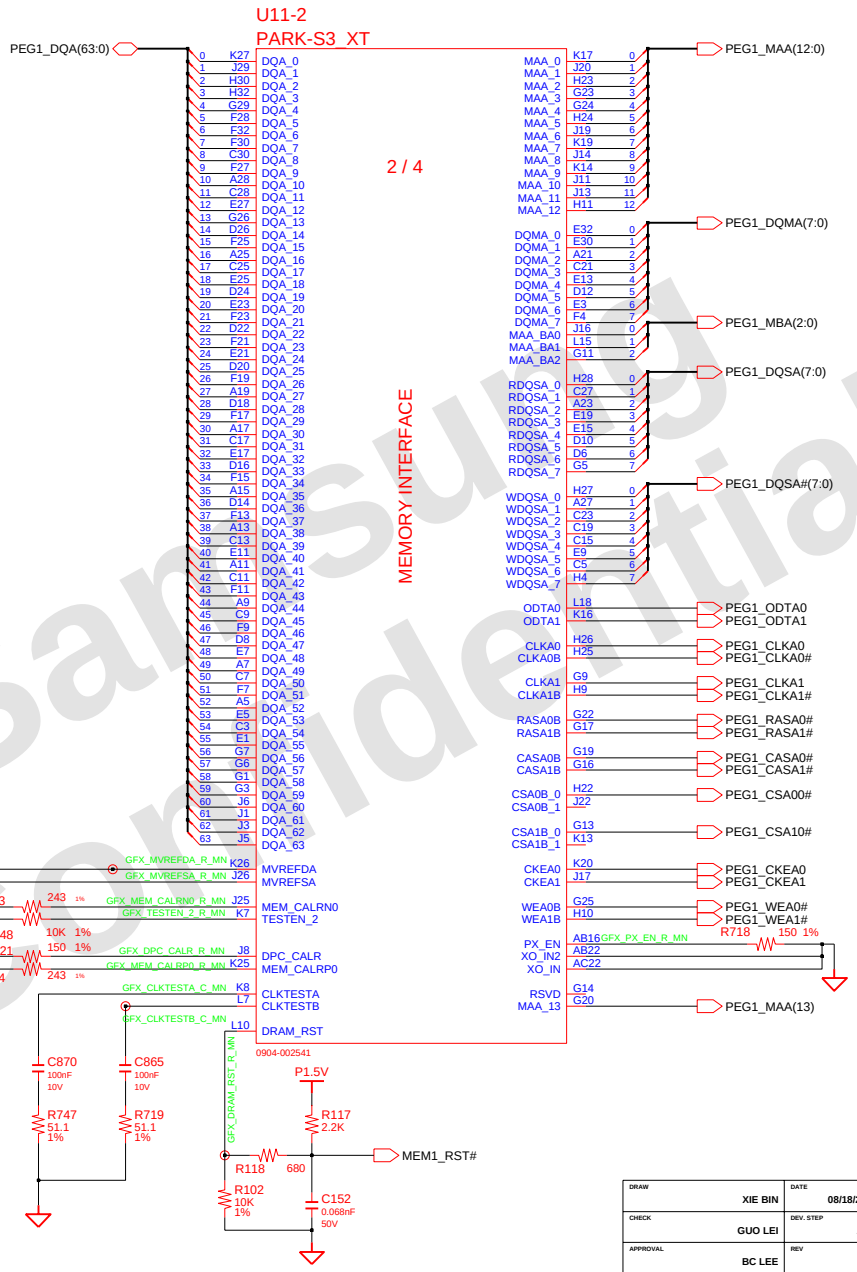


ICT FREE

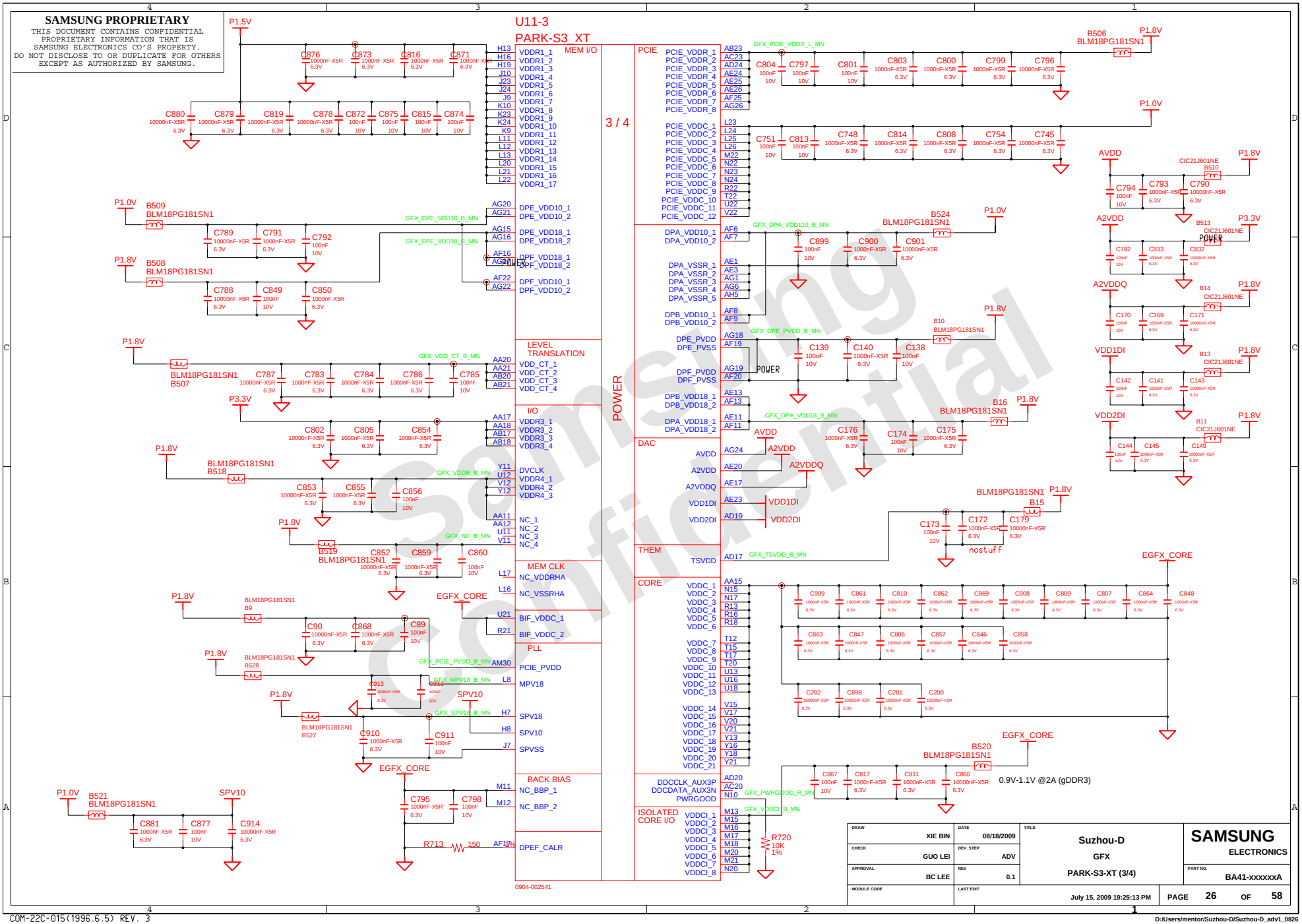


DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	SPI_BIOS_ROM	
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 23 OF 58	

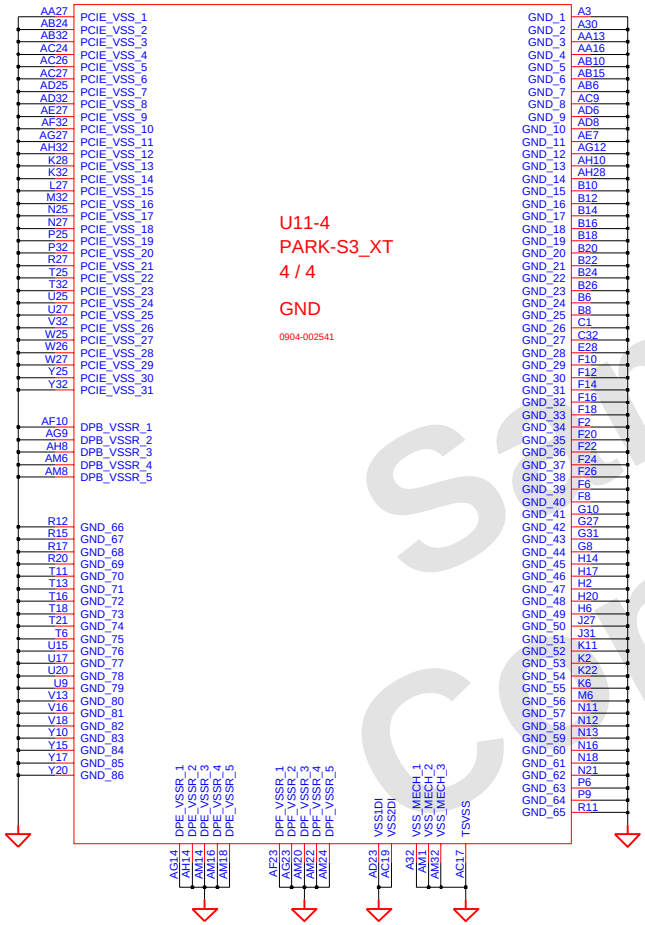


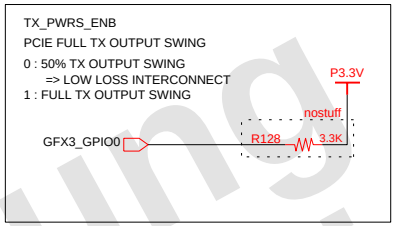


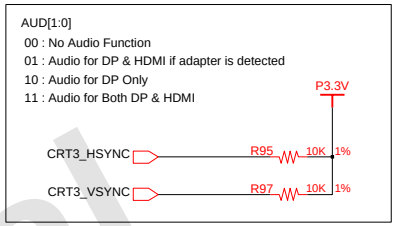
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / GFX / PARK-S3-XT (2/4)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 25 OF 58	

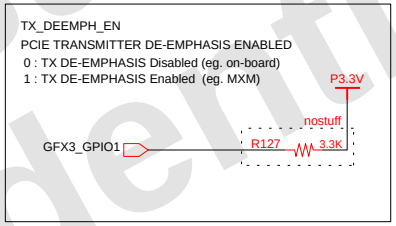


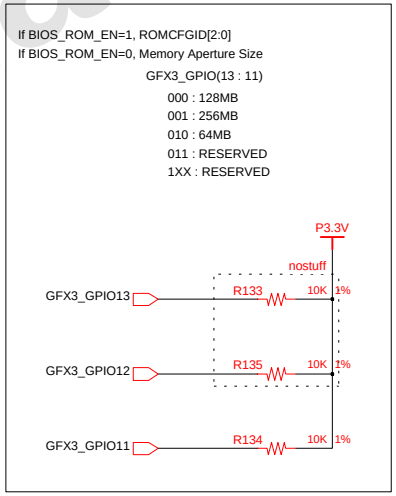
PARK Straps

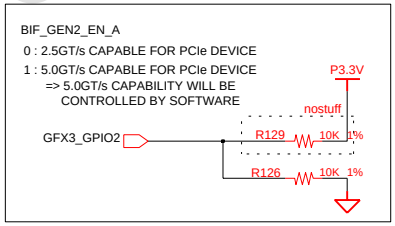






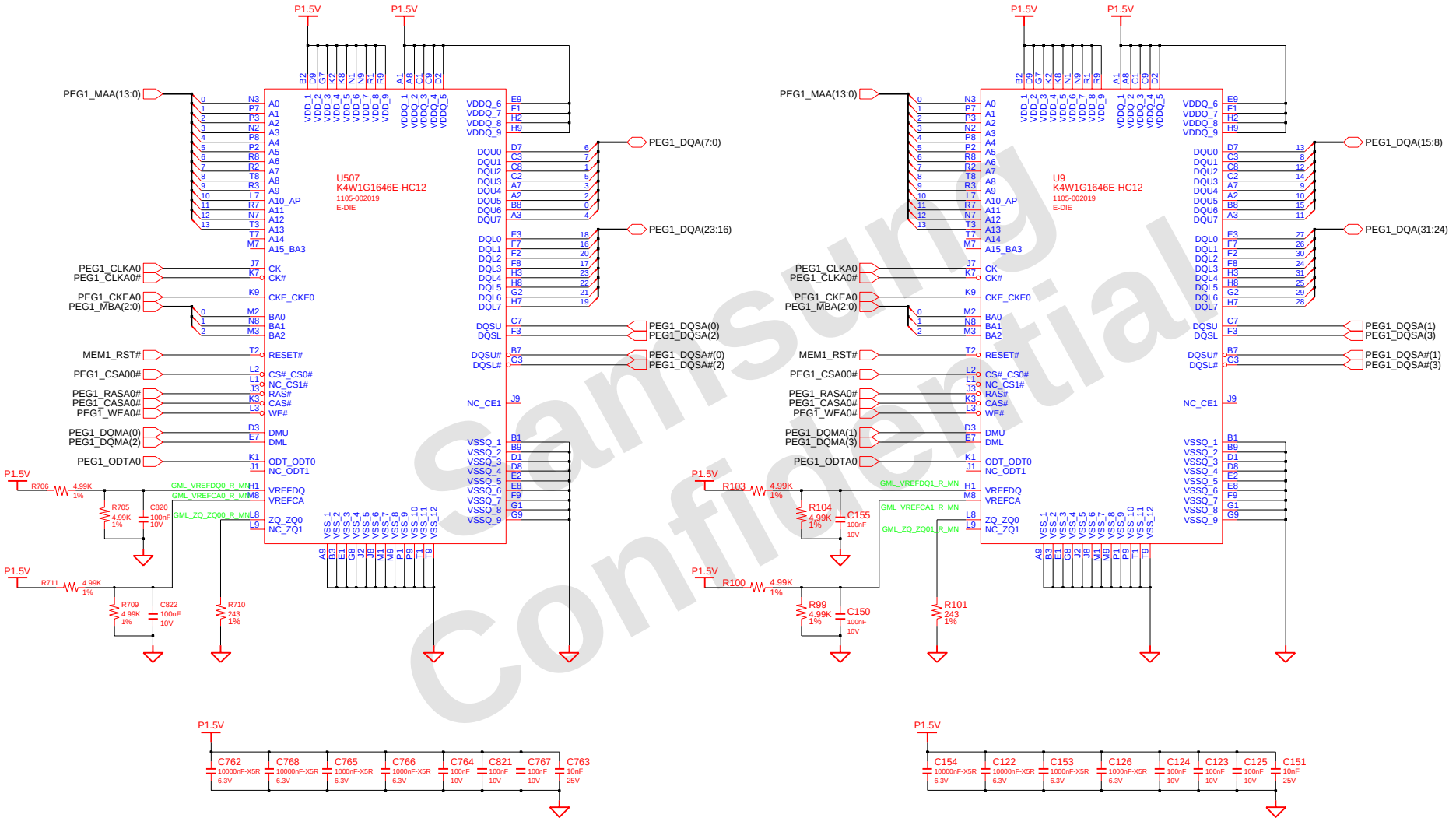






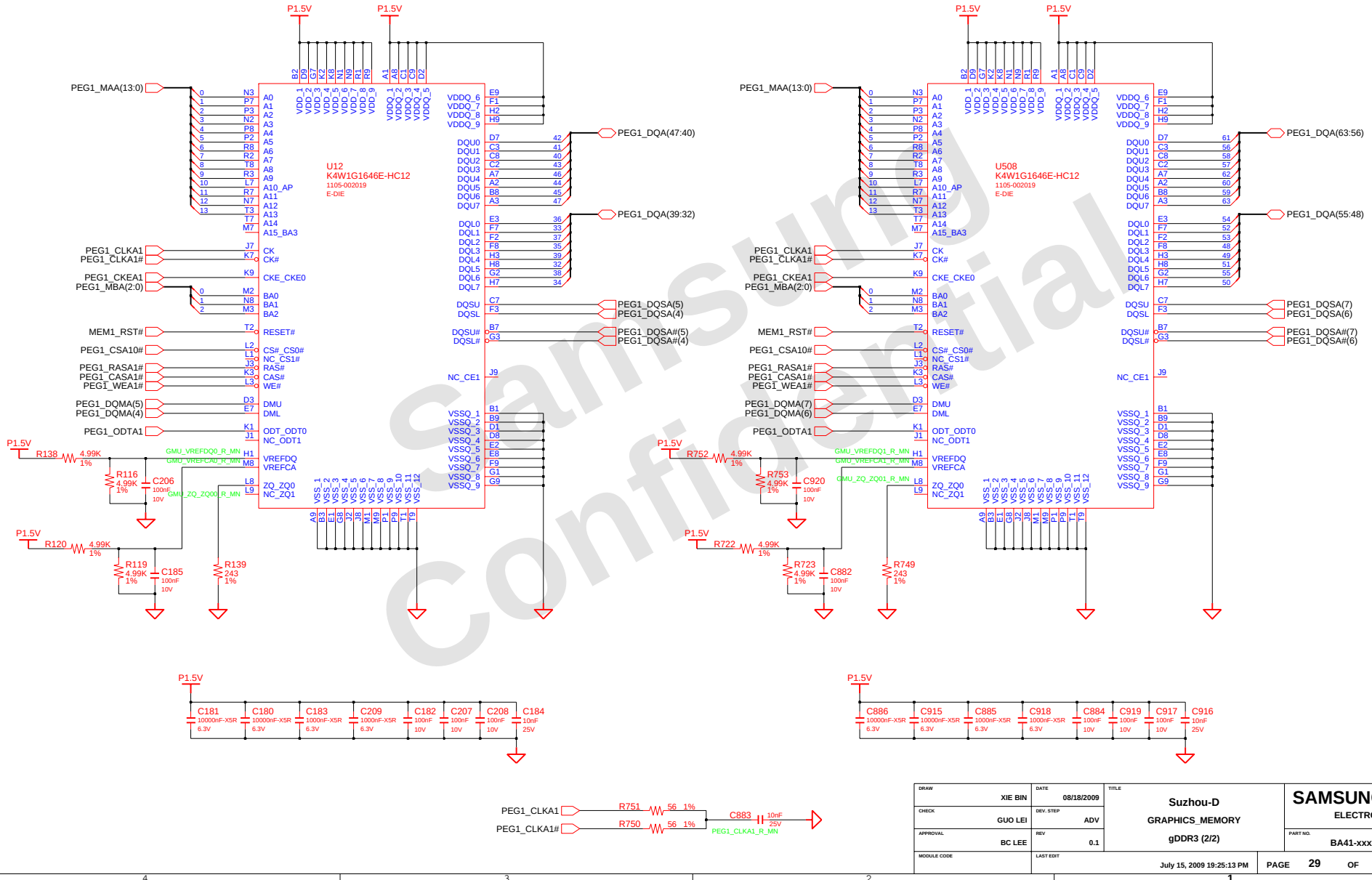
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / GFX / PARK-S3-XT (4/4)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 27 OF 58	

A-channel Lower Data



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D GRAPHICS_MEMORY gDDR3 (1/2)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 28 OF 58	

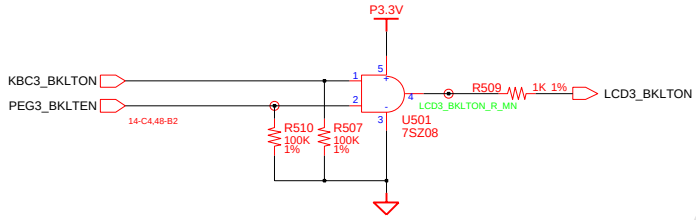
A-channel Upper Data



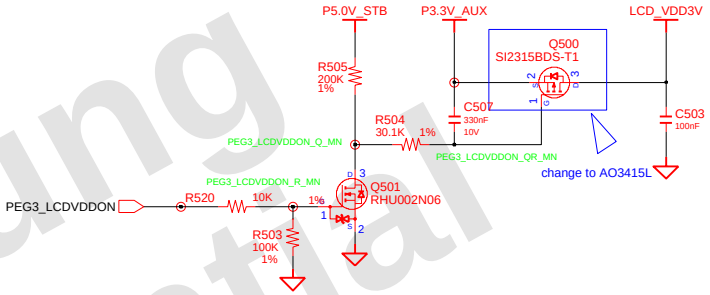
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D GRAPHICS_MEMORY gDDR3 (2/2)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 29 OF 58	

LVDS

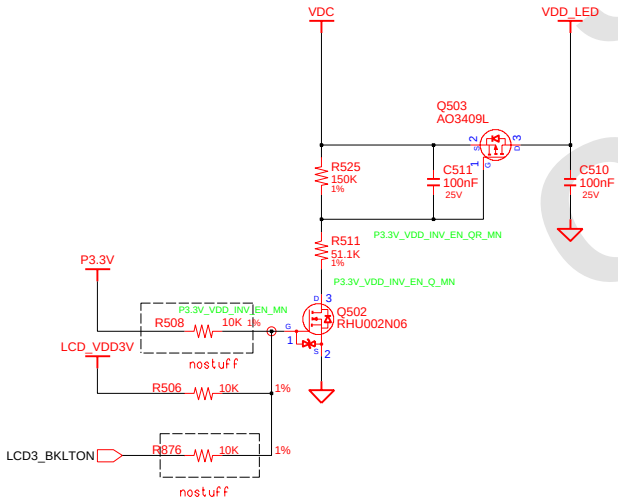
Backlight On



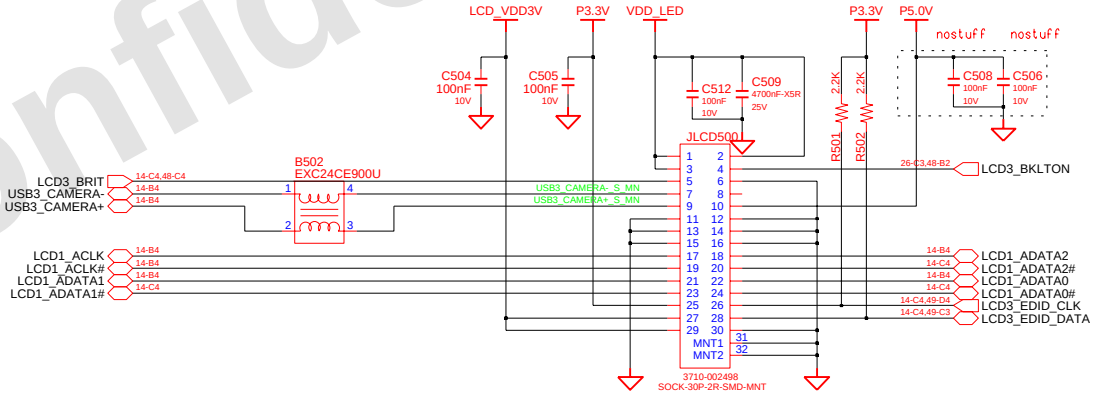
LCD Power EBL Purpose



Converter Power

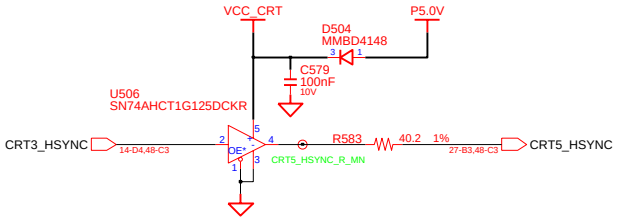


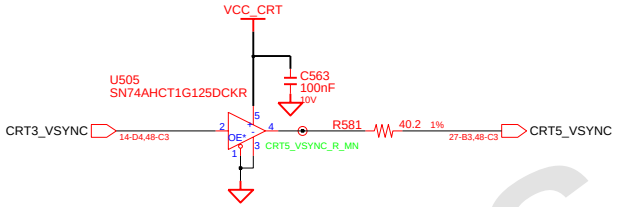
Camera + LCD Connector

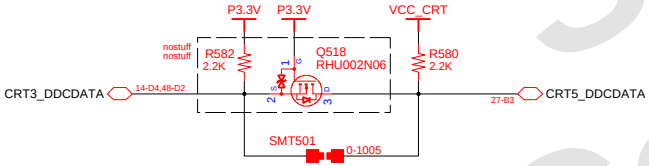


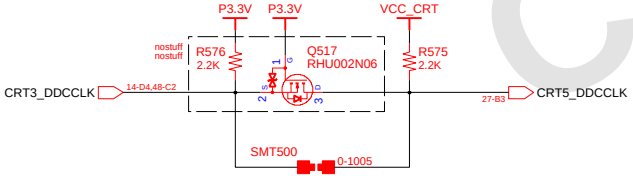
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1	GRAPHICS_IF (1/2)	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 30 OF 58	

CRT

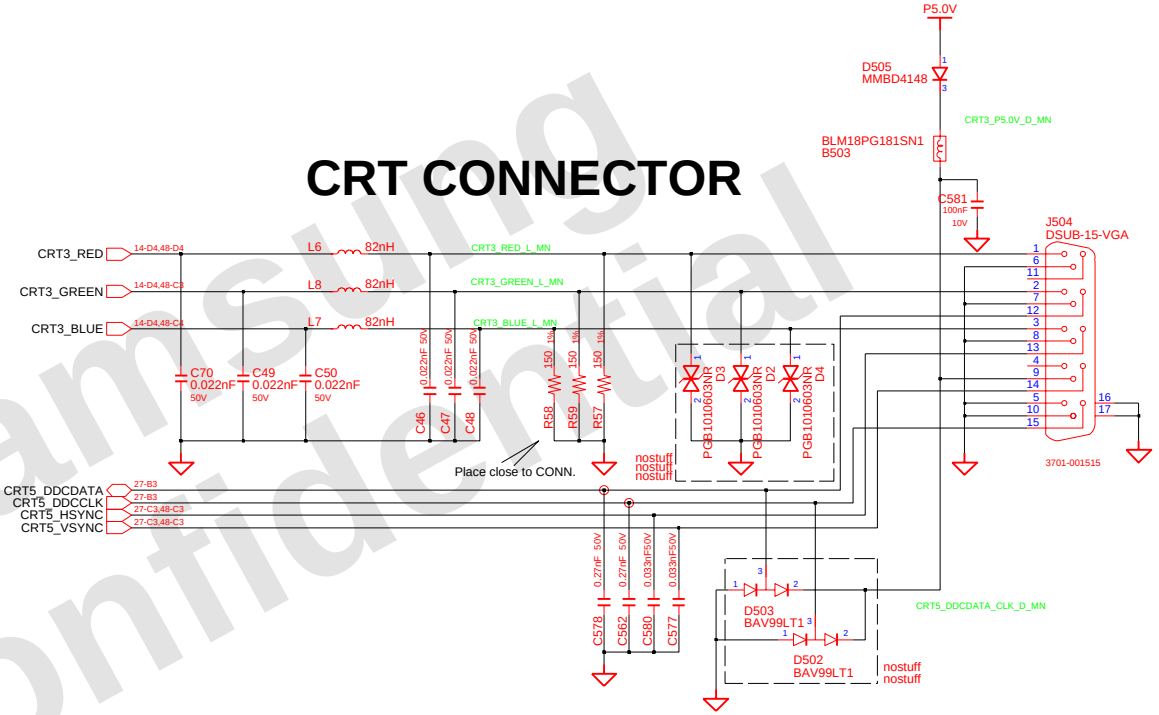








CRT CONNECTOR

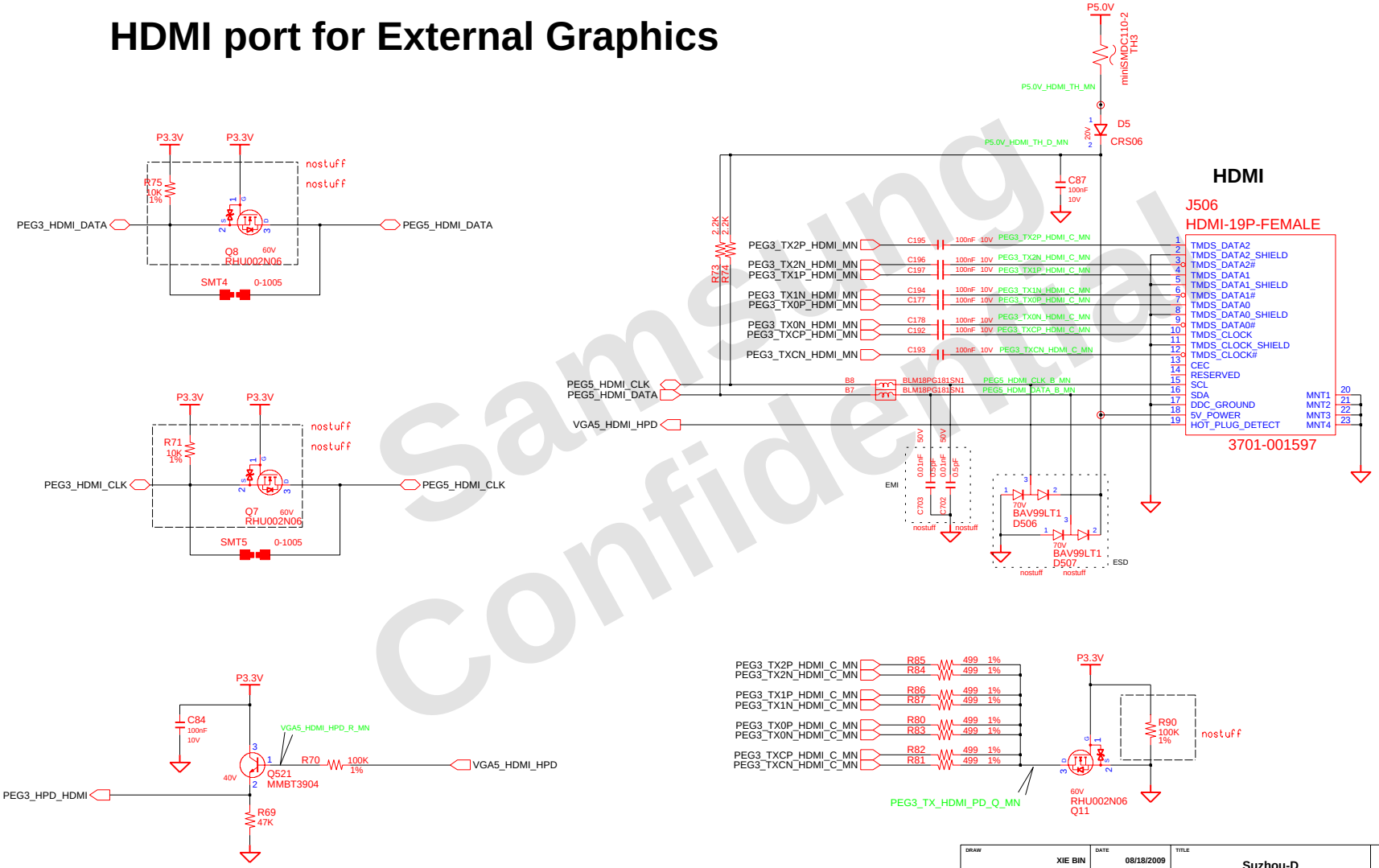


Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1	GRAPHICS_IF (2/2)	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 31 OF 58	

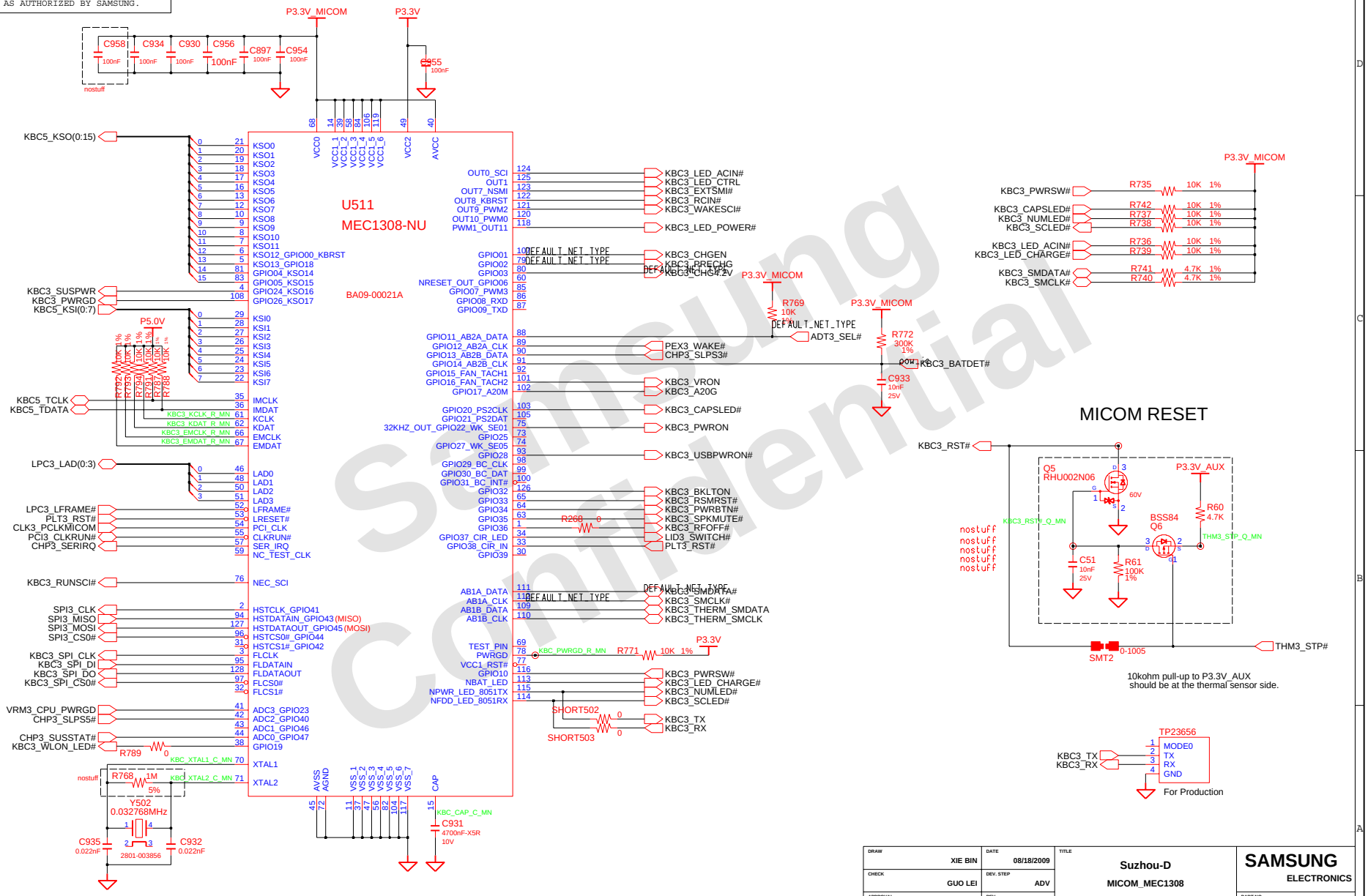
HDMI

HDMI port for External Graphics



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 32 OF 58	

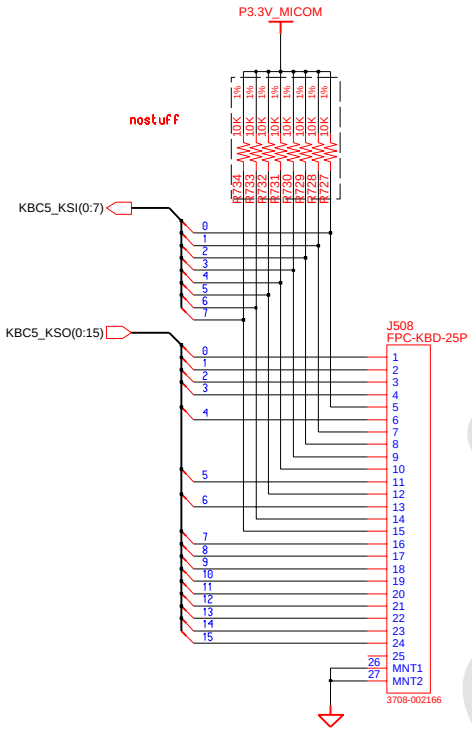
MICOM_MEC1308-NU



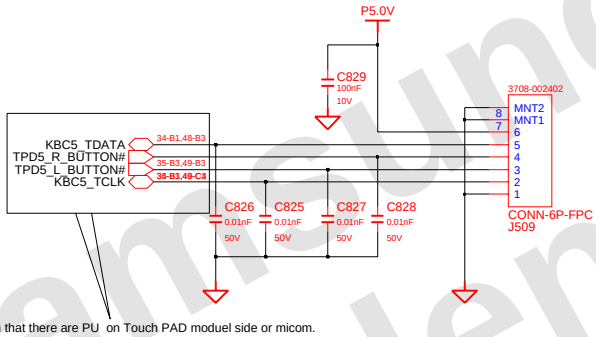
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MICOM_MEC1308 MICOM_MEC1308	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 33 OF 58	

Micom Glue Logic

KEYBOARD

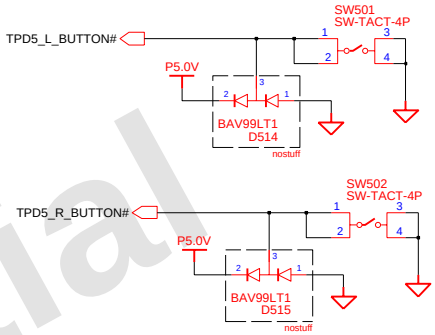


TOUCHPAD

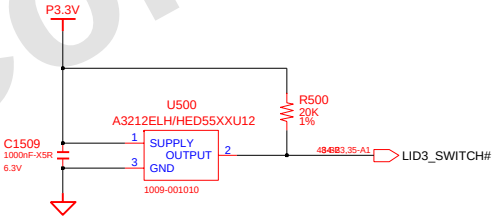


Confrim that there are PU on Touch PAD moduel side or micom.

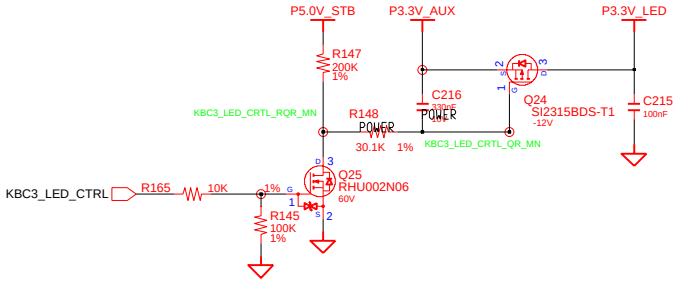
TOUCHPAD BUTTON



LID SWITCH



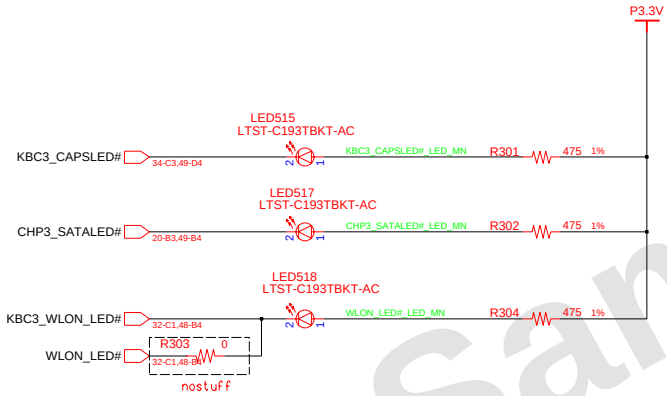
TOUCHPAD LED POWER



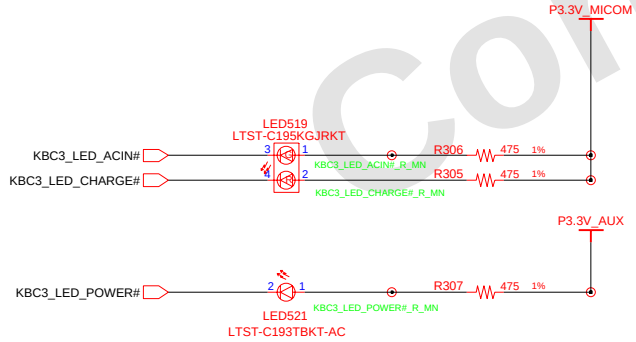
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1	MICOM_GLUE	PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 34 OF 58	

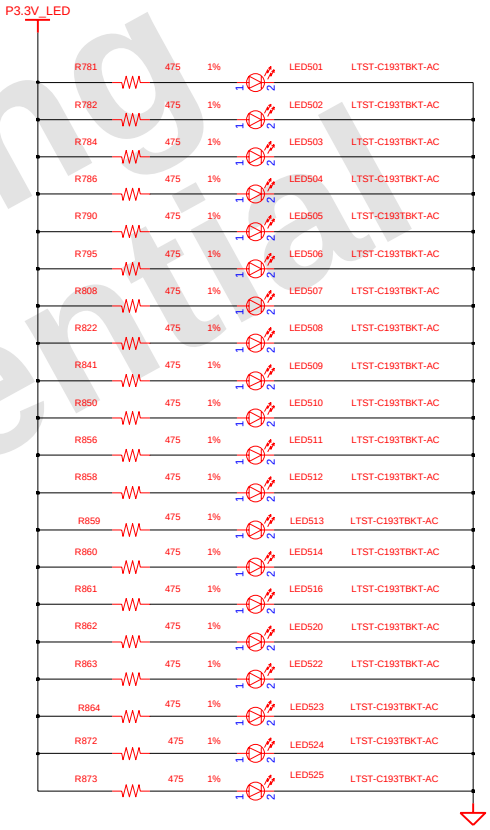
LEDs

FUNCTION KEY LED



ADAPTERIN/CHARGING LED

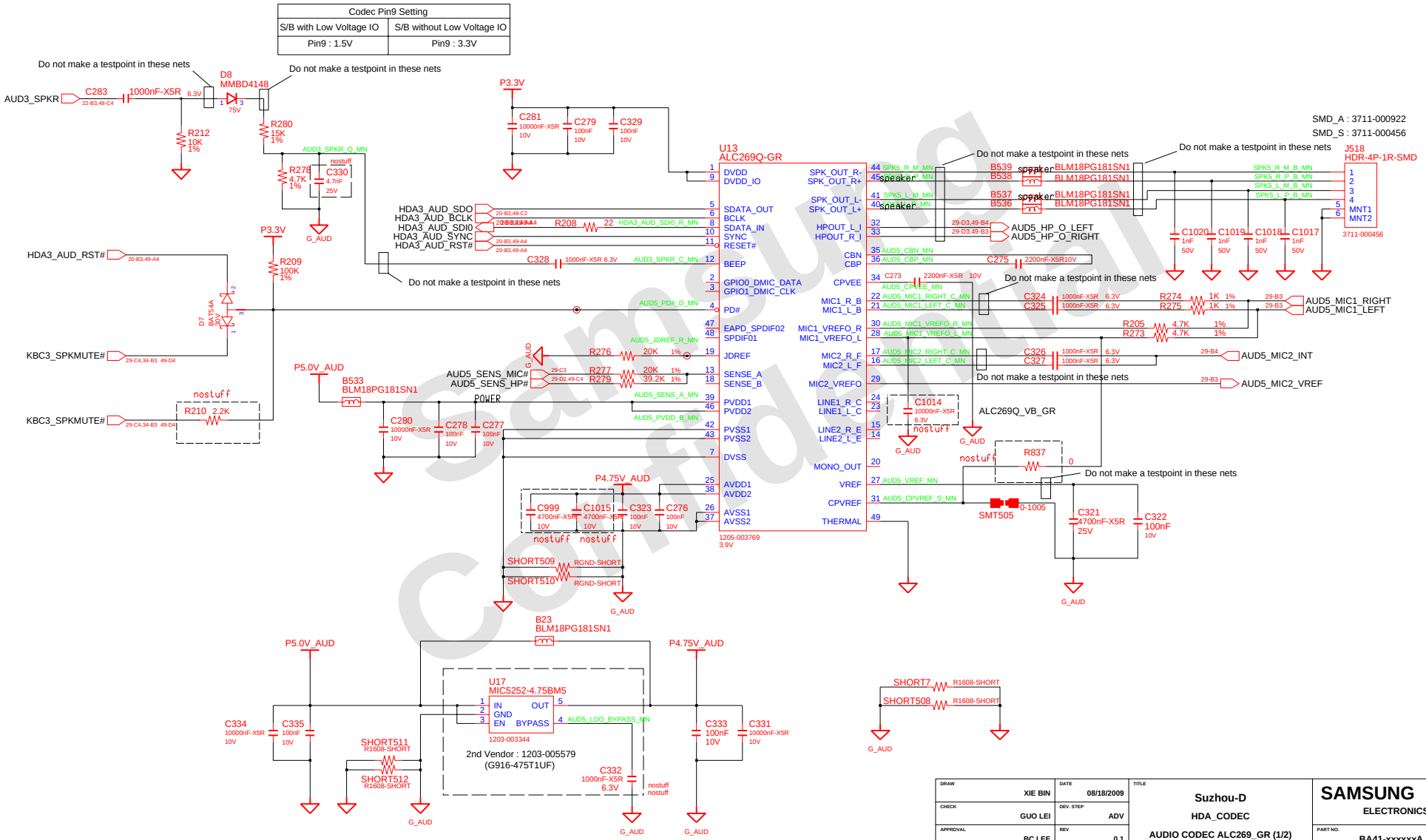




DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D LED_SWITCH LED_SWITCH	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 35 OF 58	

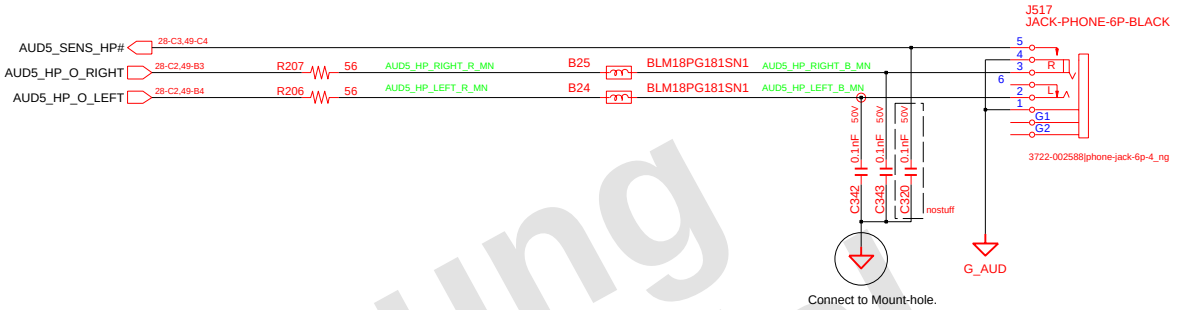
AUdio Codec (ALC269)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

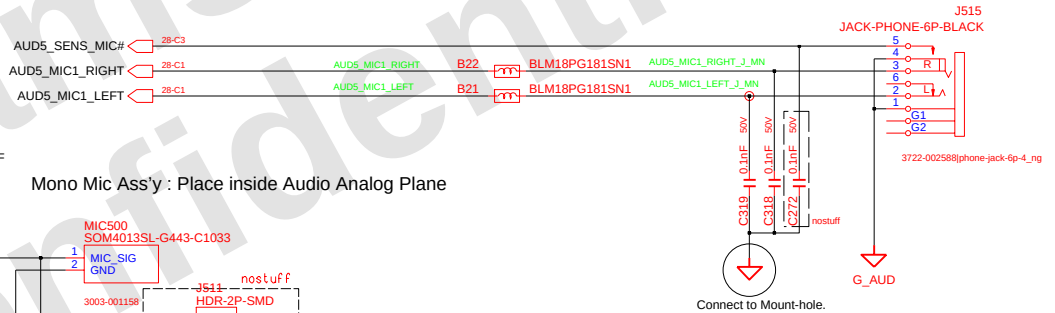


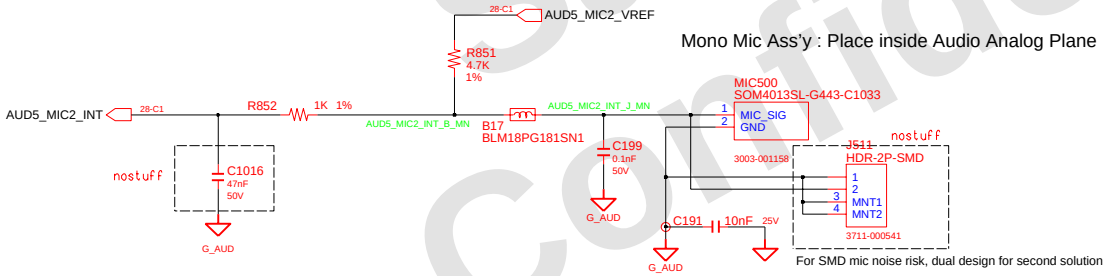
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D HDA_CODEC AUDIO CODEC ALC269_GR (1/2)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 36 OF 58	

HEADPHONE

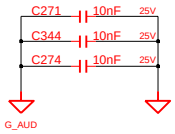


MIC JACK



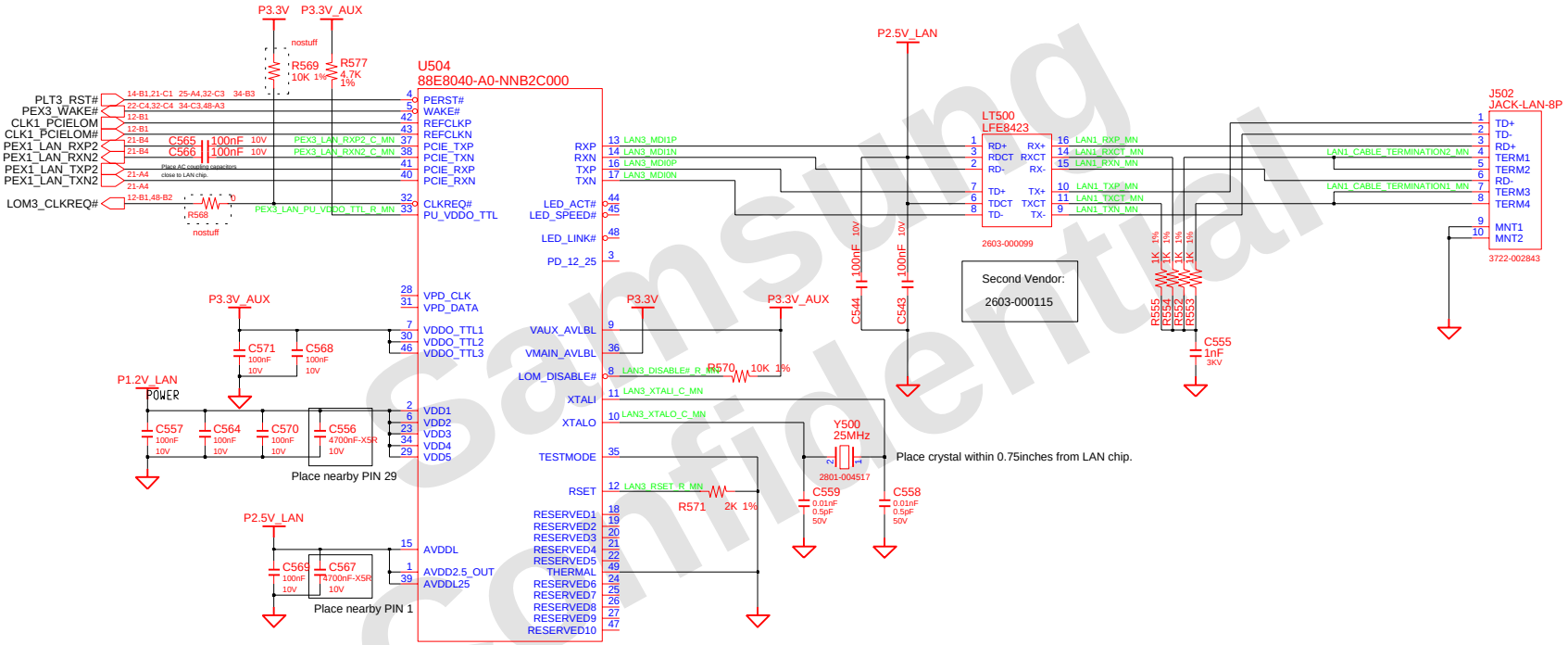


Mono Mic Ass'y : Place inside Audio Analog Plane



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / HDA_CODEC / AUDIO CODEC ALC269_GR (2/2)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 37 OF 58	

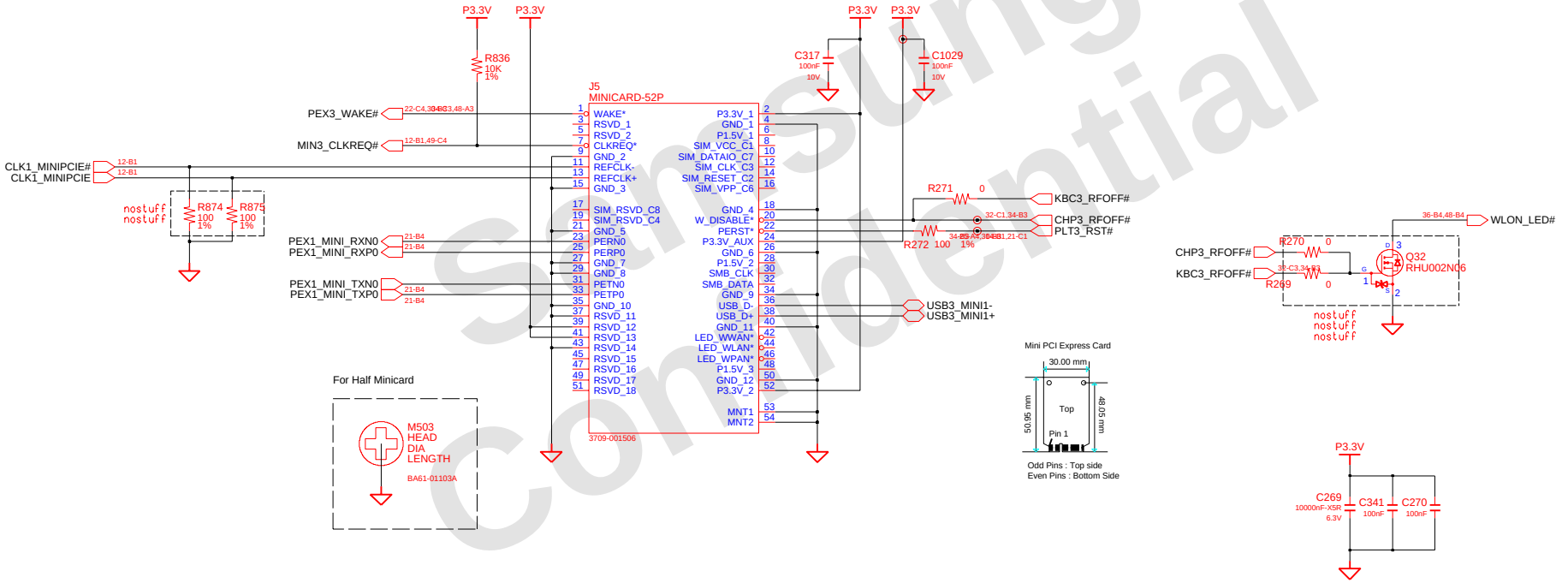
LAN Controller (Marvell 88E8040)



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / LAN / LAN_Marvell 88E8040	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 38 OF 58	

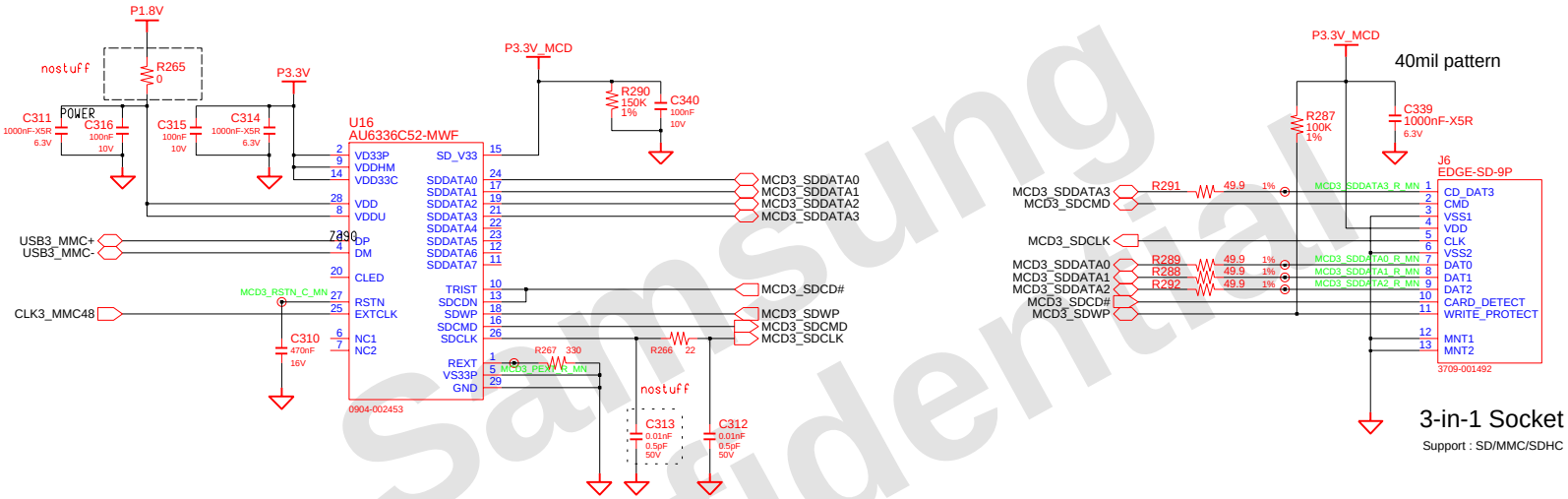
Wireless LAN

WLAN, 4mm



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MINI_PCIE_CONN Wiress LAN	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 39 OF 58	

Card Reader (AU6336)

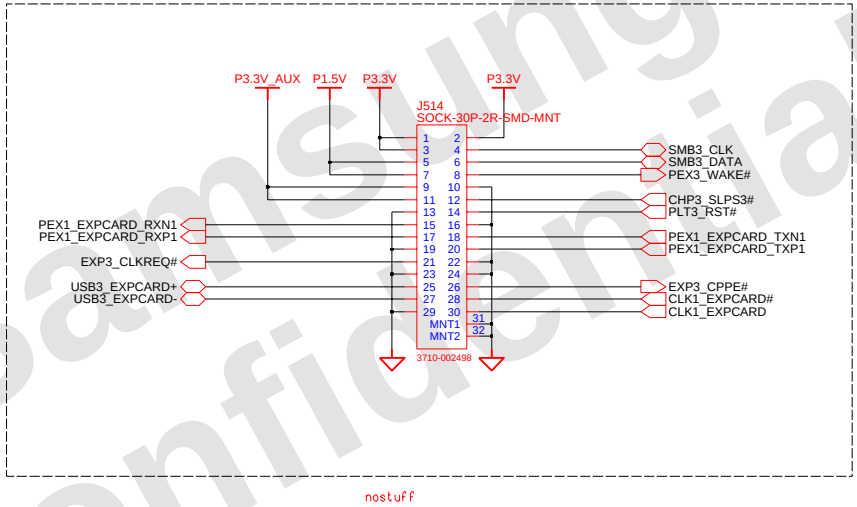


MCD3_SD_SPD	SD v1.0 Clock Option
PU / PD : No Stuff	24 MHz (default)
PU : Stuff, PD : No Stuff	15 MHz

MCD3_CLK_IN	827S Clock Source option
PU : X, PD : X	12MHz, fixed S/N
PU : No Stuff, PD : Stuff	12MHz, no S/N
PU : Stuff, PD : No Stuff	48MHz

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MULTICARD 3 IN 1 CARD	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 40 OF 58	

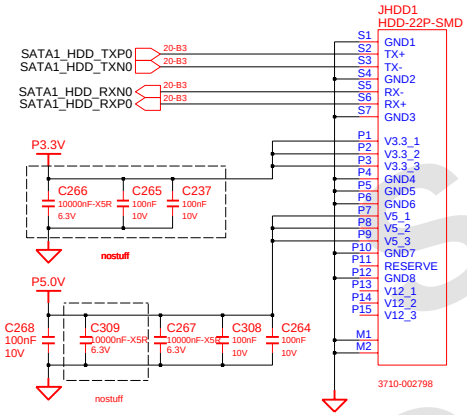
Express Card Connector



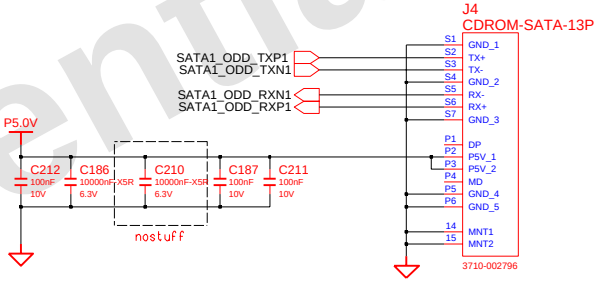
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1	EXPRESS CARD	PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 41 OF 58	

SATA I/F CONN

SATA HDD CONN

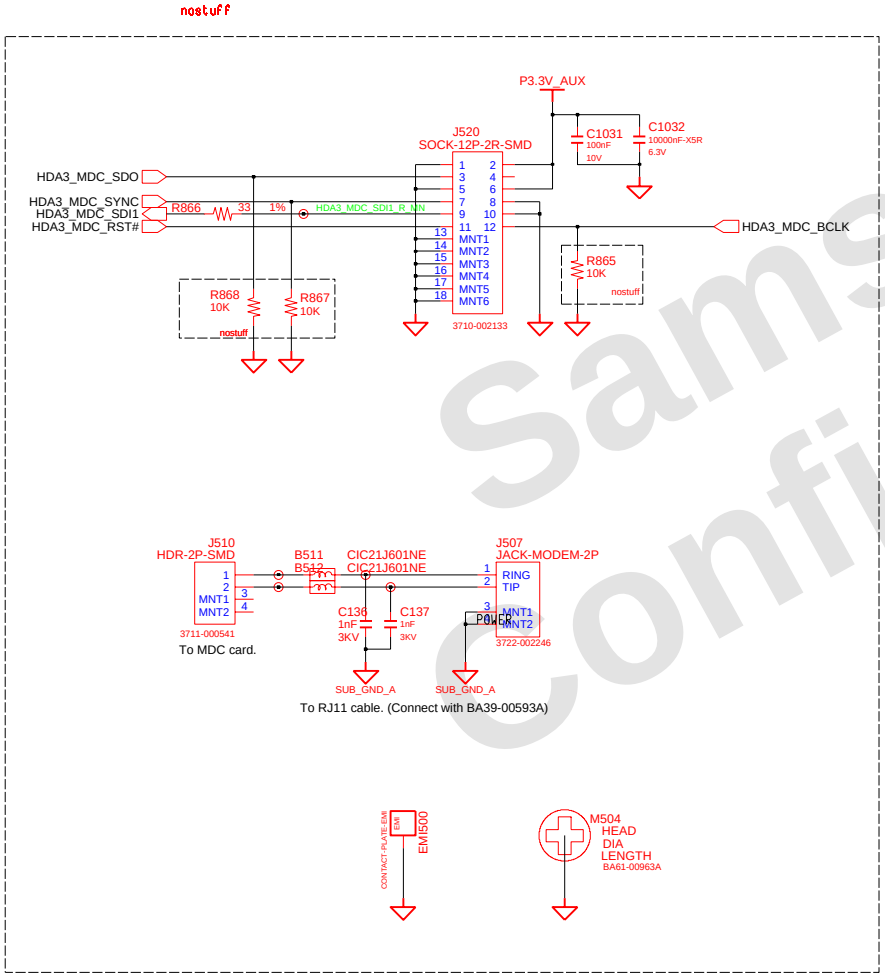


ODD CONN

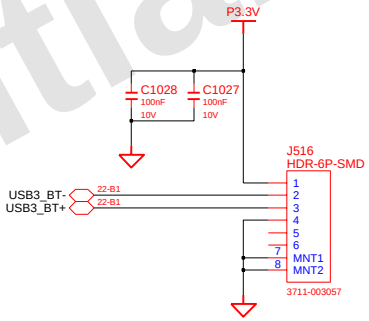


DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D SATA_DEVICES HDD & ODD SUB BONNECTOR	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 42 OF 58	

MDC Connector

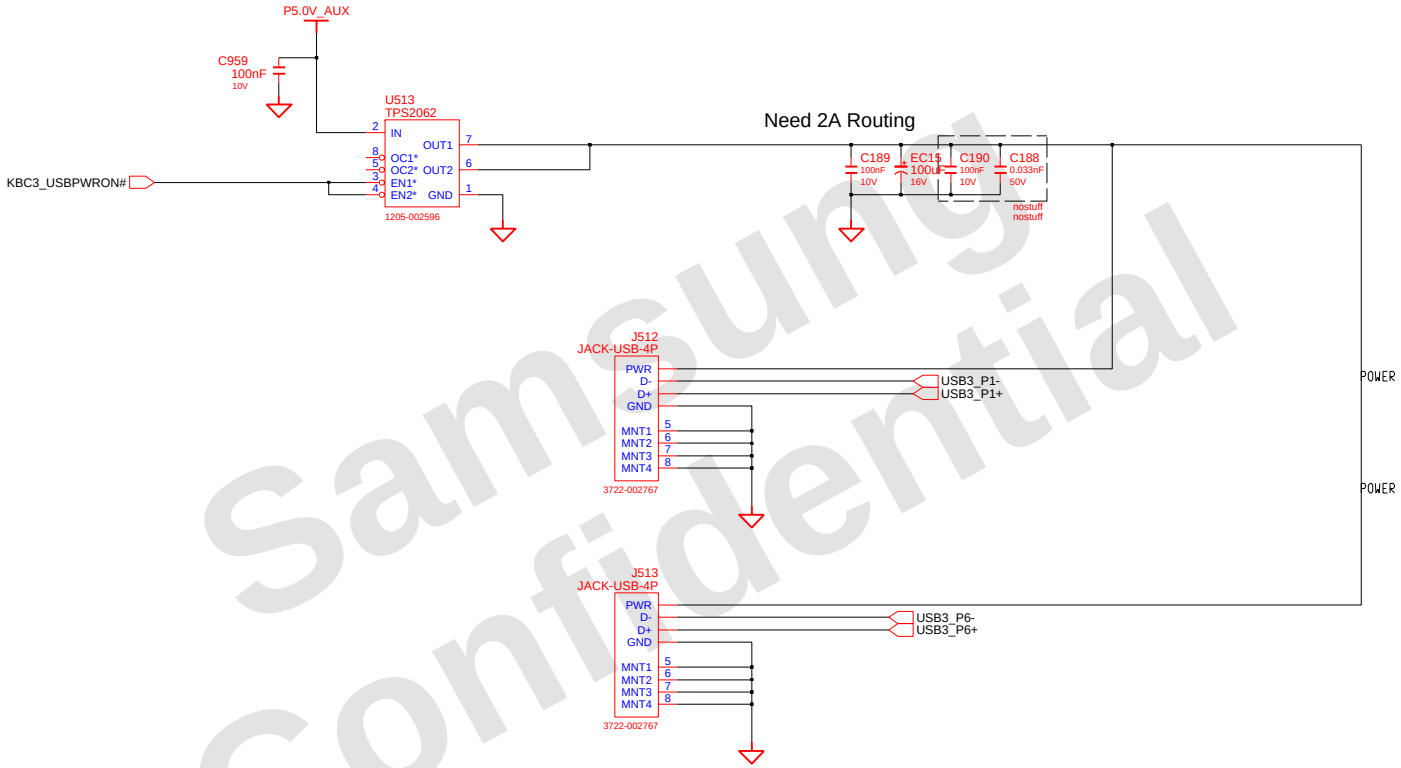


BLUETOOTH



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	HDA_MODEM & BLUETOOTH	
APPROVAL: BC LEE	REV: 0.1	MODEM & BLUETOOTH	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 43 OF 58	

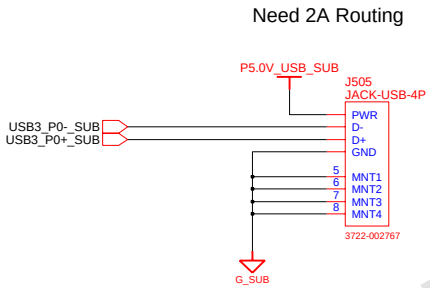
LEFT USB PORT



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D / USB_CONNECTOR / USB_CONNECTOR (1/2)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 44 OF 58	

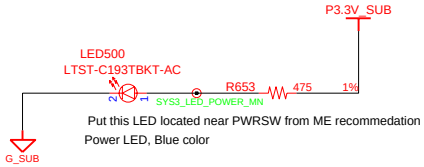
USB PORT & POWER S/W SUB B'D

TOP RIGHT USB PORT

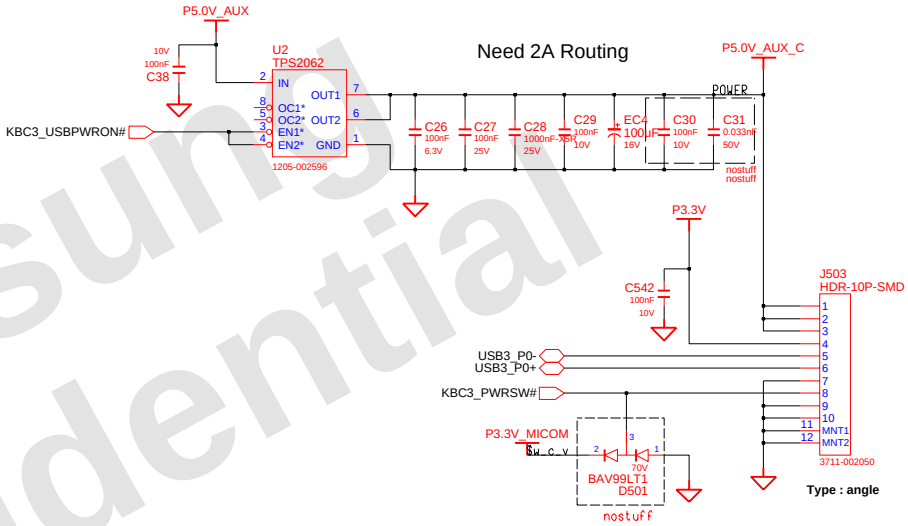


Power Button

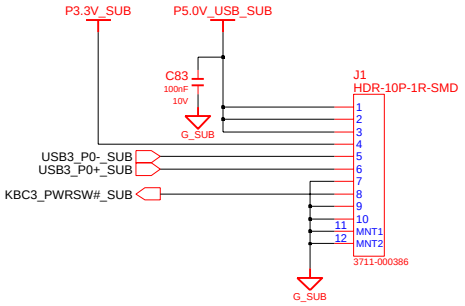
Power ON LED



MAIN TO SUB USB CONN

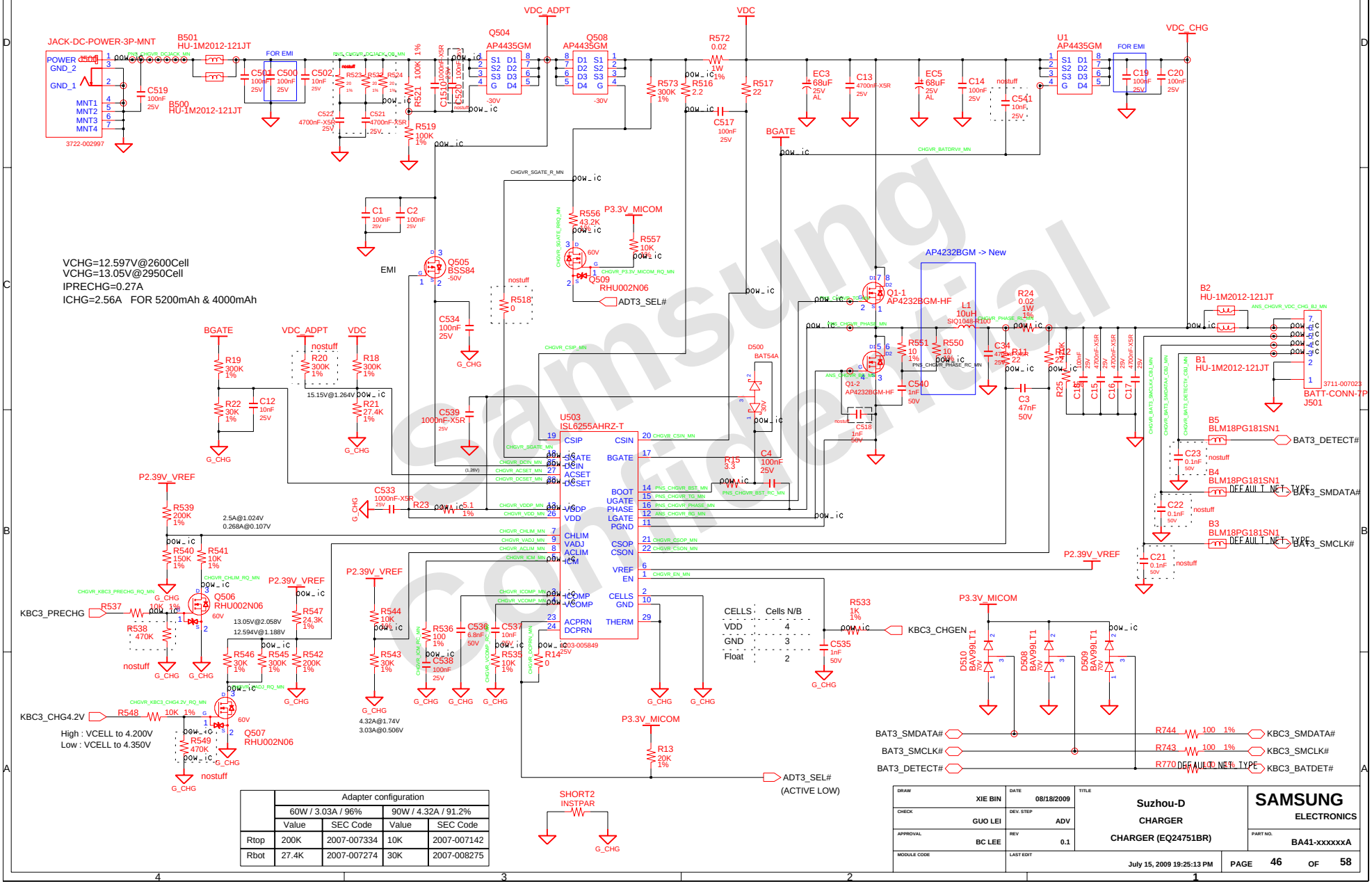


SUB TO MAIN USB CONN



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	USB_CONNECTOR	
APPROVAL: BC LEE	REV: 0.1	USB_CONNECTOR (2/2)	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 45 OF 58	

CHARGER & POWER MANAGEMENT



	Adapter configuration			
	60W / 3.03A / 96%		90W / 4.32A / 91.2%	
	Value	SEC Code	Value	SEC Code
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30K	2007-008275

DRAW	XIE BIN	DATE	08/18/2009
CHECK	GUO LEI	DEV. STEP	ADV
APPROVAL	BC LEE	REV	0.1
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM

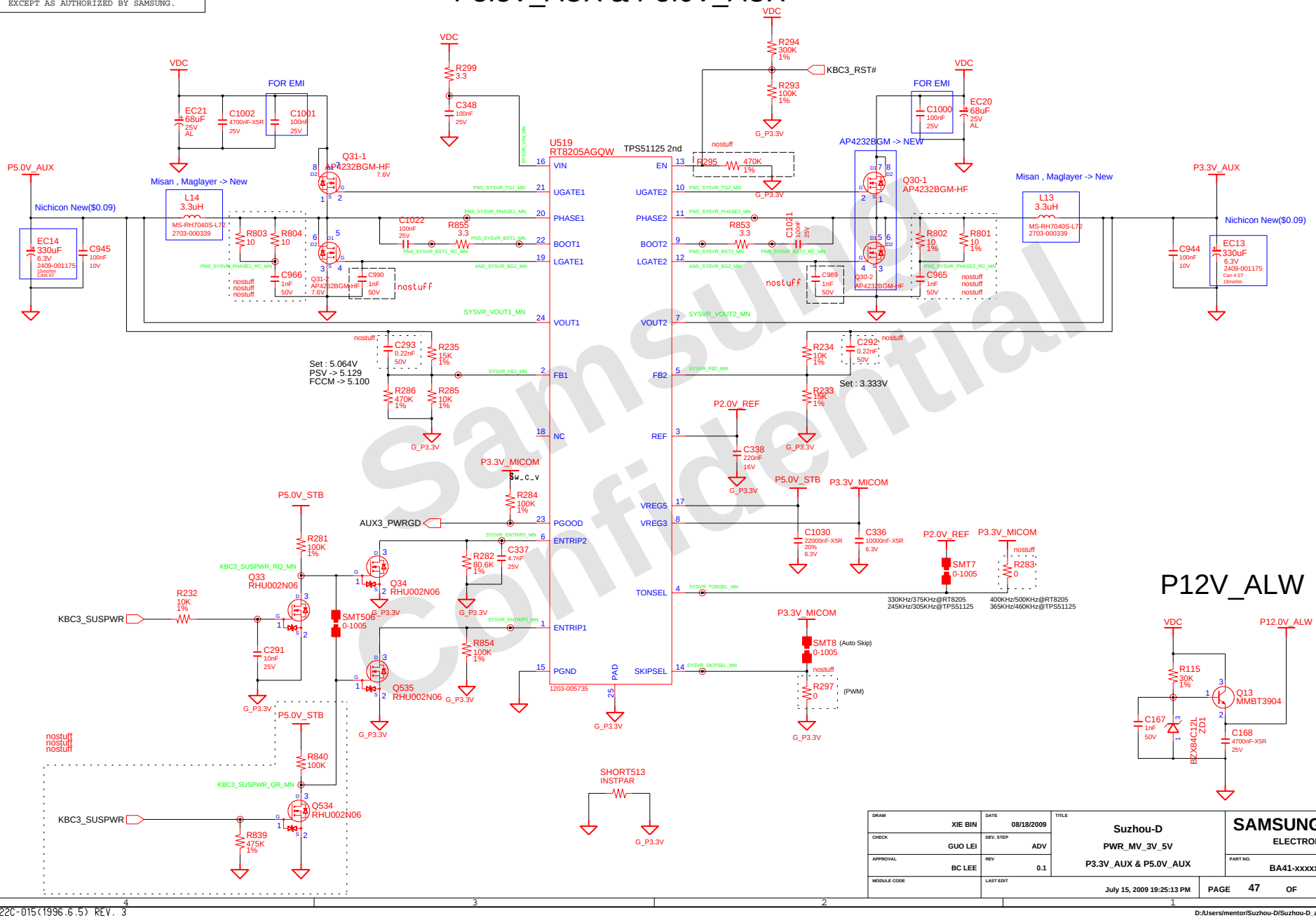
TITLE: Suzhou-D CHARGER CHARGER (EQ24751BR)

SAMSUNG ELECTRONICS

PART NO. BA41-xxxxxxA

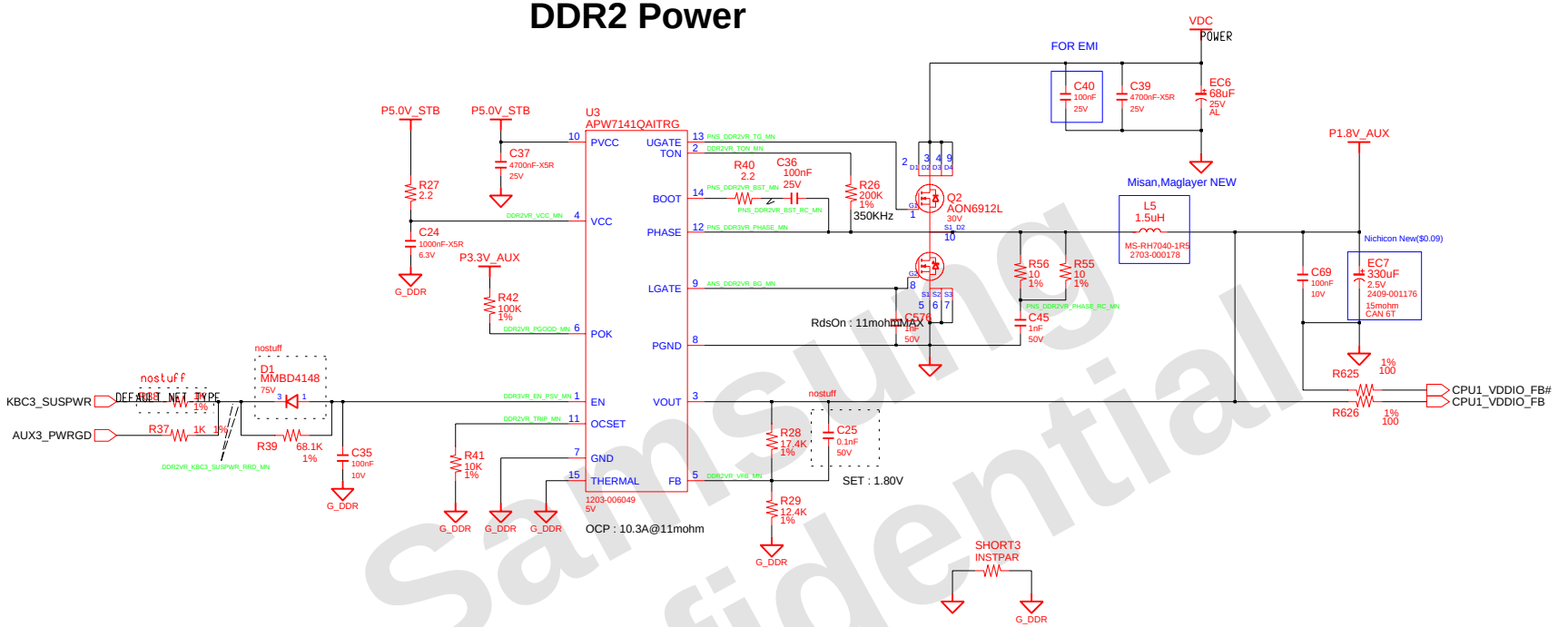
PAGE 46 OF 58

P3.3V_AUX & P5.0V_AUX

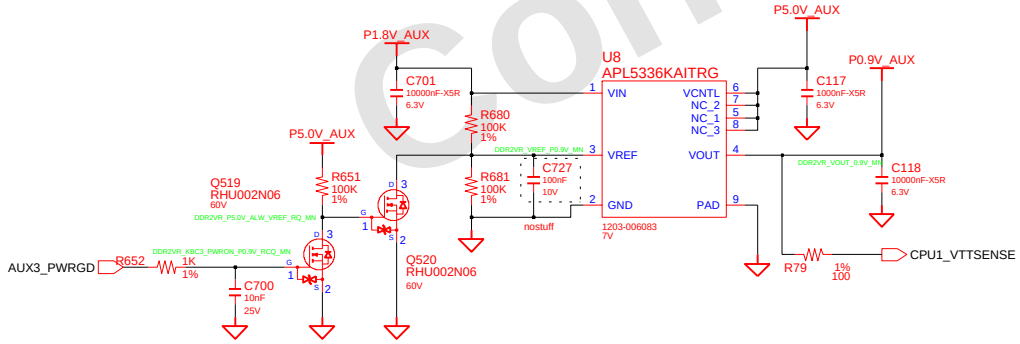


DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	PWR_MV_3V_5V	
APPROVAL: BC LEE	REV: 0.1	P3.3V_AUX & P5.0V_AUX	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 47 OF 58	

DDR2 Power

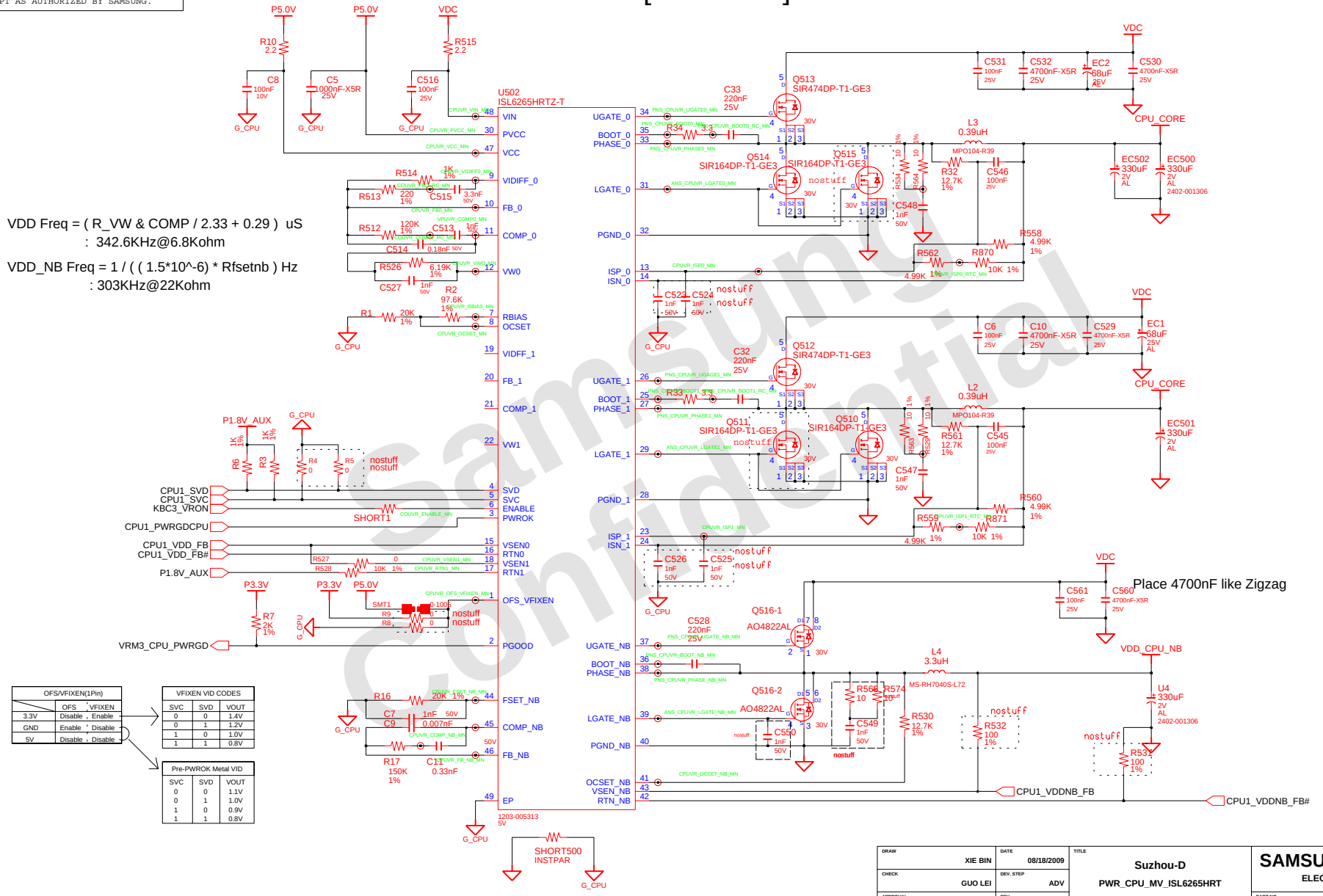


DDR2 VTT(P0.9V_AUX)



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D PWR_MEMORY DDR2 POWER	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 48 OF 58	

CPU VRM [INTERSIL]



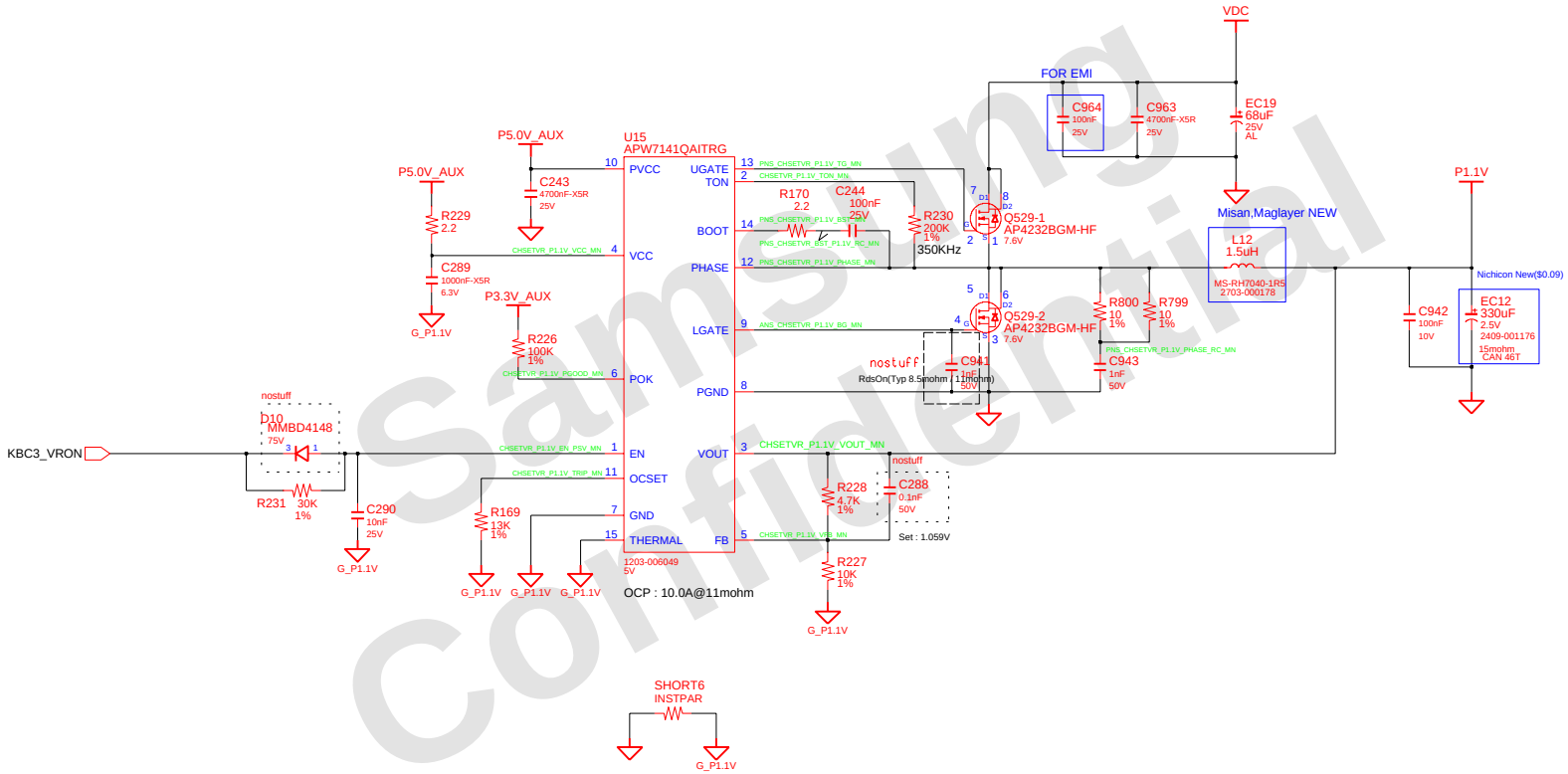
OFS/VFIXEN(1Pin)		
	OFS	VFIXEN
3.3V	Disable	Enable
GND	Enable	Disable
5V	Disable	Disable

VFIXEN VID CODES		
SVC	SVD	VOUT
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

Pre-PWROK Metal VID		
SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

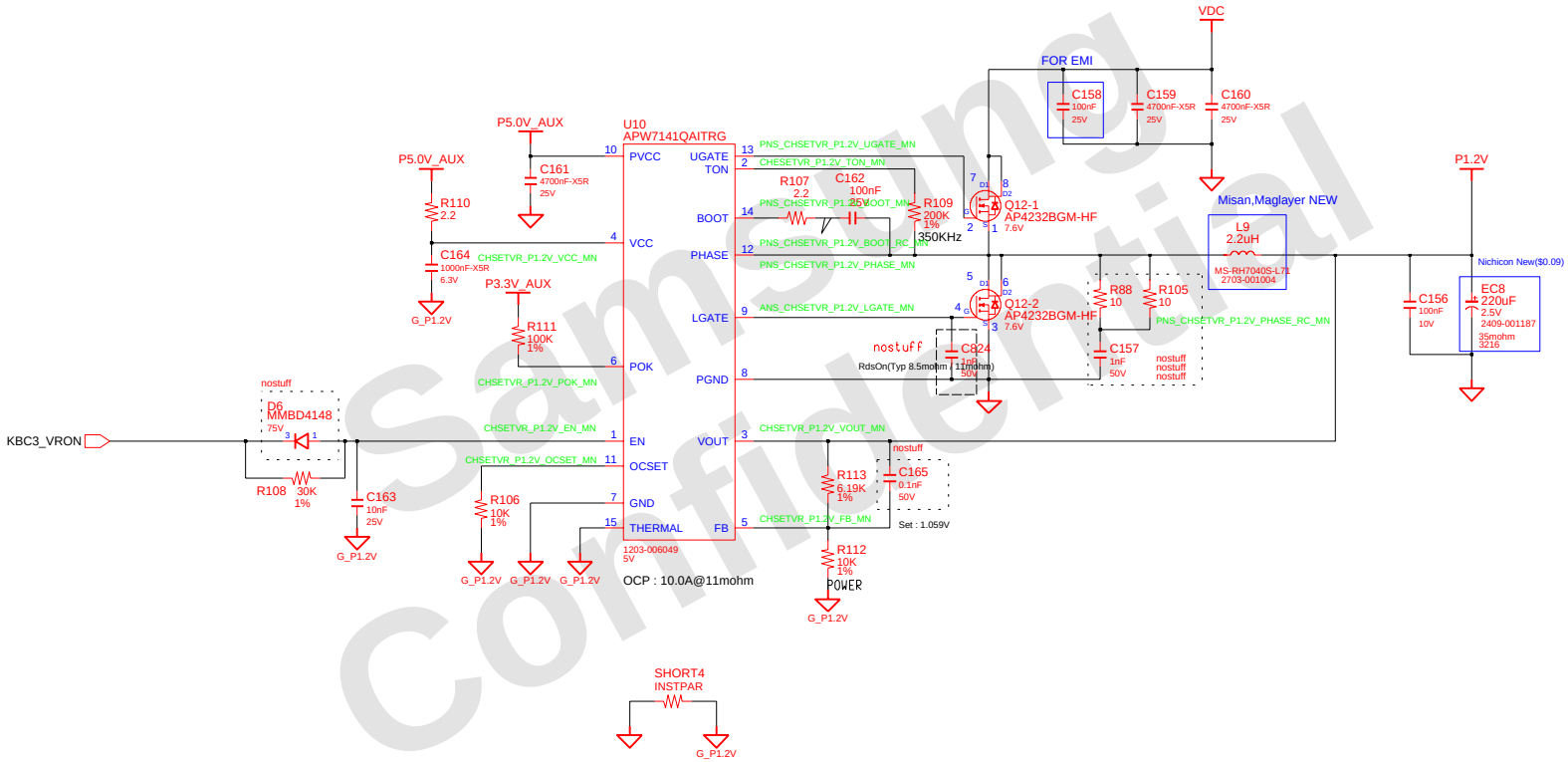
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D PWR_CPU_MV_ISL6265HRT CPU VRM (IMVP6+)	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 49 OF 58	

CHIPSET POWER(P1.1V)



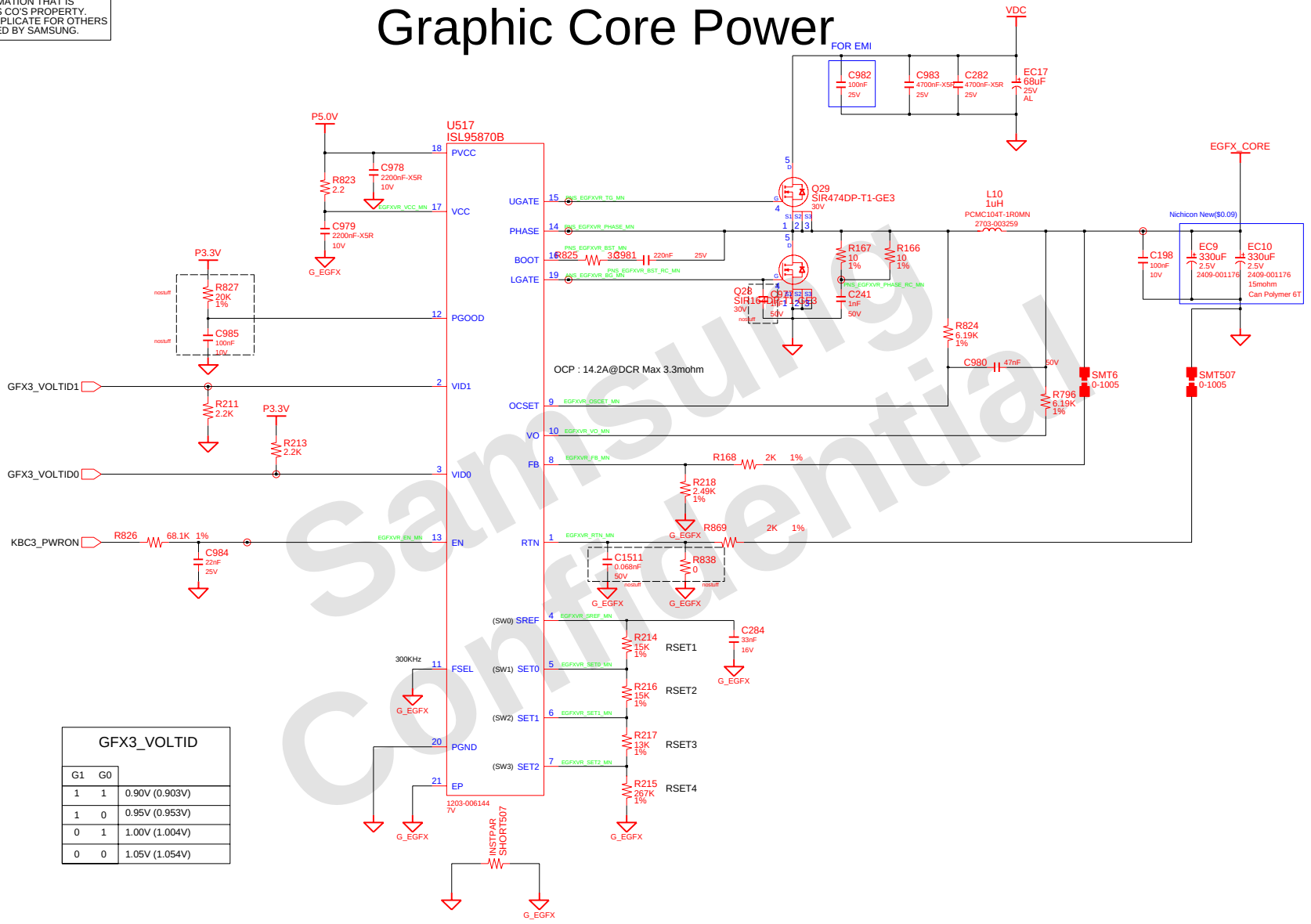
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	PWR_MV_RX881	
APPROVAL: BC LEE	REV: 0.1	P1.1V	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 50 OF 58	

CHIPSET POWER(P1.2V)



DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	PWR_MV_RX881	
APPROVAL: BC LEE	REV: 0.1	P1.2V	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 51 OF 58	

Graphic Core Power

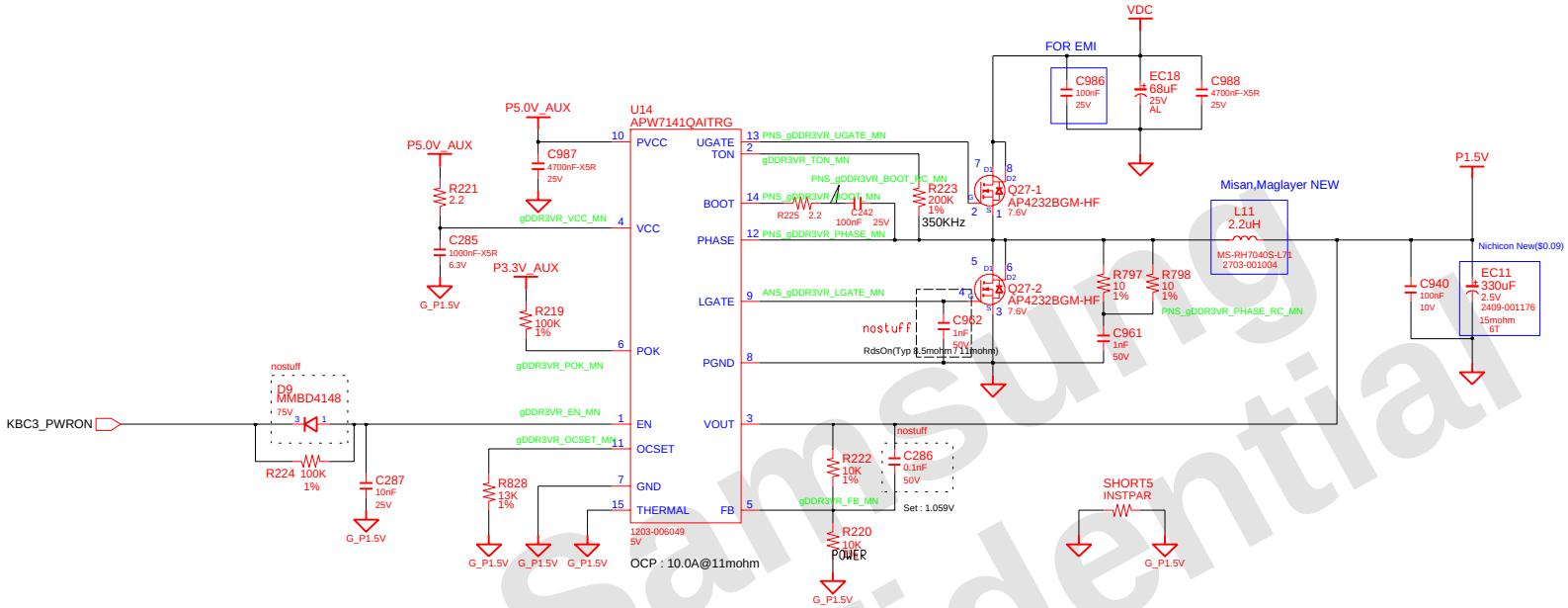


GFX3_VOLTID

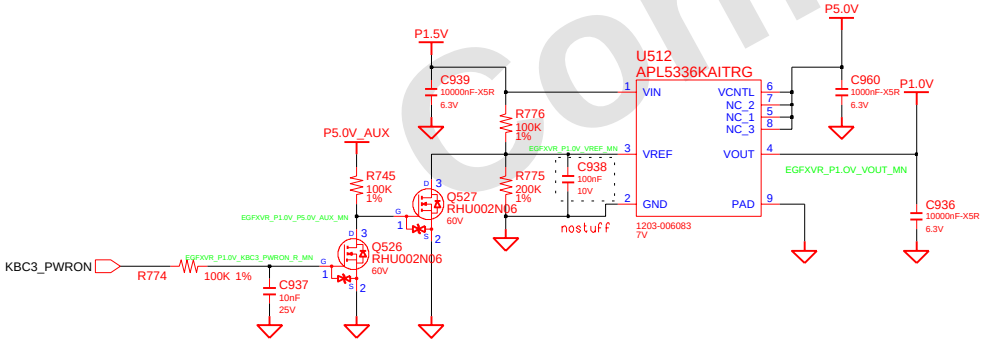
G1	G0	
1	1	0.90V (0.903V)
1	0	0.95V (0.953V)
0	1	1.00V (1.004V)
0	0	1.05V (1.054V)

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D PWR_GFX GFX POWER	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 52 OF 58	

gDDR3 POWER(P1.5V)



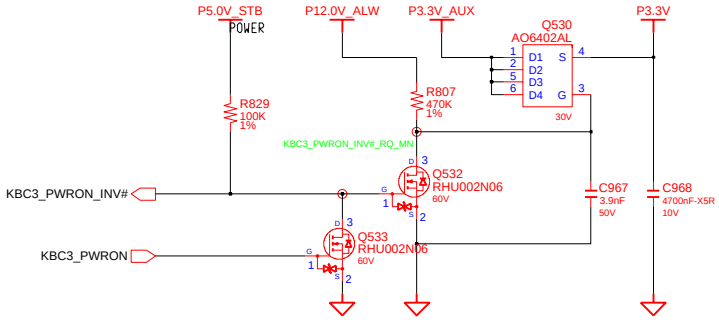
P1.0V



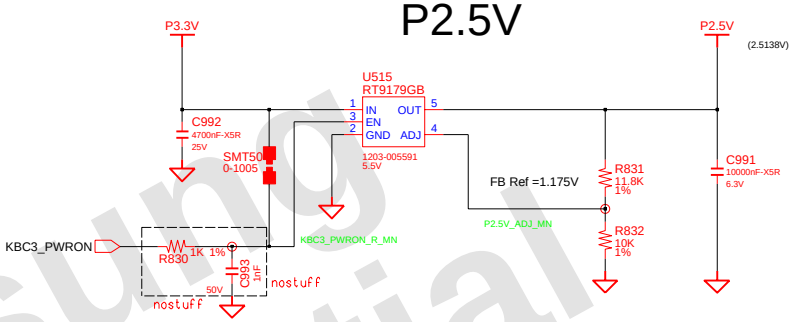
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D PWR_GFX MEMORY gDDR3 POWER	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 53 OF 58	

Switched Power

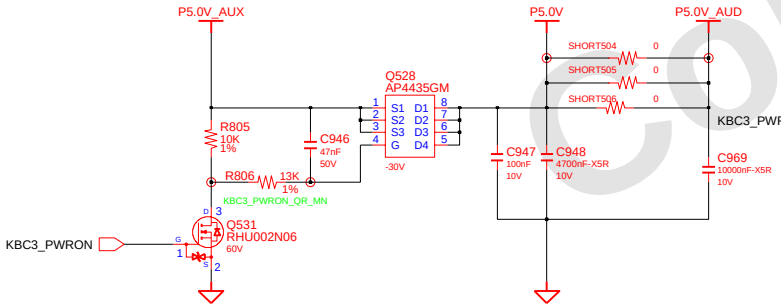
Switched Power On (P3.3V)



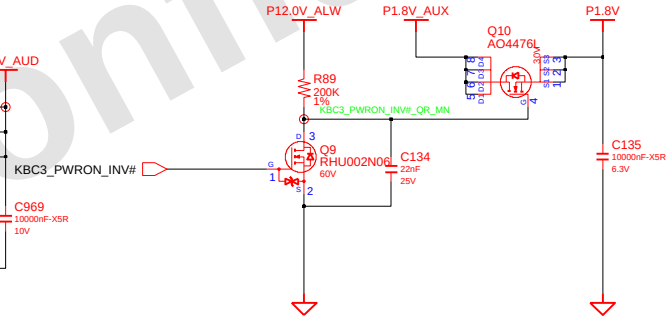
P2.5V



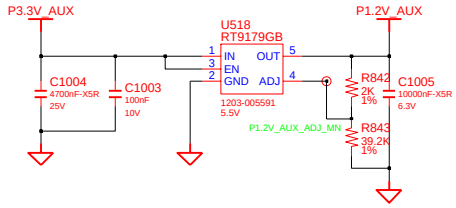
Switched Power On (P5.0V)



Switched Power On (P1.8V)

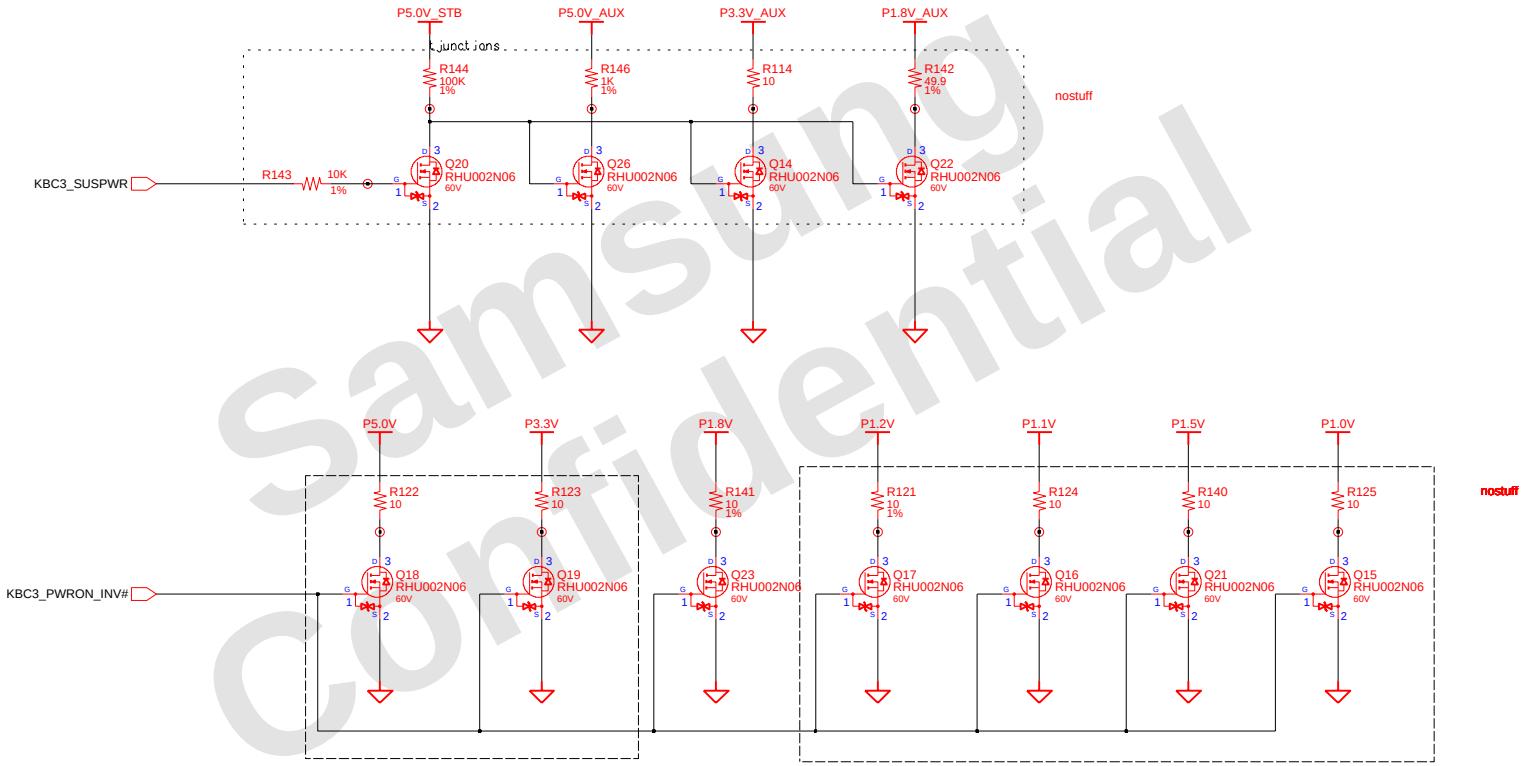


P1.2V_AUX

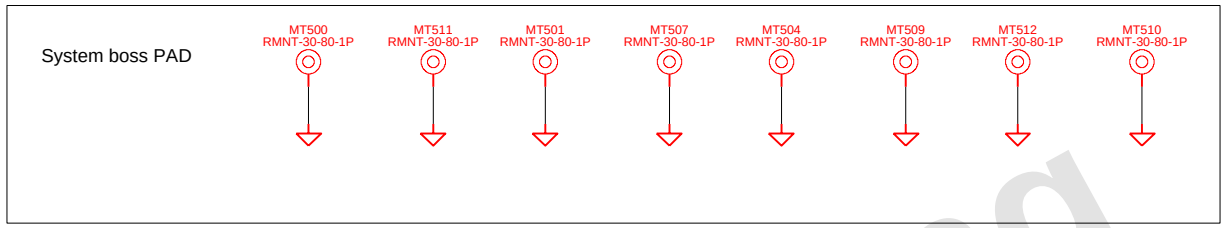


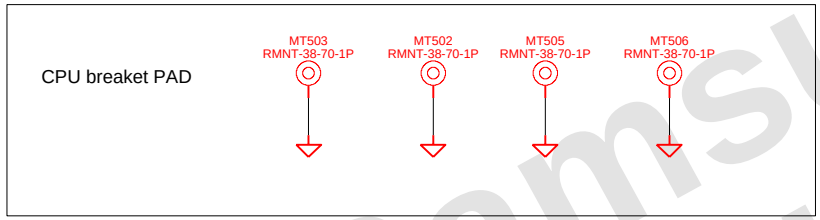
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	PWR_SWITCH	
APPROVAL: BC LEE	REV: 0.1	SWITCH POWER	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 54 OF 58	

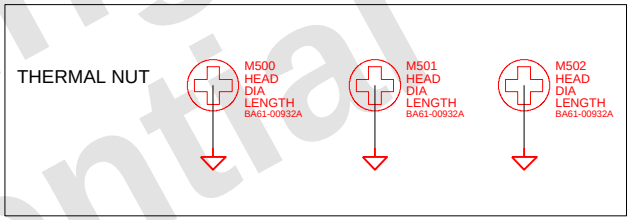
POWER DISCHARGER

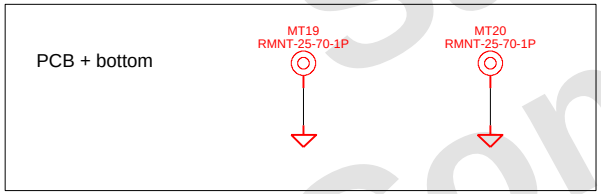


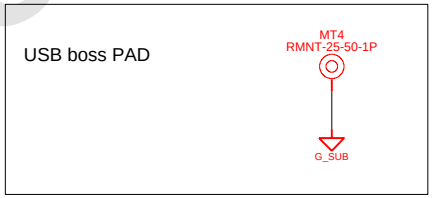
DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV	PWR_CPU_MV_IDISCHARGER	
APPROVAL: BC LEE	REV: 0.1	DISCHARGER LOGIC	PART NO.: BA41-xxxxxxA
MODULE CODE	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 55 OF 58	

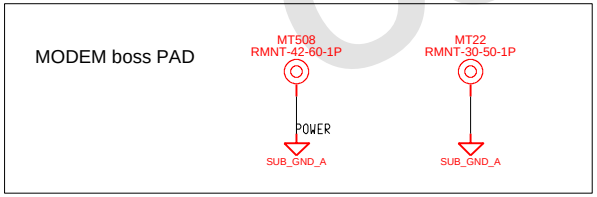












DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 56 OF 58	

- VREFG
- CPU1_SIC
- CPU1_SID
- CPU1_SVC
- CPU1_SVD
- CRT3_RED
- SMB3_CLK
- SPI3_CLK
- ADT3_SEL#
- CRT3_BLUE
- KBC3_A20G
- KBC3_VRON
- KBC5_TCLK
- LCD1_ACLK
- LCD3_BRIT
- LPC3_CLK0
- LPC3_CLK1
- MCD3_SDWP
- SMB3_DATA
- SPI3_CS0#
- SPI3_MISO
- SPI3_MOSI
- THM3_STP#
- WLON_LED#
- CRT3_GREEN
- CRT3_HSYNC
- CRT3_VSYNC
- CRT5_HSYNC
- CRT5_VSYNC
- DBG3_HSYNC
- DBG3_VSYNC
- GFX3_GPIO0
- GFX3_GPIO1
- GFX3_GPIO2
- KBC3_CHGEN
- KBC3_PWRGD
- KBC3_PWRON
- KBC3_RCIN#
- KBC5_TDATA
- MCD3_SDCD#
- MCD3_SDCLK
- MCD3_SDCMD
- MEM1_VREF0
- MEM1_VREF1
- PEX3_WAKE#
- SB_X1_C_MN
- SB_X2_C_MN

- CHGVR_EN_MN
- CHP3_GPIO16
- CHP3_GPIO17
- CHP3_RTCCLK
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS5#
- CK_PDI#_R_MN
- CPU1_ALERT#
- CRT3_DDCCLK
- GFX_NC_B_MN
- KBC3_BKLTON
- KBC3_PRECHG
- KBC3_PWRSW#
- KBC3_RFOFF#
- KBC3_SCLED#
- KBC3_SMCLK#
- KBC3_SPI_DI
- KBC3_SPI_DO
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)

- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- LCD3_BKLTON
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- SMB3_ALERT#
- BAT3_DETECT#
- CHGVR_ICM_MN
- CHGVR_VDD_MN
- CPU1_LDTREQ#
- CPU1_LDTRST#
- CPU1_LDTSTP#
- CRT3_DDCDATA
- EGFXVR_FB_MN
- EGFXVR_VO_MN
- EXP3_CLKREQ#
- KBC3_BATDET#
- KBC3_CHG4.2V
- KBC3_EXTSMI#
- KBC3_NUMLED#
- KBC3_PWRBTN#
- KBC3_RSMRST#
- KBC3_RUNSCI#
- KBC3_SMDATA#
- KBC3_SPI_CLK
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)
- KBC_CAP_C_MN
- LID3_SWITCH#
- LPC3_LFRAME#
- MCD3_SDDATA0
- MCD3_SDDATA1
- MCD3_SDDATA2
- MCD3_SDDATA3
- MCH3_EXTTS0#
- MCH3_EXTTS1#
- MIN3_CLKREQ#
- PCI3_CLKRUN#
- SYSVR_FB2_MN
- CHGVR_CSIN_MN
- CHGVR_CSIP_MN
- CHGVR_CSON_MN
- CHGVR_CSOP_MN
- CHGVR_DCIN_MN
- CHGVR_VADJ_MN
- CHGVR_VDDP_MN
- CHP3_NB_PWRGD
- CHP3_SATALED#
- CHP3_SB_TEST0
- CHP3_SB_TEST2
- CHP3_SUSSTAT#
- CPU1_VDDIO_FB
- CPU1_VDDNB_FB
- CPU1_VTTSENSE
- CRT3_RED_L_MN
- DDR2VR_TON_MN
- DDR2VR_VCC_MN
- DDR2VR_VFB_MN
- EGFXVR_RTN_MN
- EGFXVR_VCC_MN

- GDDR3VR_EN_MN
- GDDR3VR_FB_MN
- GFX_RSET_R_MN
- KBC3_CAPSLED#
- KBC3_LED_CTRL
- KBC3_SPI_CS0#
- KBC3_SPKMUTE#
- KBC3_WAKESCI#
- LCD3_EDID_CLK
- PEG3_HPD_HDMI
- PEG5_HDMI_CLK
- VGA5_HDMI_HPD
- CHGVR_ACLIM_MN
- CHGVR_ACSET_MN
- CHGVR_CHLIM_MN
- CHGVR_DCPRN_MN
- CHGVR_DCSET_MN
- CHGVR_ICOMP_MN
- CHGVR_SGATE_MN
- CHGVR_VCOMP_MN
- CHP3_BIOS_CRI#
- CHP3_INTRUDER#
- CHP3_THRMTRIP#
- CPU1_THRMTRIP#
- CPU1_VDDIO_FB#
- CPU1_VDDNB_FB#
- CPUVR_VSEN1_MN
- DDR2VR_TRIP_MN
- EGFXVR_SET0_MN
- EGFXVR_SET1_MN
- EGFXVR_SET2_MN
- EGFXVR_SREF_MN
- GDDR3VR_POK_MN
- GDDR3VR_TON_MN
- GDDR3VR_VCC_MN
- GFX_MPV18_B_MN
- GFX_PX_EN_R_MN
- GFX_R2SET_R_MN
- KBC3_KCLK_R_MN
- KBC3_KDAT_R_MN
- KBC3_LED_ACIN#
- KBC3_USBPWRON#
- KBC3_WLON_LED#
- LAN3_RSET_R_MN
- LCD3_EDID_DATA
- PEG3_HDMI_DATA
- PEG5_HDMI_DATA
- TP05_L_BUTTON#
- TPD5_R_BUTTON#
- VRM3_CPU_PWRGD
- CHGVR_ICM_RC_MN
- COUVR_ENABLE_MN
- CPU1_ALL_LDTSTP
- CRT3_GREEN_L_MN
- CRT3_P5.0V_D_MN
- DDR2VR_PGOOD_MN
- EGFXVR_OSCET_MN
- GFX_TESTEN_R_MN
- GFX_XTALIN_R_MN
- KBC3_EMCLK_R_MN
- KBC3_EMDAT_R_MN
- KBC3_LED_POWER#
- KBC3_PWRSW#_SUB
- ANS_DDR2VR_BG_MN
- ANS_SYSVR_BG1_MN
- ANS_SYSVR_BG2_MN
- CHGVR_SGATE_R_MN
- CHGVR_VADJ_RQ_MN
- DDR3VR_EN_PSV_MN
- GDDR3VR_OCSET_MN
- GFX_MVREFSA_R_MN
- GFX_PWRGOOD_R_MN
- GML_VREFCA0_R_MN
- GML_VREFCA1_R_MN
- GML_VREFDQ0_R_MN

- GML_VREFDQ1_R_MN
- GML_ZQ_ZQ00_R_MN
- GML_ZQ_ZQ01_R_MN
- GMU_VREFCA0_R_MN
- GMU_VREFCA1_R_MN
- GMU_VREFDQ0_R_MN
- GMU_VREFDQ1_R_MN
- GMU_ZQ_ZQ00_R_MN
- GMU_ZQ_ZQ01_R_MN
- KBC3_LED_CHARGE#
- KBC3_THERM_SMCLK
- PNS_CHGVR_BST_MN
- PNS_DDR2VR_TG_MN
- PNS_SYSVR_TG1_MN
- PNS_SYSVR_TG2_MN
- SB_DDC1_SCL_R_MN
- SB_DDC1_SDA_R_MN
- TH_SHDN_SEL_R_MN
- WLON_LED#_LED_MN
- CHGVR_CHLIM_RQ_MN
- CHGVR_VCOMP_RC_MN
- CPU_TEST25_H_R_MN
- CPU_TEST25_L_R_MN
- GFX_CLKTESTA_C_MN
- GFX_DPC_CALR_R_MN
- GFX_TESTEN_2_R_MN
- KBC3_THERM_SMDATA
- PNS_DDR2VR_BST_MN
- PNS_EGFXVR_BST_MN
- CHGVR_SGATE_RRQ_MN
- GFX_DPAB_CALR_R_MN
- GFX_DPA_VDD18_B_MN
- GFX_DPC_VDD10_B_MN
- GFX_DPLL_VDDC_B_MN
- LAN3_DISABLE#_R_MN
- PEG5_HDMI_CLK_B_MN
- VGA5_HDMI_HPD_R_MN
- CHSETVR_P1.2V_EN_MN
- CHSETVR_P1.2V_FB_MN
- DDR2VR_VOUT_0.9V_MN
- GFX_MEM_CALRN0_R_MN
- GFX_MEM_CALRP0_R_MN
- GFX_PCIE_CALRN_R_MN
- GFX_PCIE_CALRP_R_MN
- PEG3_LCDVDDON_QR_MN
- PNS_CHGVR_BST_RC_MN
- PNS_DDR3VR_PHASE_MN
- PNS_GDDR3VR_BOOT_MN
- ANS_GDDR3VR_LGATE_MN
- CHP3_SATALED#_LED_MN
- CHSETVR_P1.1V_TON_MN
- CHSETVR_P1.1V_VCC_MN
- CHSETVR_P1.1V_VFB_MN
- CHSETVR_P1.2V_POK_MN
- CHSETVR_P1.2V_VCC_MN
- DDR2VR_VREF_P0.9V_MN
- EGFXVR_P1.0V_VREF_MN
- EGFXVR_P1.0V_VOUT_MN
- KBC3_CAPSLED#_LED_MN
- PNS_DDR2VR_BST_RC_MN
- PNS_EGFXVR_BST_RC_MN
- PNS_GDDR3VR_PHASE_MN
- PNS_GDDR3VR_UGATE_MN
- CHESETVR_P1.2V_TON_MN
- CHSETVR_P1.1V_TRIP_MN
- KBC3_LED_CHARGE#_R_MN
- NB_ALLOW_LDTSTOP_R_MN
- P3.3V_VDD_INV_EN_Q_MN
- PNS_CHGVR_PHASE_RC_MN
- CHSETVR_P1.1V_PGOOD_MN
- CHSETVR_P1.2V_OCSET_MN
- P3.3V_VDD_INV_EN_QR_MN
- PNS_DDR2VR_PHASE_RC_MN
- PNS_GDDR3VR_BOOT_RC_MN
- PNS_SYSVR_PHASE2_RC_MN

- ANS_CHSETVR_P1.1V_BG_MN
- CHGVR_KBC3_PRECHG_RQ_MN
- CHGVR_P3.3V_MICOM_RQ_MN
- CHSETVR_P1.1V_EN_PSV_MN
- CK_REF_0_SEL_HTT66_R_MN
- PNS_CHSETVR_P1.1V_TG_MN
- PNS_GDDR3VR_PHASE_RC_MN
- CHGVR_KBC3_CHG4.2V_RQ_MN
- PNS_CHSETVR_P1.1V_BST_MN
- DDR2VR_KBC3_SUSPWR_RRD_MN
- EGFXVR_P1.0V_P5.0V_AUX_MN
- PNS_CHSETVR_P1.2V_BOOT_MN
- ANS_CHSETVR_P1.2V_LGATE_MN
- NB_REFCLK_N_PWM_GPIO3_R_MN
- PNS_CHSETVR_P1.1V_PHASE_MN
- PNS_CHSETVR_P1.2V_PHASE_MN
- PNS_CHSETVR_P1.2V_UGATE_MN
- DDR2VR_P5.0V_ALW_VREF_RQ_MN
- PNS_CHSETVR_BST_P1.1V_RC_MN
- EGFXVR_P1.0V_KBC3_PWRON_R_MN
- PNS_CHSETVR_P1.2V_BOOT_RC_MN
- PNS_CHSETVR_P1.1V_PHASE_RC_MN
- PNS_CHSETVR_P1.2V_PHASE_RC_MN
- DDR2VR_KBC3_PWRON_P0.9V_RCQ_MN
- AVDD
- A2VDD
- A2VDDQ
- CPU_CORE
- CPU_CORE
- DPC_PVDD
- DPC_VDD18
- G_CHG
- G_CPU
- G_DDR
- G_SUB
- G_EGFX
- G_P1.1V
- G_P1.2V
- G_P1.5V
- G_P3.3V
- LCD_VDD3V
- P1.0V
- P2.5V
- P0.9V_AUX
- P1.2V_AUX
- P1.2V_LAN
- P1.8V_AUX
- P2.0V_REF
- P2.5V_LAN
- P3.3V_LED
- P3.3V_LED
- VDD_LED
- P3.3V_MCD
- P3.3V_MCD
- P3.3V_SUB
- P5.0V_AUX
- P5.0V_AUX
- P5.0V_STB
- P5.0V_STB
- P12.0V_ALW
- P12.0V_ALW

- P4.75V_AUD
- P2.39V_VREF
- P2.39V_VREF
- P5.0V_AUX_C
- P5.0V_USB_SUB
- P5.0V_USB_SUB
- SPV10
- SUB_GND_A
- VDC
- VDC
- VDD1DI
- VDD2DI
- VCC_CRT

- VCC_CRT
- VDD_LED

DRAW: XIE BIN	DATE: 08/18/2009	TITLE: Suzhou-D Test Point	SAMSUNG ELECTRONICS
CHECK: GUO LEI	DEV. STEP: ADV		
APPROVAL: BC LEE	REV: 0.1		PART NO.: BA41-xxxxxxA
MODULE CODE:	LAST EDIT: July 15, 2009 19:25:13 PM	PAGE 57 OF 58	