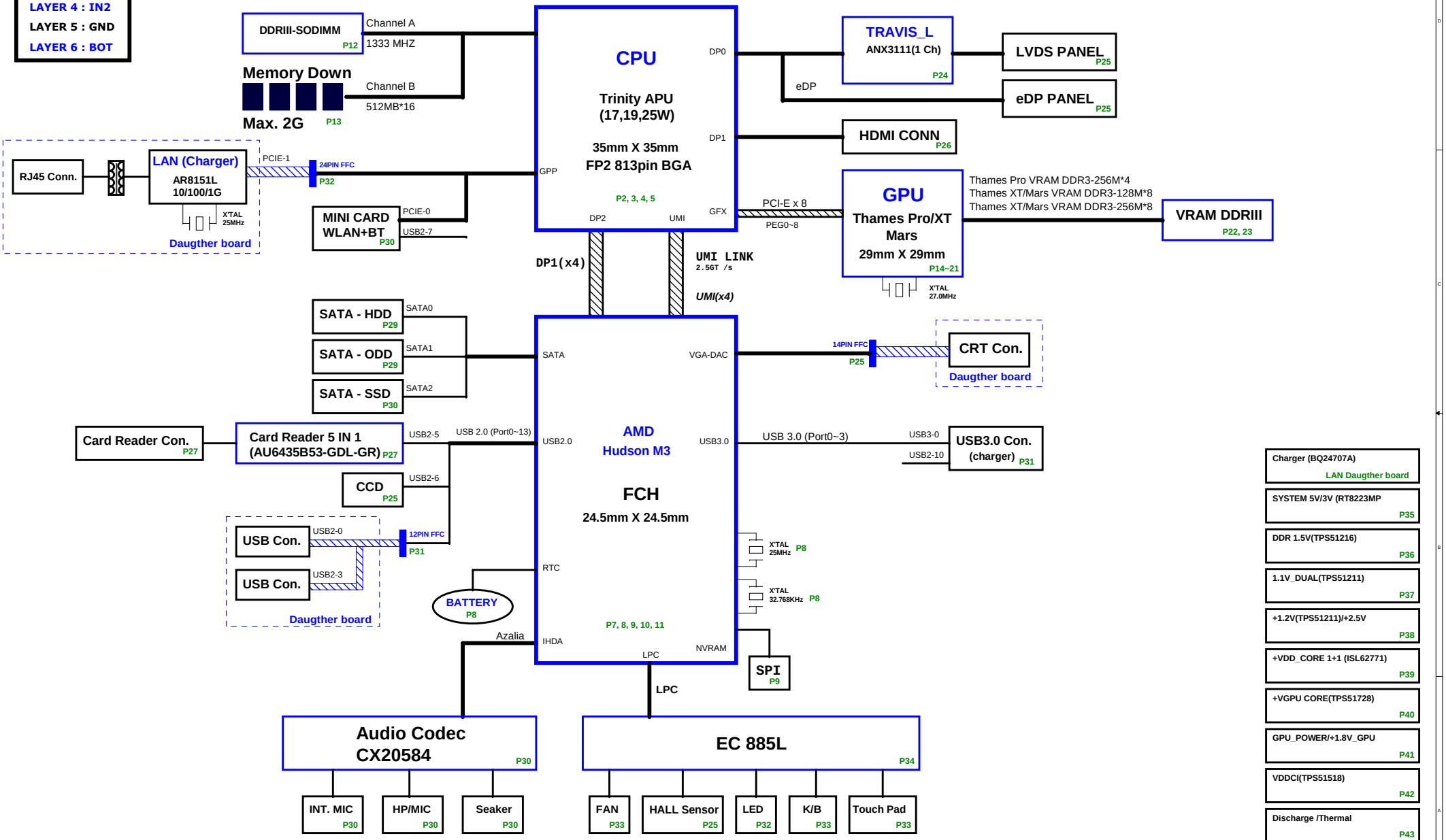
15.6" ZRP Block Diagram

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SVCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT



Quanta Computer Inc.
PROJECT : ZRP

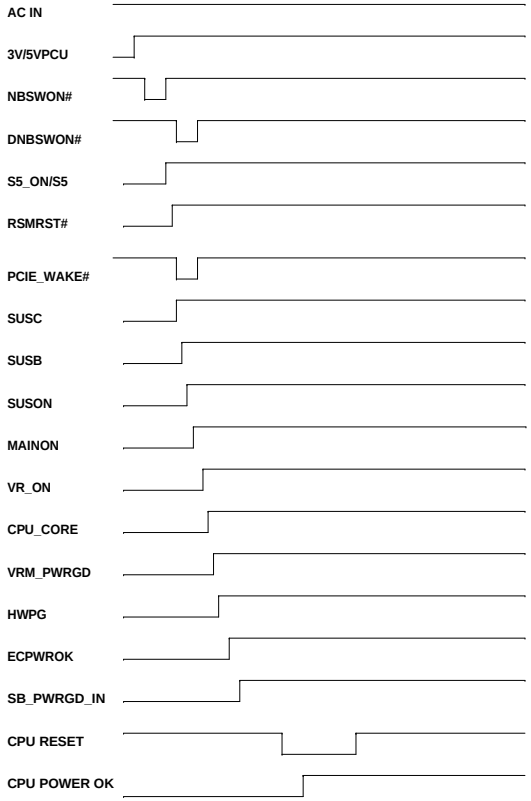
Size	Document Number	Rev
	BLOCK DIAGRAM	A1A

Date: Tuesday, May 29, 2012 Sheet 1 of 44

BOM Option

ITEM	DESCRIPTION	MARK
1	LVDS Panel Sku	LVDS@
2	eDP Panel Sku	eDP@
3	VGA Sku	EV@
4	VGA Thames Sku	EV_T@
5	VGA Mars Sku	EV_M@
6	VGA Sku for Thames and Mars stuff different value parts	EV_SP@
7	GPU 128bit Sku	EV_128@
8	GPU 128bit Sku of Special part value change	EV_128SP@
9	USB Charge Functions Sku	CH@
10	No USB Charge Functions Sku	NCH@
11	USB3.0 Re-Driver Sku	RD@
12	No USB3.0 Re-Driver Sku	NRD@
13	Always connect functions Sku	AC@
14	No Always connect functions Sku	NAC@
15	Special part value change or modify for different BOM sku	SP@

Power Sequence



Hudson M3 SM BUS

FCH SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AD25	DDR / RFID
SCLK1 SDATA1 (+3V_S5)	T7 R7	not used
SCLK2 SDATA2 (+3V_S5)	H19 G19	EC
SCLK3 SDATA3 (+3VPCU)	G22 G21	BATTERY
SCL4 SDATA4 (+3V_S5)	J19 K19	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

EC	FCH	Device	I2C_Device(S)		
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

EC will Conflict with FCH.
Do not mount

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	SYSTEM INFORMATION	A1A

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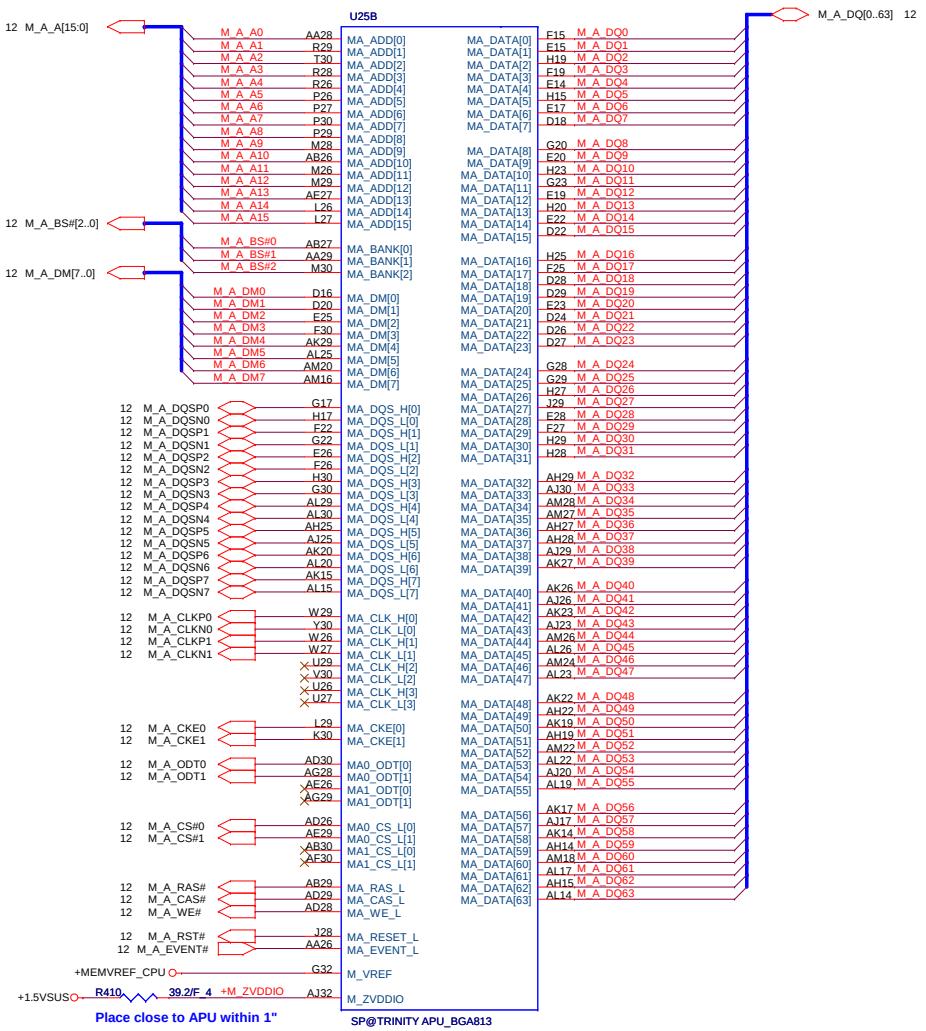
SP : A10(AJ04655UT01)
A8(AJ04555VT01)
A6(AJ04455UT01)
A4(AJ04355UT00)

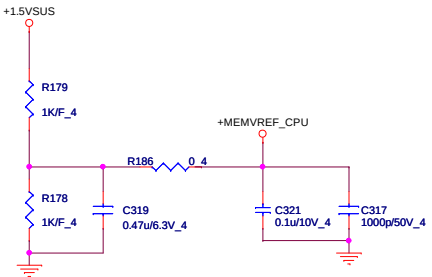
Quanta Computer Inc.
PROJECT : ZRP

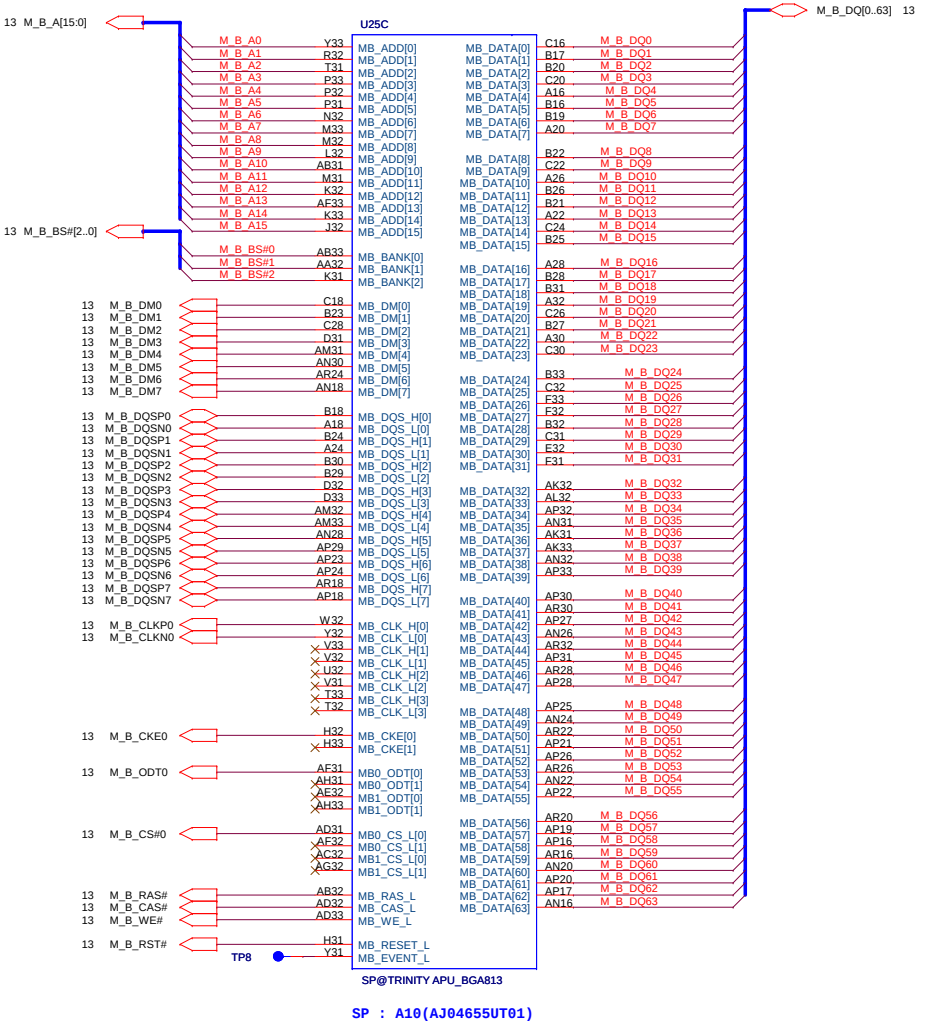
Size	Document Number	Rev
	APU 1/4(PCIE/UMI/GPP/HDT)	A1A
Date: Friday, June 01, 2012	Sheet 3 of 44	

Soldermask openings for all bottom side vias/TPs under FS1



SP : A10(AJ04655UT01)
A8(AJ04555VT01)
A6(AJ04455UT01)
A4(AJ04355UT00)





SP : A10(AJ04655UT01)
A8(AJ04555VT01)
A6(AJ04455UT01)
A4(AJ04355UT00)

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	APU 2/4(DDR3 MEM I/F)	A1A
Date: Friday, June 01, 2012	Sheet 4 of 44	

DP0
LVDS/eDP

DP1
HDMI

DP2
Hudson-M3 VGA output

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

EC
FCH

APU Core Power

SP : A10(AJ04655UT01)
A8(AJ04555VT01)
A6(AJ04455UT01)
A4(AJ04355UT00)

SP@TRINITY APU_BGA813

LVDS / eDP

FCH VGA

To AMD HDT

DMAACTIVE_L controls entry and exit from the sleep and power states

7/8 For Comal.

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

M_TEST CONNECTION TBD

Fan

for normal operation
open Ra , Rb,Rc

		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	APU 3/4(Display/Misc)	A1A
Date: Friday, June 01, 2012	Sheet 5 of 44	

22A
Maximum IDDNBspike 33A

+VDDNB_CORE

C652 22u/6.3V_8 C676 22u/6.3V_8 C659 22u/6.3V_8 C681 22u/6.3V_8

C341 0.22u/10V_4 C335 0.22u/10V_4 C340 180p/50V_4 C345 180p/50V_4 C333 180p/50V_4

For EMI

+VDDNB_CAP

C242 180p/50V_4 C294 *22u/6.3V_8 C264 *22u/6.3V_8 C234 22u/6.3V_8 C586 22u/6.3V_8

+VDD_CORE

U25E

J12 J14 J15 J17 J19 J20 J22 M11 M12 M14 M15 M17 M19 M20 M22 R8 R9 R11 R12 R14 R15 R17 R19 R20 R22 U8 V9 V11 V12 V14 V15 — VDD

V17 V19 V20 V22 W8 AA8 AA9 AA11 AA12 AA14 AA15 AA17 AA19 AA20 AA22 AD9 AD11 AD12 AD14 AD15 AD17 AD19 AD20 AD22 AG12 AG14 AG15 AG17 AG19 AG20 AG22 — VDD

+VDDNB_CORE

A7 A8 A9 A10 A11 A12 A13 A14 A15 B7 B8 B9 B10 — VDDNB

B11 B12 B13 B14 B15 C8 C10 C12 C14 D8 D10 D12 D14 — VDDNB

+VDDNB_CAP

M9 N9 — VDDNB_CAP

+1.5VSUS

2.3A Up to DDR3-1333 @ 1.5V VDDIO

C122 0.22u/10V_4 C114 0.22u/10V_4 C124 0.22u/10V_4 C125 0.22u/10V_4 C273 0.22u/10V_4 C183 0.22u/10V_4

C275 0.22u/10V_4 C184 0.22u/10V_4 C186 0.22u/10V_4 C123 0.22u/10V_4

J33 K23 K25 L28 L30 L33 M27 N23 N25 N30 N33 P28 R27 R30 R33 U28 U30 U33 W28 W30 — VDDIO

W33 AA23 AA25 AA27 AA30 AA33 AB28 AC30 AC33 AD23 AD25 AD27 AE28 AE30 AE33 AG23 AG25 AG27 AG30 AG33 — VDDIO

+1.2V_VDDP

+1.2V R75 0_8

VDDP = 3.5A

C93 22u/6.3V_8 C502 22u/6.3V_8 C503 *22u/6.3V_8 C100 0.22u/10V_4

C98 180p/50V_4 C102 180p/50V_4 C90 1000p/50V_4 C99 1000p/50V_4 C101 0.22u/10V_4

AM12 AN12 AP12 AP13 AR12 AR13 — VDDP

+VDDP_CAP

AA6 AA7 — VDDP_CAP

AM13 AM14 — VDDA

C208 *22u/6.3V_8 C574 22u/6.3V_8

+2.5V_VDDA

+2.5V L5 HCB1608KF-221T20_2A

VDDA= 0.75A

C38 4.7u/6.3V_6 C37 0.22u/10V_4 C41 3300p/50V_4 C39 1000p/50V_4

SP@TRINITY APU_BGA813

SP : A10(AJ04655UT01)
A8(AJ04555VT01)
A6(AJ04455UT01)
A4(AJ04355UT00)

22A
Maximum IDDspike 35A

+VDD_CORE

C145 C266 C265 C188 C193 C240 C189 C144 — 22u/6.3V_8

C238 C237 C292 C190 C134 C291 C293 — 22u/6.3V_8 / *22u/6.3V_8

C219 C116 C143 C224 C117 C115 C223 C169 C221 — 0.22u/10V_4 / 0.01u/25V_4

C168 C267 C220 C167 — 180p/50V_4

For EMI

+VDDNB_CORE

+VDDNB_CAP

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	1.0V ~ 1.3V
VDDNB	+VDDNB_CORE	1.05V ~ 1.325V
VDDIO	+1.5VSUS	1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

+1.5VSUS

C277 22u/6.3V_8 C157 22u/6.3V_8 C256 4.7u/6.3V_6 C222 4.7u/6.3V_6 C302 4.7u/6.3V_6 C130 4.7u/6.3V_6

C241 180p/50V_4 C108 180p/50V_4 C276 180p/50V_4 C204 180p/50V_4

For EMI

VDDR = 3.2A (Up to DDR3-1333 @ 1.5V)

+1.2V_VDDR +1.2V R376 0_8

C50 C51 C499 C52 C498 C500 C47 — 0.22u/10V_4 / 1000p/50V_4 / 180p/50V_4 / 4.7u/6.3V_6

C49 0.01u/25V_4 C48 0.01u/25V_4

SP : A10(AJ04655UT01)
A8(AJ04555VT01)
A6(AJ04455UT01)
A4(AJ04355UT00)

DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split

+1.5VSUS

C181 4.7u/6.3V_6 C227 4.7u/6.3V_6 C178 4.7u/6.3V_6 C268 4.7u/6.3V_6 C309 0.22u/10V_4 C121 0.22u/10V_4 C185 0.22u/10V_4 C310 0.22u/10V_4 C126 *180p/50V_4 C274 *180p/50V_4

If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows

U25F

A17 A19 A21 A23 A25 A27 A29 A31 B1 B3 C4 C33 D5 D9 D11 D13 D15 D17 D19 D21 D23 D25 D30 E4 E27 E29 E30 E33 F5 F6 F7 F8 F17 F20 F23 F28 F29 G1 G2 G4 G15 G19 G25 G26 G27 G33 H8 H9 H22 H26 J4 J8 J9 J11 J23 J25 J26 J27 J30 K9 K11 K12 K14 K15 K17 K19 K20 K22 L1 L2 L4 M8 M23 M25 N4 N11 N12 N14 N15 N17 N19 N20 N22 R1 R2 R4 T9 T11 T12 T14 T15 T17 T19 T20 T22 U4 W1 W2 W4 W5 W6 W7 Y9 — VSS

Y11 Y12 Y14 Y15 Y17 Y19 Y20 Y22 AA4 AA5 AB7 AB8 AC1 AC2 AC4 AC9 AC11 AC12 AC14 AC15 AC17 AC19 AC20 AC22 AC23 AC25 AE4 AF9 AF11 AF12 AF14 AF15 AF17 AF19 AF20 AF22 AF23 AF25 AG1 AG2 AG4 AG9 AG11 AG26 AH7 AH17 AH20 AH23 AH26 AH30 AJ4 AJ5 AJ6 AJ7 AJ9 AJ14 AJ15 AJ19 AJ22 AJ27 AJ28 AJ33 AK6 AK8 AK25 AK28 AK30 AL1 AL2 AL4 AL8 AL11 AL27 AL28 AL33 AM5 AM7 AM9 AM11 AM15 AM17 AM19 AM21 AM23 AM25 AM29 AM30 AN3 AN4 AN33 AP5 AP9 AR2 AR5 AR9 AR17 AR19 AR21 AR23 AR25 AR27 AR29 AR31 — VSS

SP@TRINITY APU_BGA813

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PROJECT : ZRP

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	APU 4/4(POWER/GND)	A1A

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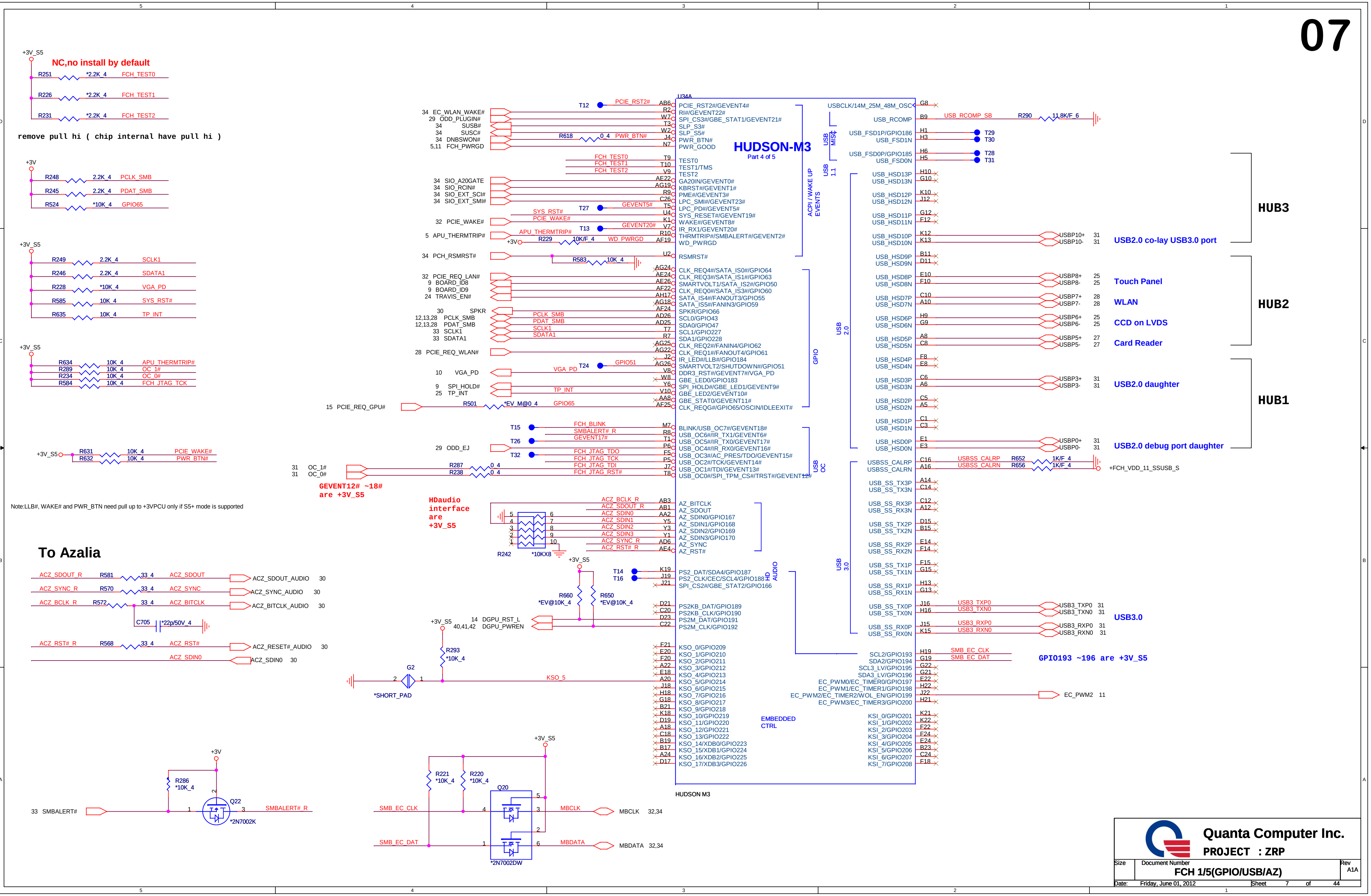

NC,no install by default
R251 *2.2K_4 FCH_TEST0
R226 *2.2K_4 FCH_TEST1
R231 *2.2K_4 FCH_TEST2
remove pull hi (chip internal have pull hi)
R248 2.2K_4 PCLK_SMB
R245 2.2K_4 PDAT_SMB
R524 *10K_4 GPIO65
R249 2.2K_4 SCLK1
R246 2.2K_4 SDATA1
R228 *10K_4 VGA_PD
R585 10K_4 SYS_RST#
R635 10K_4 TP_INT
R634 10K_4 APU_THERMTRIP#
R289 10K_4 OC_1#
R234 10K_4 OC_0#
R584 10K_4 FCH_JTAG_TCK
R631 10K_4 PCIE_WAKE#
R632 10K_4 PWR_BTN#
Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported
GEVENT12# ~18# are +3V_S5
HDaudio interface are +3V_S5
To Azalia
ACZ_SDOUT_R R581 33_4 ACZ_SDOUT ACZ_SDOUT_AUDIO 30
ACZ_SYNC_R R570 33_4 ACZ_SYNC ACZ_SYNC_AUDIO 30
ACZ_BCLK_R R572 33_4 ACZ_BITCLK ACZ_BITCLK_AUDIO 30
C705 *22p/50V_4
ACZ_RST#_R R568 33_4 ACZ_RST# ACZ_RESET#_AUDIO 30
ACZ_SDIN0 ACZ_SDIN0 30
33 SMBALERT# R286 *10K_4 Q22 *2N7002K SMBALERT#_R
SMB_EC_CLK R221 *10K_4 R220 *10K_4 Q20 *2N7002DW MBCLK 32,34
SMB_EC_DAT MBDATA 32,34
G2 *SHORT_PAD KSO_5
R293 *10K_4 14 DGPU_RST_L 40,41,42 DGPU_PWREN
R660 *EV@10K_4 R650 *EV@10K_4
U34A
HUDSON-M3
Part 4 of 5
HUDSON M3
PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
GPIO
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209 … KSO_17/XDB3/GPIO226
EMBEDDED CTRL
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P … USB_HSD0N
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P … USB_SS_RX0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201 … KSI_7/GPIO208
R290 11.8K/F_6 USB_RCOMP_SB
HUB3
USBP10+ USBP10- 31 USB2.0 co-lay USB3.0 port
HUB2
USBP8+ USBP8- 25 Touch Panel
USBP7+ USBP7- 28 WLAN
USBP6+ USBP6- 25 CCD on LVDS
USBP5+ USBP5- 27 Card Reader
HUB1
USBP3+ USBP3- 31 USB2.0 daughter
USBP0+ USBP0- 31 USB2.0 debug port daughter
R652 1K/F_4 R656 1K/F_4 USBSS_CALRP USBSS_CALRN +FCH_VDD_11_SSUSB_S
USB3_TXP0 USB3_TXN0 USB3_RXP0 USB3_RXN0 31 USB3.0
SMB_EC_CLK SMB_EC_DAT
GPIO193 ~196 are +3V_S5
EC_PWM2 11
Quanta Computer Inc.
PROJECT : ZRP
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FCH 1/5(GPIO/USB/AZ)
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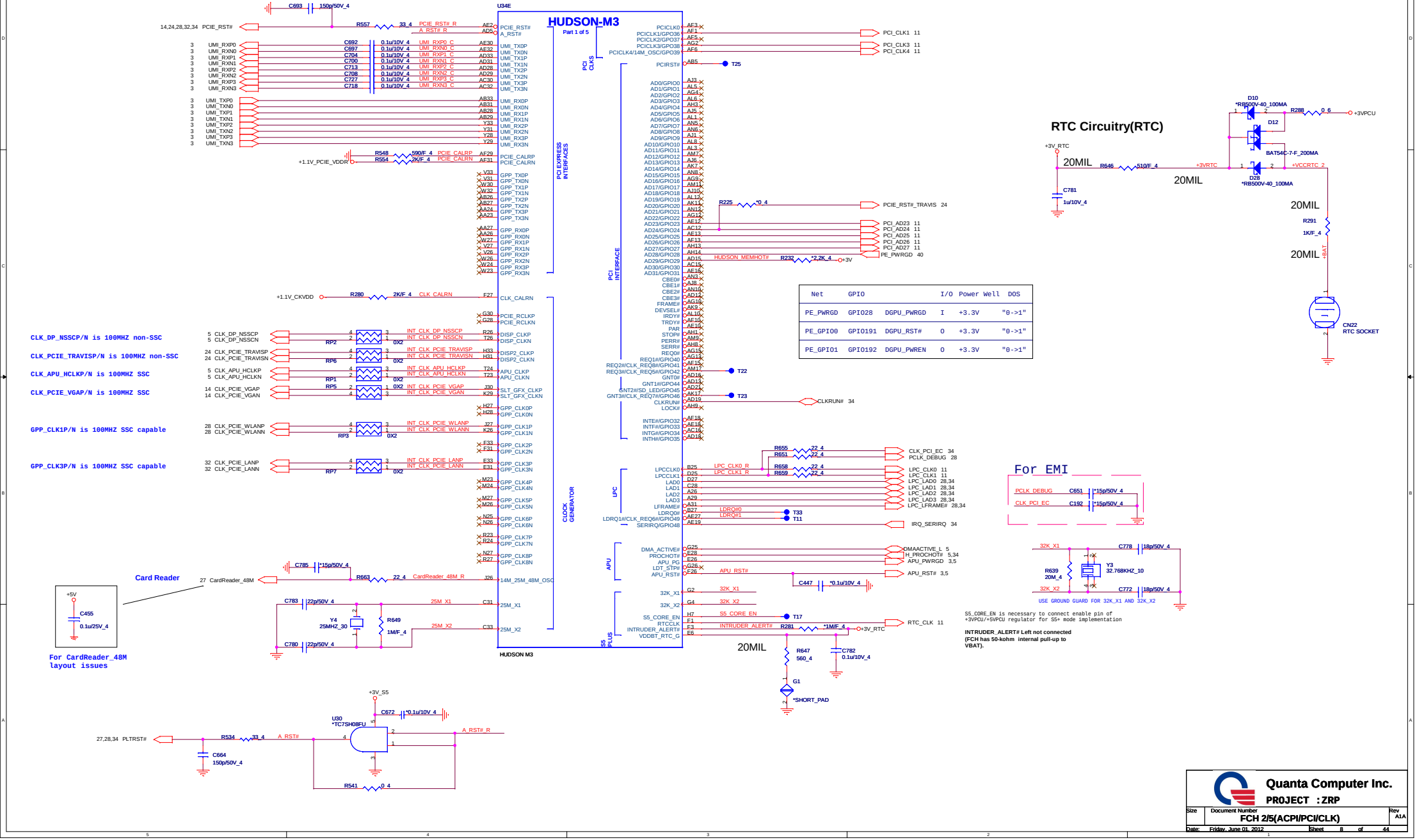
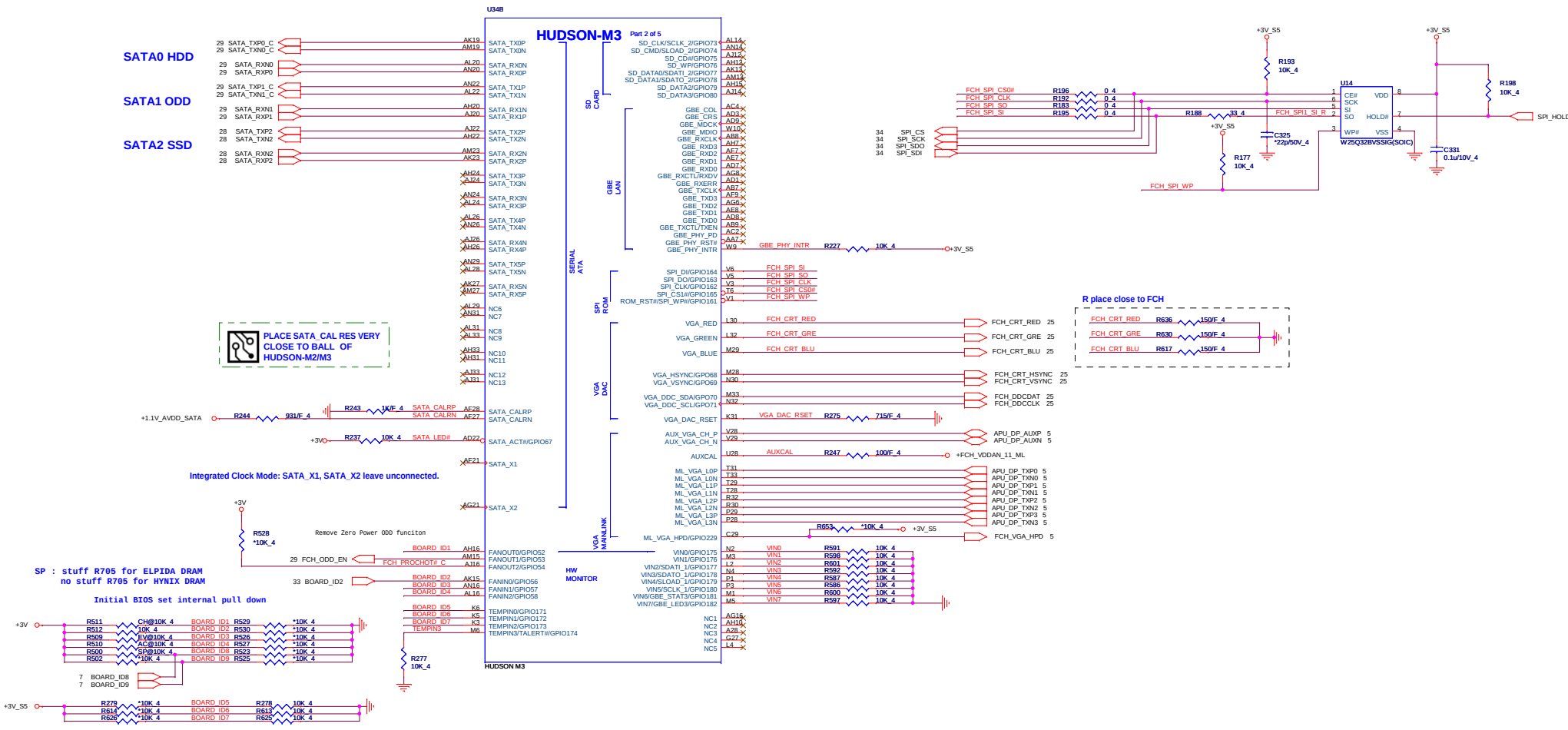


Net	GPIO		I/O	Power Well	DOS
PE_PWRGD	GPIO28	DGPU_PWRGD	I	+3.3V	"0->1"
PE_GPIO0	GPIO191	DGPU_RST#	O	+3.3V	"0->1"
PE_GPIO1	GPIO192	DGPU_PWREN	O	+3.3V	"0->1"



BOARD ID SETTING

ID5,ID6,ID7 S5 Power State

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
USB Charge No USB Charge	H L								
Synaptics ELAN		H L							
VGA SKU UMA SKU			H L						
AC No AC				H L					
Reserve					H L				
Reserve						H L			
Reserve							H L		
ELPIDA DRAM HYNIX DRAM								H L	
Reserve									H L

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	FCH 3/5(SATA/VGA/GND/SPI)	A1A

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

HUDSON-M3 Part 3 of 5

VDDQ--3.3V I/O power 102mA

VDD-- S/B CORE power 1007mA

CKVDD_1.1V-- Internal clock Generator I/O power 340mA

Check +1.1V_CKVDD leakage issues

PCIE_VDDR--PCIE I/O power 1088mA

AVDD_SATA--SATA phy power 1337mA

S5 plus mode

S5_3.3--3.3v standby power 59mA

S5_1.1V--1.1V standby power 5mA

Check pull down or not

Check to connect +3.3V A-test

HUDSON-M3 Part 5 of 5

Quanta Computer Inc.
PROJECT : ZRP

FCH 4/5(POWER)

Size | Document Number | Rev A1A

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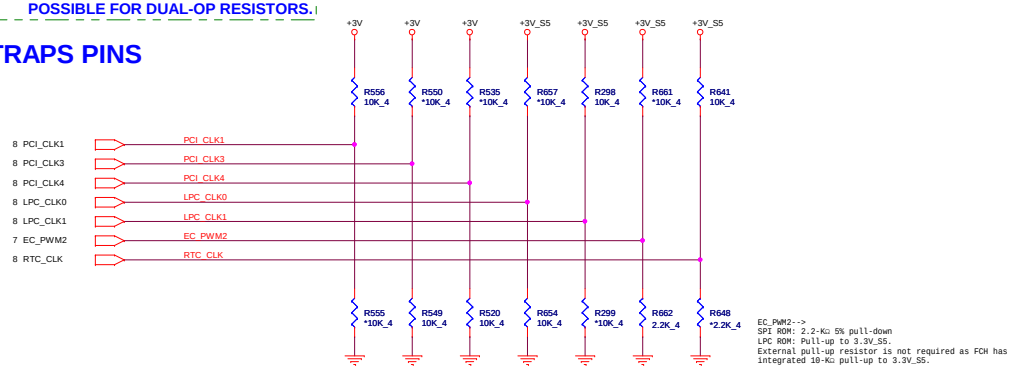
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

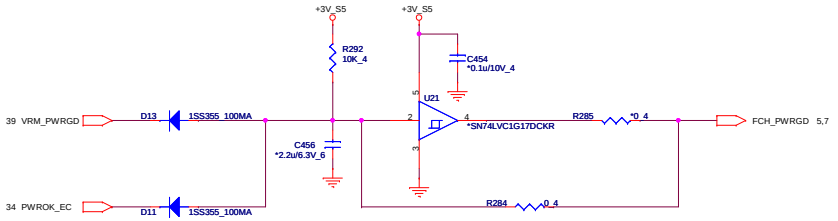


Remove PCI_CLK2 function

REQUIRED STRAPS

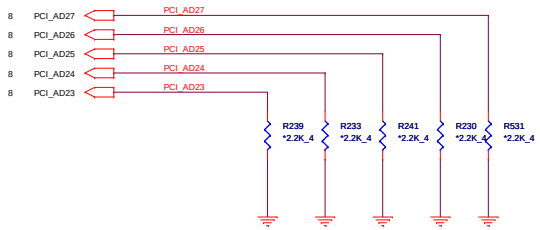
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

FCH PWRGD CKT



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

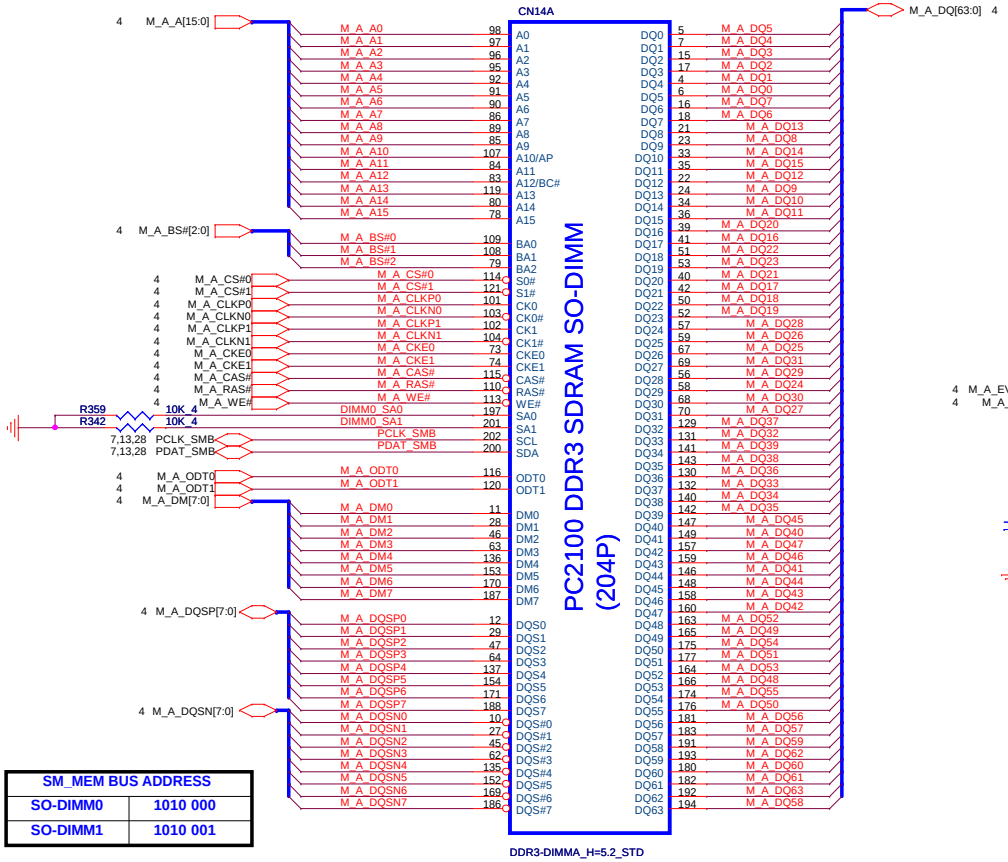
Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	A1A

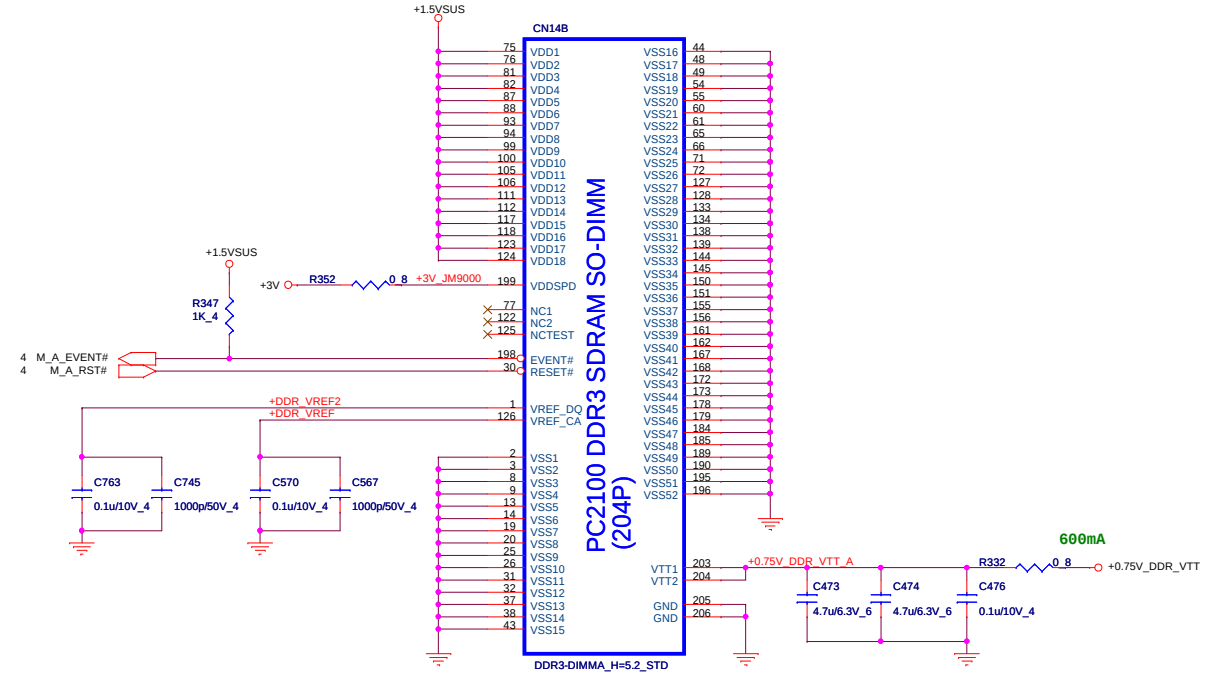
Date: Friday, June 01, 2012 Sheet 11 of 44

DDR3 DIMM-A

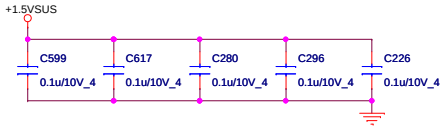
+1.5VSUS 4,5,6,13,24,36,39,41
+0.75V_DDR_VTT 13,36,43
+3V 3,5,7,8,9,10,11,13,14,24,25,26,27,28,29,30,33,34,35,36,37,38,39,40,41,42,43

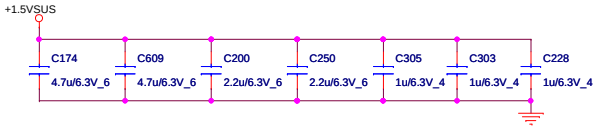


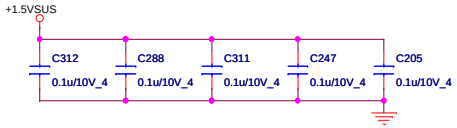
SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

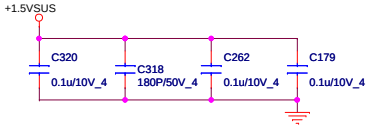


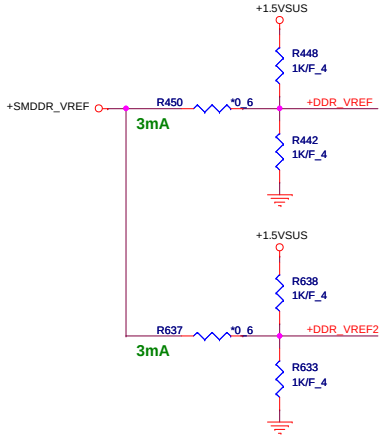
Place these Caps near So-Dimm A











Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	DDR3 SO-DIMM A	A1A
Date: Friday, June 01, 2012	Sheet 12 of 44	

<DDR>

4 M_B_DQSP[7:0]
4 M_B_DQSN[7:0]
4 M_B_DQ[63:0]

BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

U18 U15 U9 U3

100-BALL SDRAM DDR3 SP@RAM _DDR3

SP : ELPIDA DRAM P/N : AKD5JGST400
HYNIX DRAM P/N : AKD5JGQTW01

Should be 243 Ohms +-1%

R546 243/F_4 R169 243/F_4 R395 243/F_4 R350 243/F_4

U5 *M24C02-WMN6TP

address:A2

WP =1 : WRITE DISABLE

Place these Caps near Memory Down

+1.5VSUS

C554 C633 C703 C559 C637 C689 0.22u/10V_4

C733 C715 C696 C691 C732 0.22u/10V_4

+0.75V_DDR_VTT

C711 C667 C661 C497 C526 C634 0.22u/10V_4

C683 C380 C381 C382 C684 0.22u/10V_4

C514 C494 C527 C682 C547 C488 0.22u/10V_4

R566 R615 R602 R562 R578 R594 R261 R595 R578 R563 R577 R263 R560 R264 R573 R240 R561 R576 R593 R574 R564 R575 R562 R565 36/F_4

R590 R589 36/F_4

C734 0.1u/10V_4

R148 R404 1K/F_4

R140 R449 *0_6

C632 C686 C481 C230 C556 C666 C716 C571 0.1u/10V_4

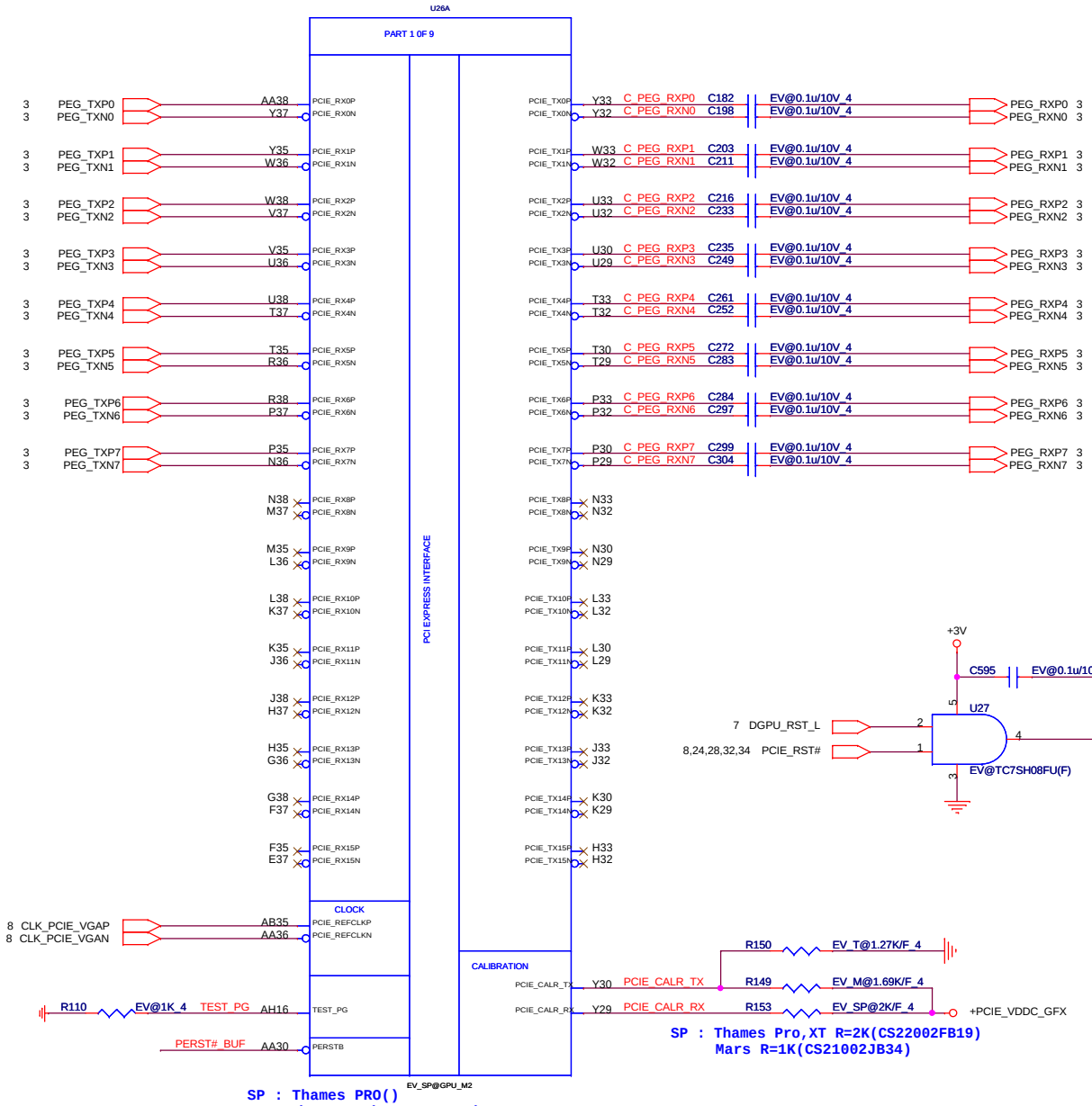
R446 R375 1K/F_4

+SMDDR_VREF

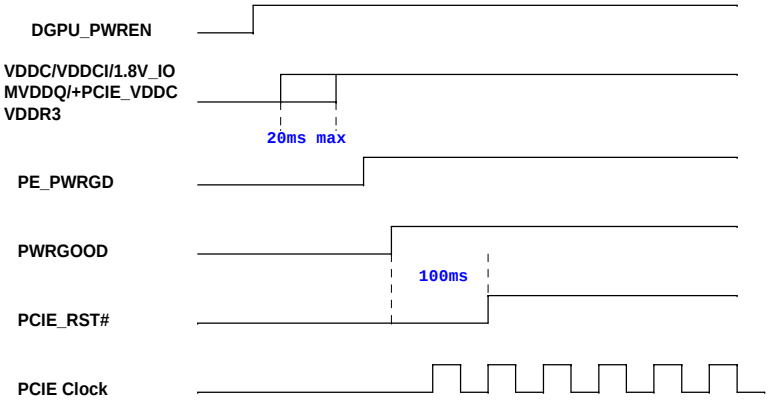
SMDDR_VREF_DQ1

Quanta Computer Inc.
PROJECT : ZRP

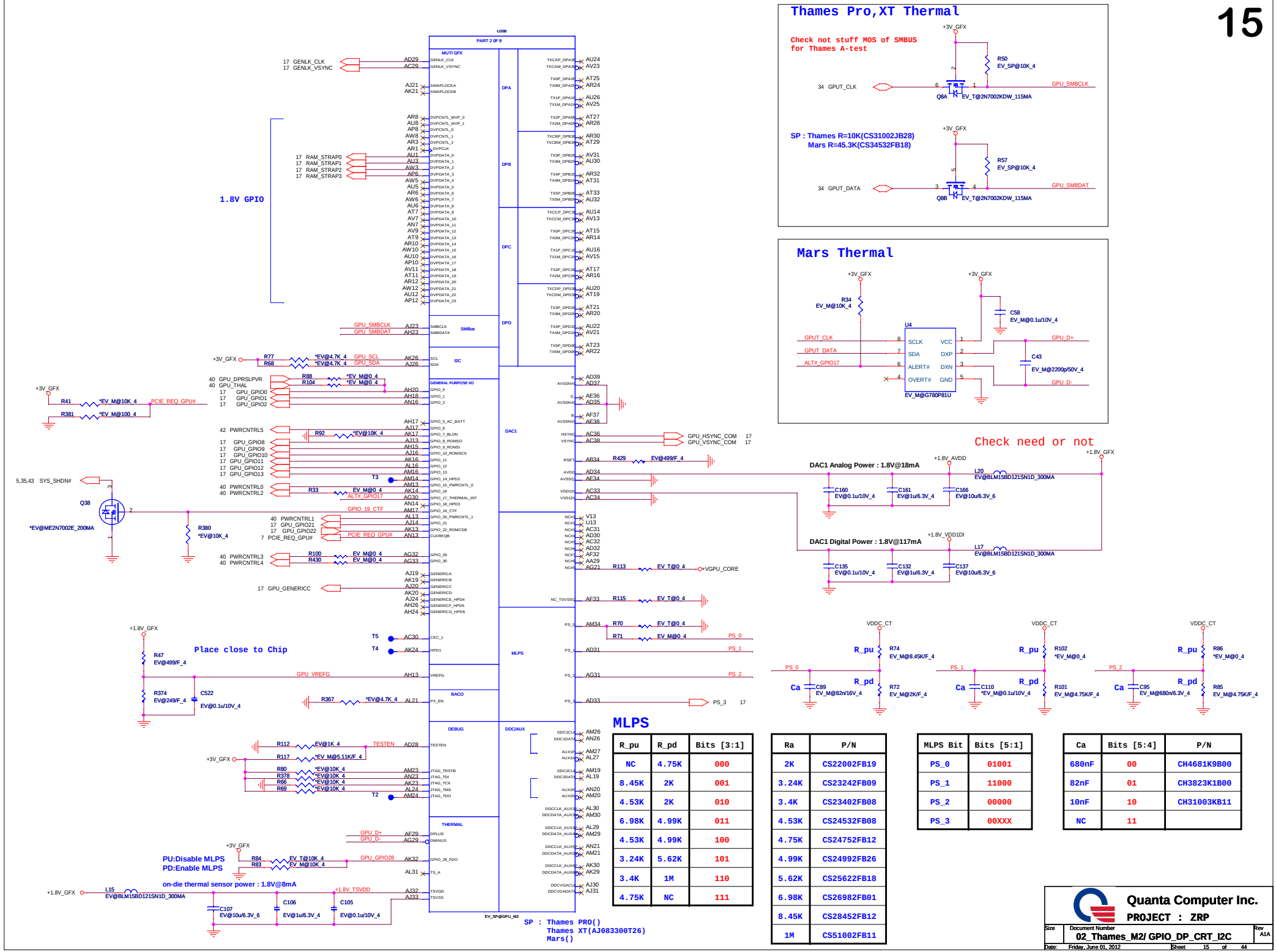
Size: Document Number: DDR3 MEMORY DOWNx16 B Rev: A1A
Date: Friday, June 01, 2012 Sheet 13 of 44



Thames(Pro,XT) and Mars Power-on sequence PX5.0(no BACO)



Quanta Computer Inc.			
PROJECT : ZRP			
Size	Document Number		Rev
	Thames_M2/ PEG*16		A1A
Date: Friday, June 01, 2012	Sheet 14 of 44		



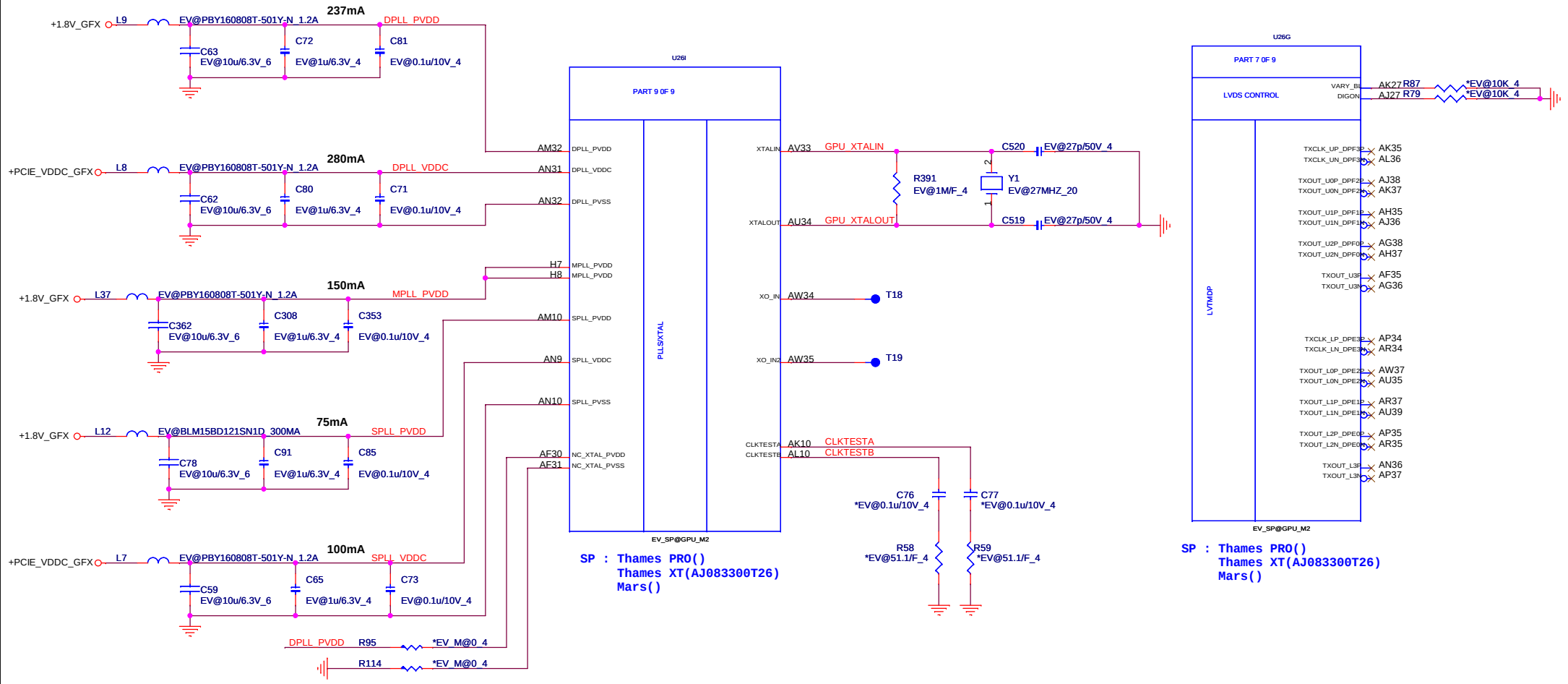
R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

MLPS Bit	Bits [5:1]
PS_0	01001
PS_1	11000
PS_2	00000
PS_3	00XXX

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

Size	Document Number: 02_Thames_M2/ GPIO_DP_CRT_I2C
Rev	A1A
Date:	Friday, June 01, 2012
Sheet	15 of 44



Quanta Computer Inc.

PROJECT : ZRP

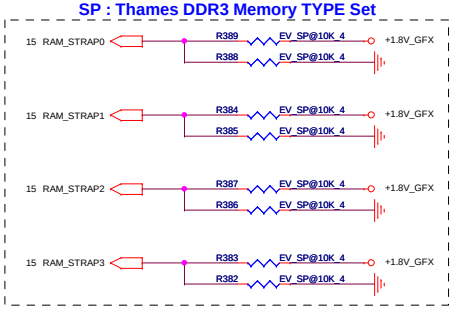
Size	Document Number	Rev
	Thames_M2/ XTAL_LVDS	A1A
Date: Friday, June 01, 2012	Sheet 16 of 44	

Vendor	Vendor P/N	STN B/S P/N	Size	Thames Pro,XT USE RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	Mars USE MLPS
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW05 * 8	1GB	0	0	0	0	000
	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW17 * 4	1GB	0	0	0	1	
		AKD5MGWTW17 * 8	2GB	0	0	1	0	001
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 8	1GB	0	1	0	0	010
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	1	
		AKD5MGWT500 * 8	2GB	0	1	1	0	011
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 8	1GB	1	0	0	0	100
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	1	0	0	1	
		AKD5DZWT700 * 8	2GB	1	0	1	0	101

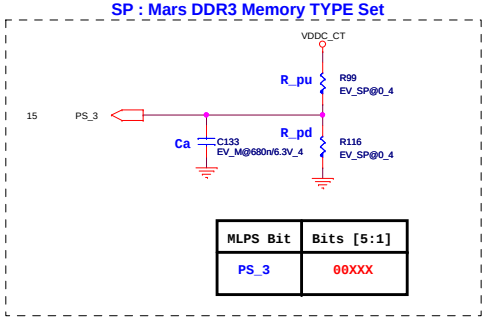
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	GENLK_CLK	Reserved	0
RESERVED	PS_1[2]	GPIO8	Reserved	0
RESERVED	NA	GPIO21	Reserved	0
RESERVED	NA	GENERICC	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

SP : Thames DDR3 Memory TYPE Set



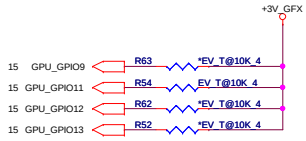
SP : Mars DDR3 Memory TYPE Set

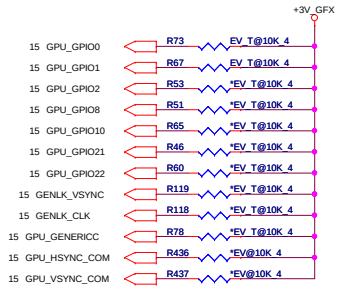


MLPS Bit	Bits [5:1]
PS_3	00XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	32M	1	1	0





MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/ STRAPS_Thermal	A1A

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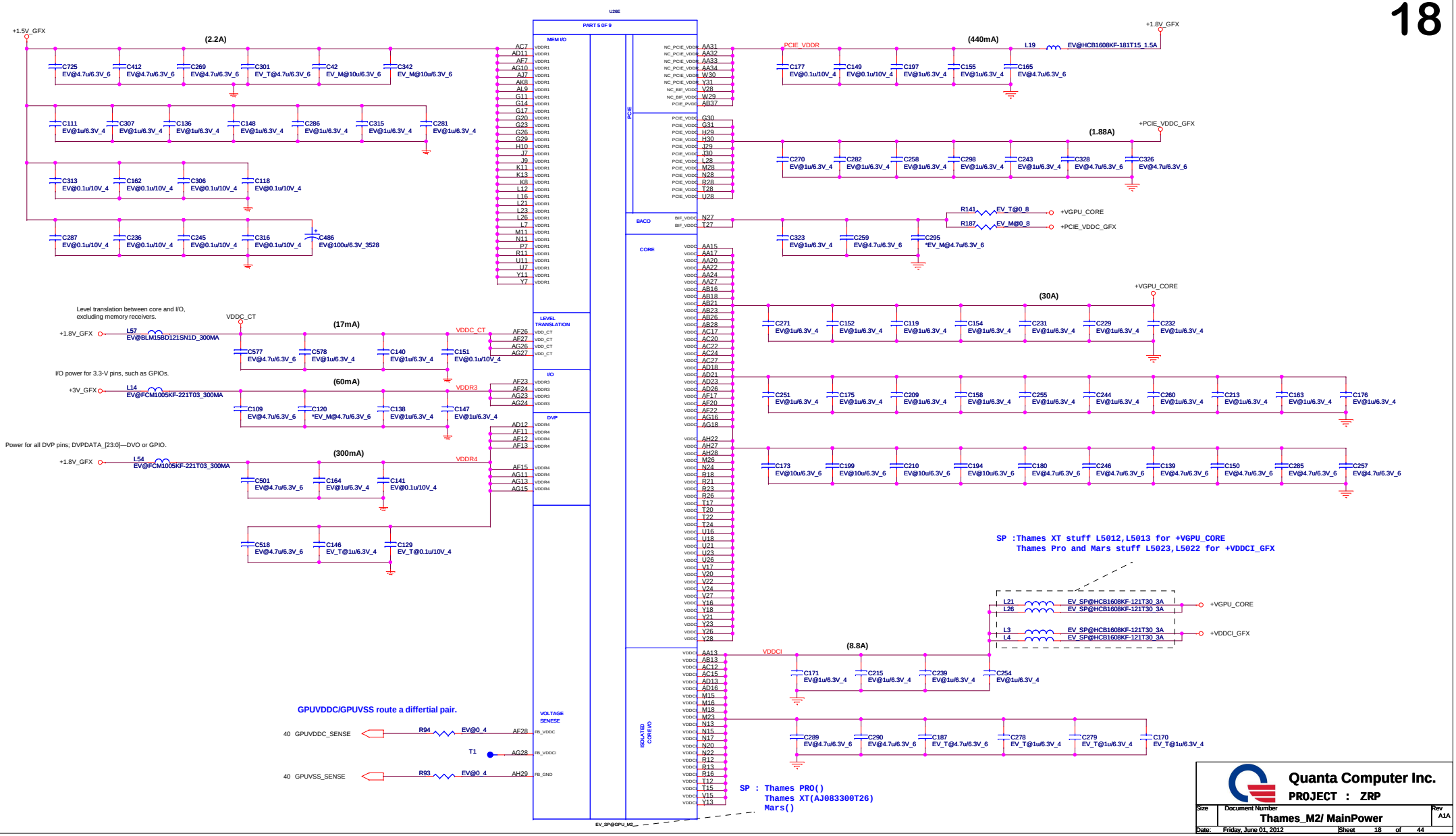
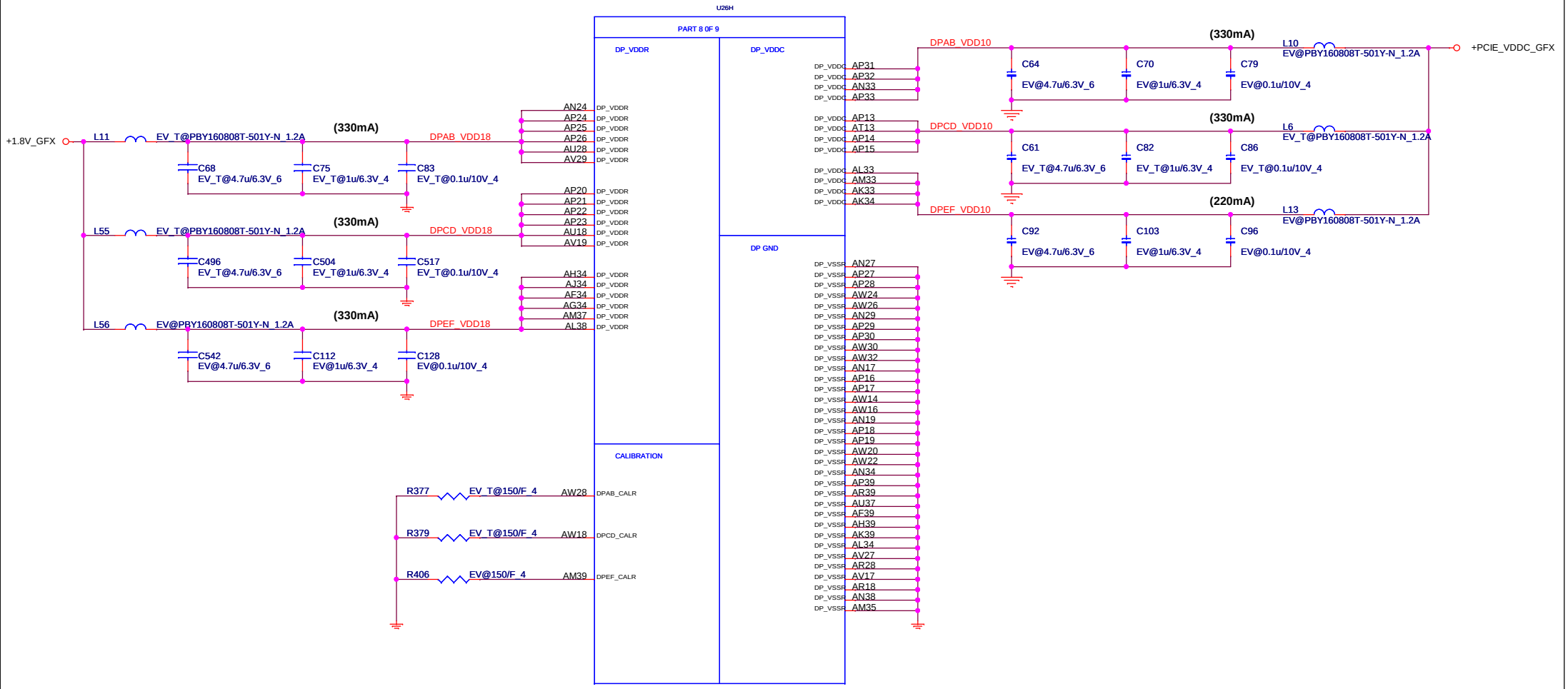


Quanta Computer Inc.			
PROJECT : ZRP			
Size	Document Number		Rev
	Thames_M2/ MainPower		A1A
Date: Friday, June 01, 2012	Sheet 18 of 44		

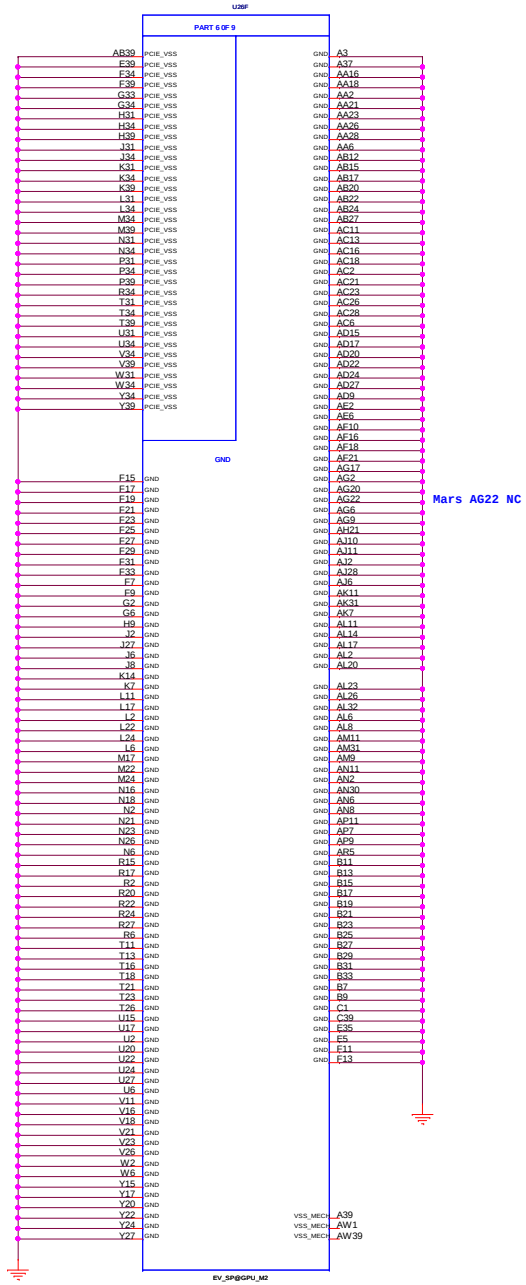


SP : Thames PRO()
Thames XT(AJ083300T26)
Mars()

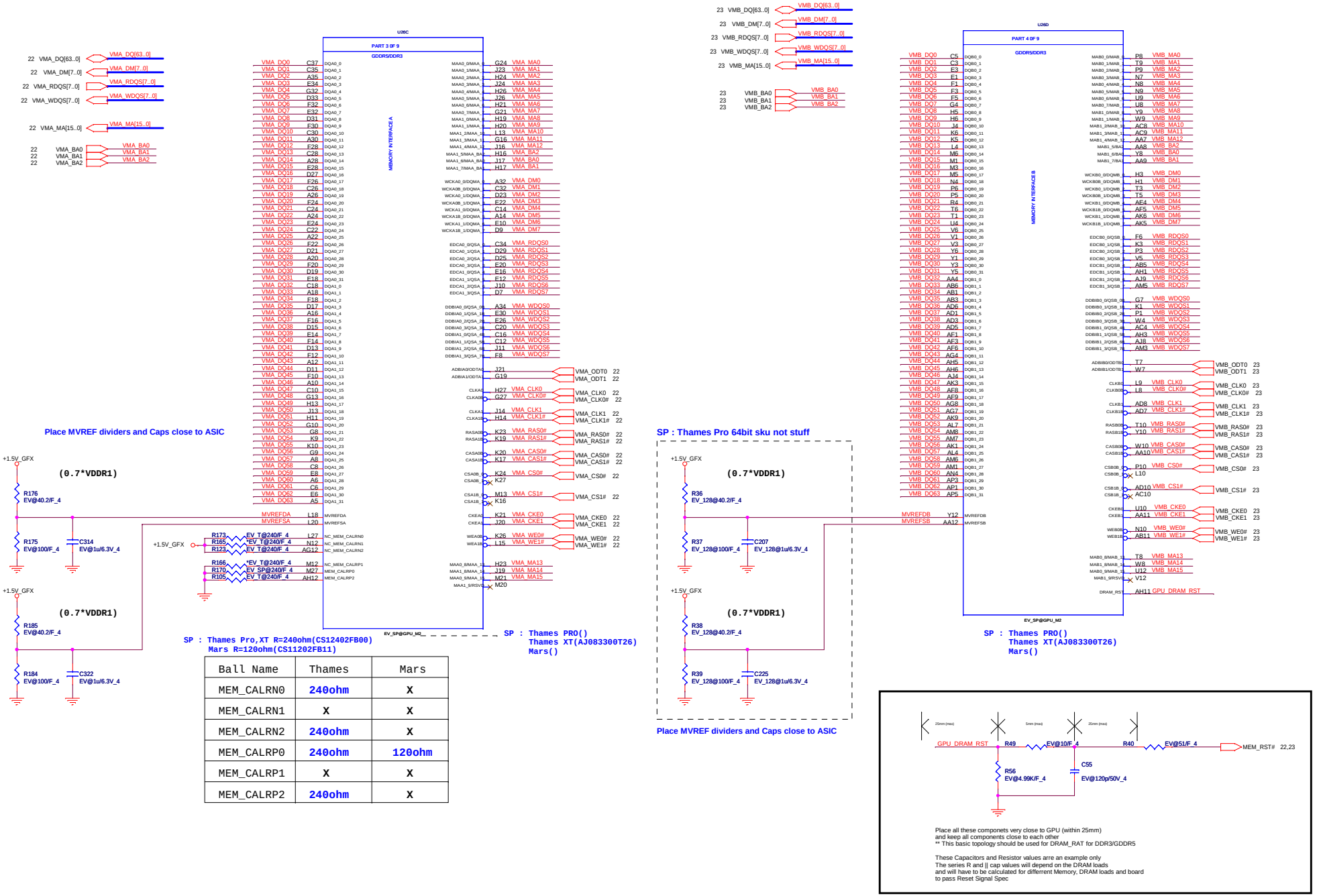
Quanta Computer Inc.

PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/ DP_Powers	A1A
Date: Friday, June 01, 2012	Sheet 19 of 44	



Quanta Computer Inc.		
PROJECT : ZRP		
Size	Document Number: Thames_M2/ GND	Rev: A1A
Date: Friday, June 01, 2012	Sheet 20 of 44	



Ball Name	Thames	Mars
MEM_CALRN0	240ohm	X
MEM_CALRN1	X	X
MEM_CALRN2	240ohm	X
MEM_CALRP0	240ohm	120ohm
MEM_CALRP1	X	X
MEM_CALRP2	240ohm	X

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/ MEM Interface	A1A

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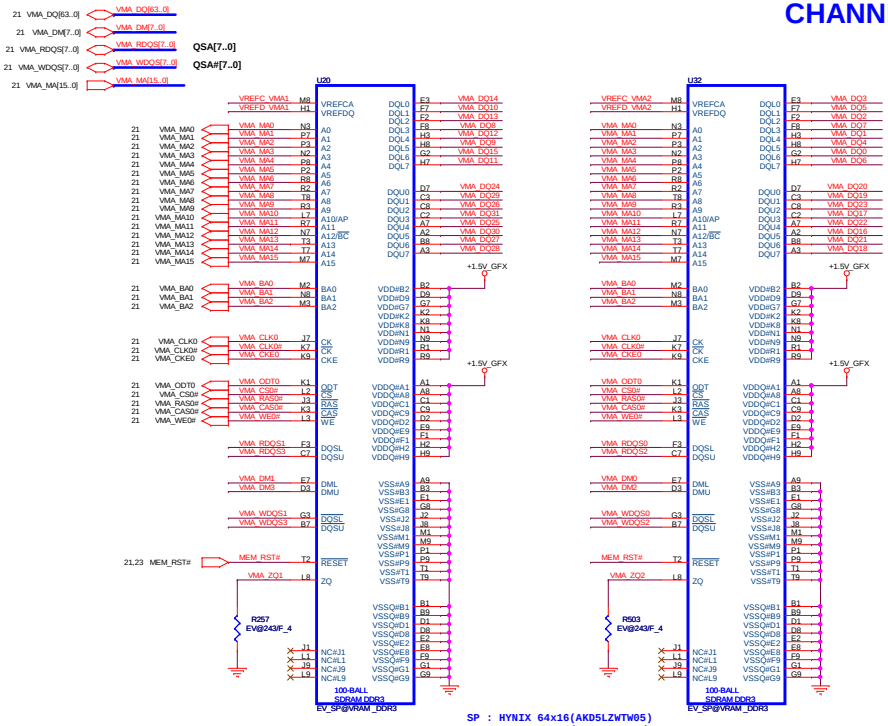
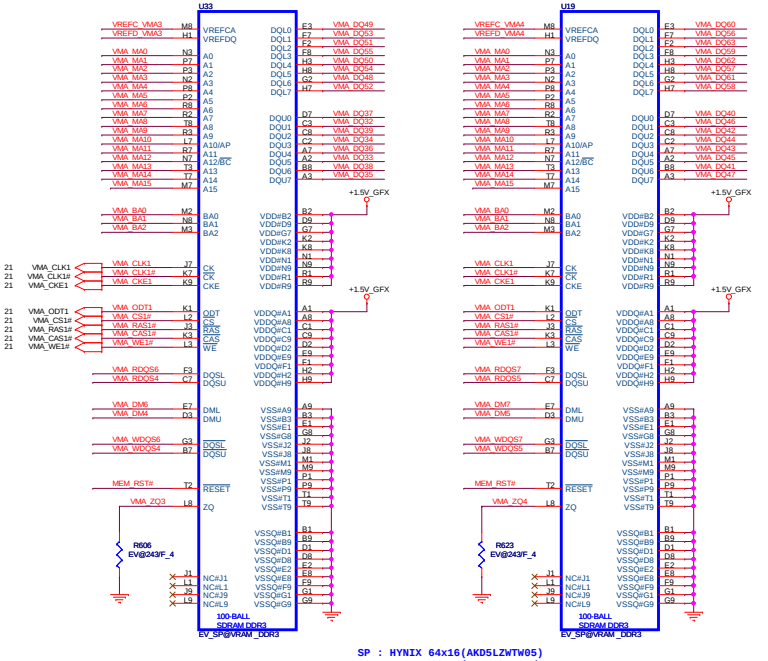
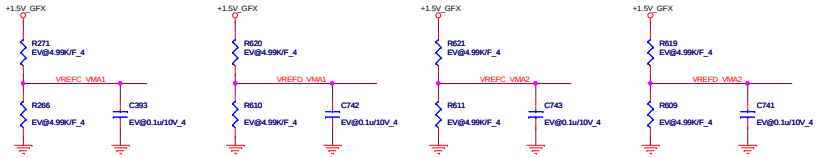
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

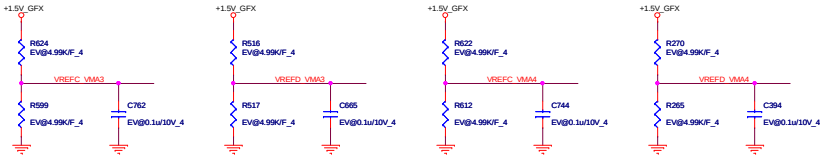




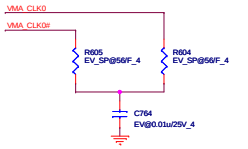
Group-A0 VREF



Group-A1 VREF

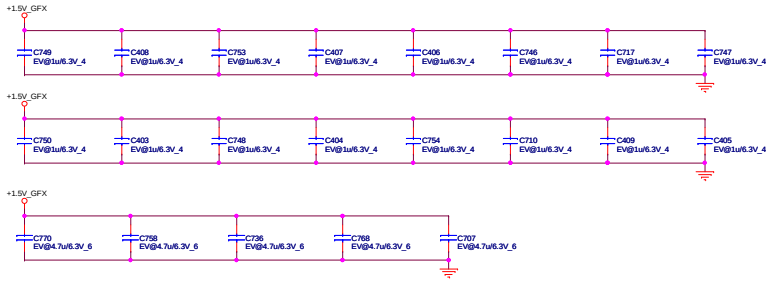


MEM_A0 CLK

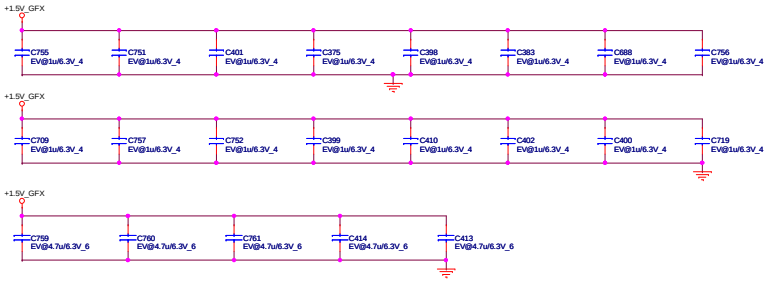


SP : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

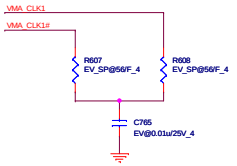
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



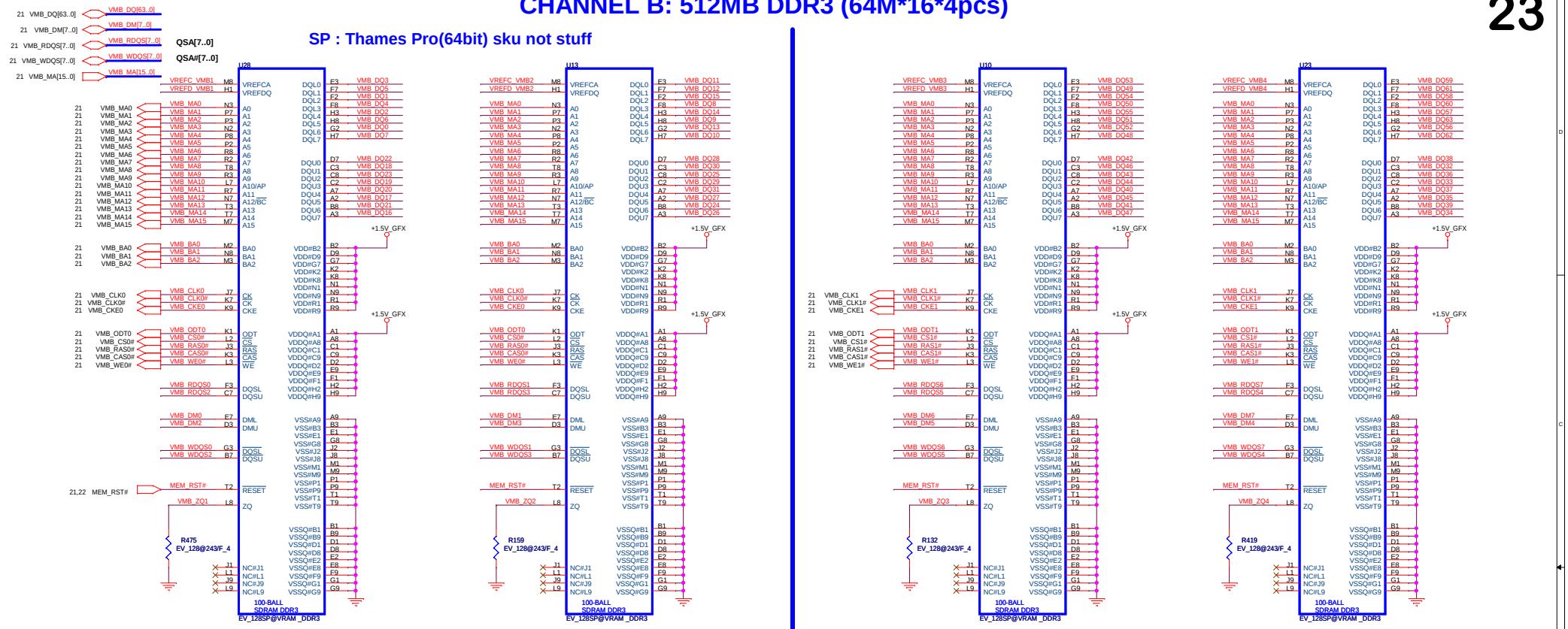
SP : Thames Pro,XT R=56ohm(CS05602FB07)
Mars R=40.2ohm(CS04022FB28)

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/VRAM_A	A1A
Date: Friday, June 01, 2012	Sheet 22 of 44	

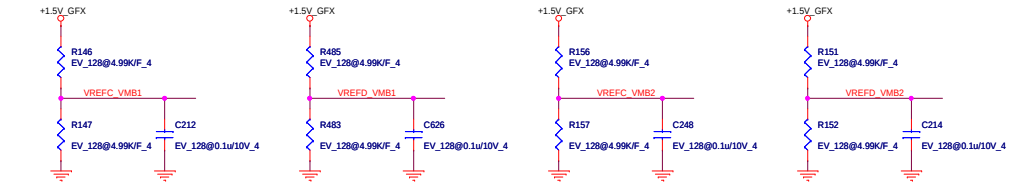
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

SP : Thames Pro(64bit) sku not stuff

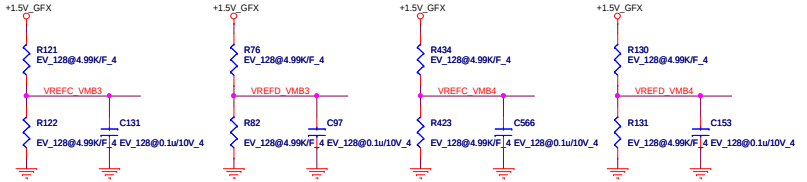


SP : HYNIX 64x16(AKD5LZWTW05)
HYNIX 128x16(AKD5MGWTW17)

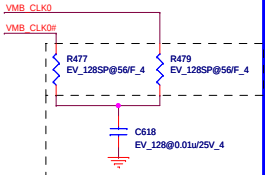
Group-B0 VREF



Group-B1 VREF

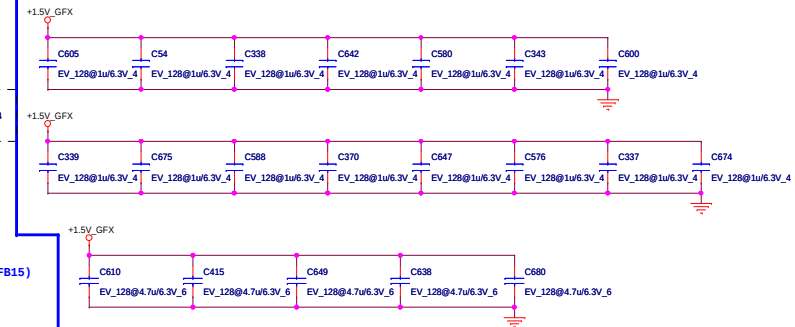


MEM_B0 CLK

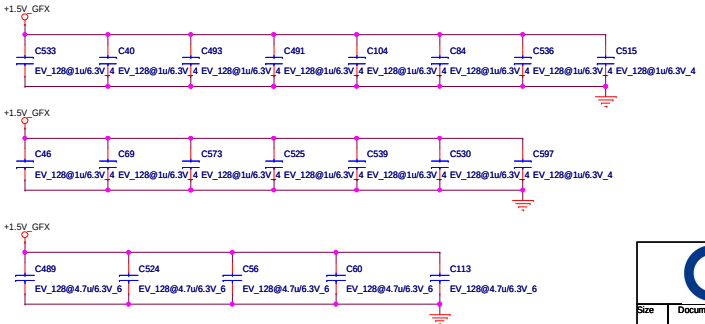


SP : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

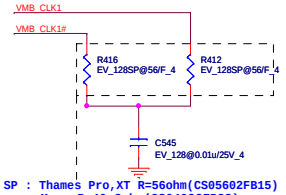
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



SP : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/VRAM_B	A1A
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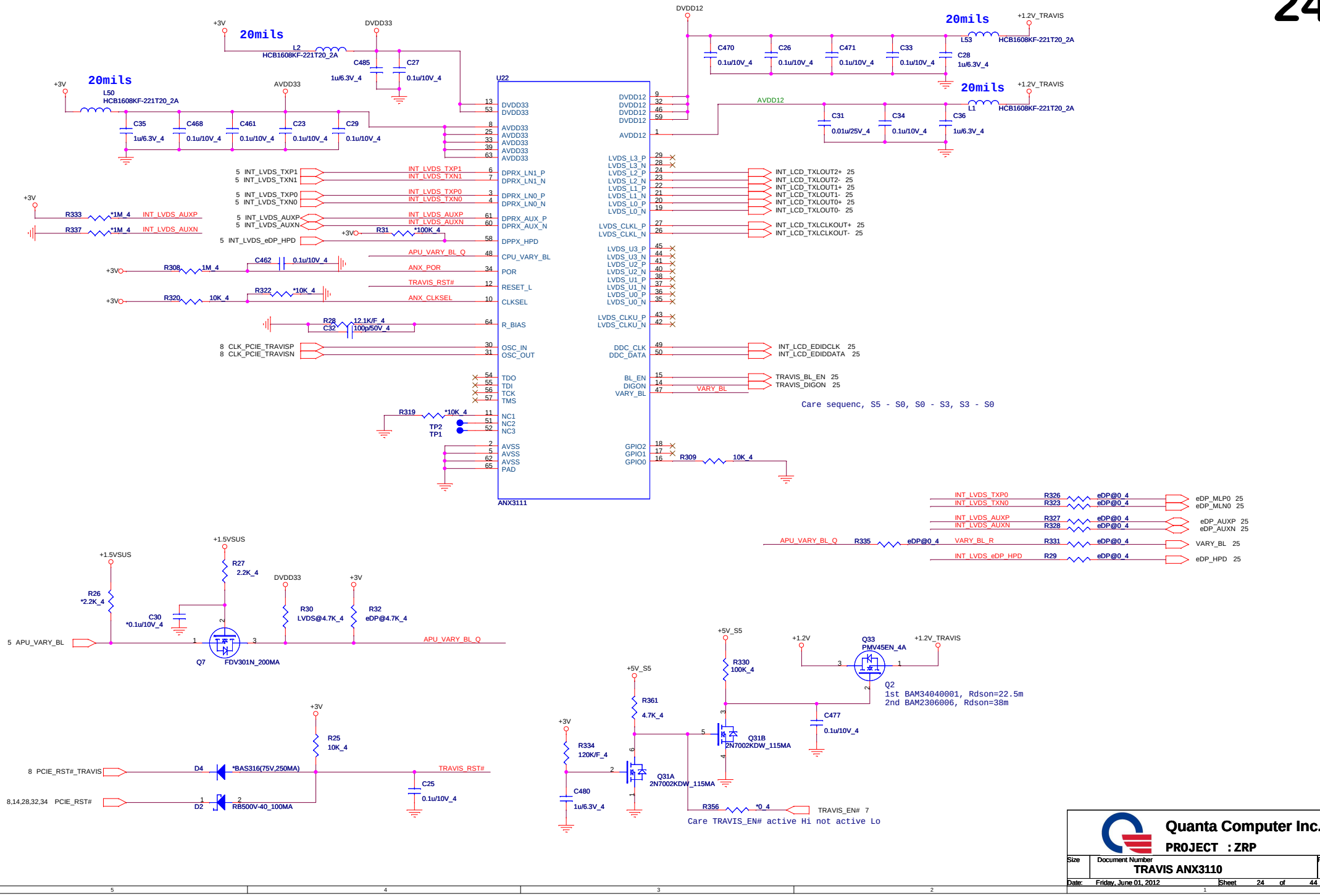

Quanta Computer Inc.

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Size	Document Number	Rev
	TRAVIS ANX3110	A1A
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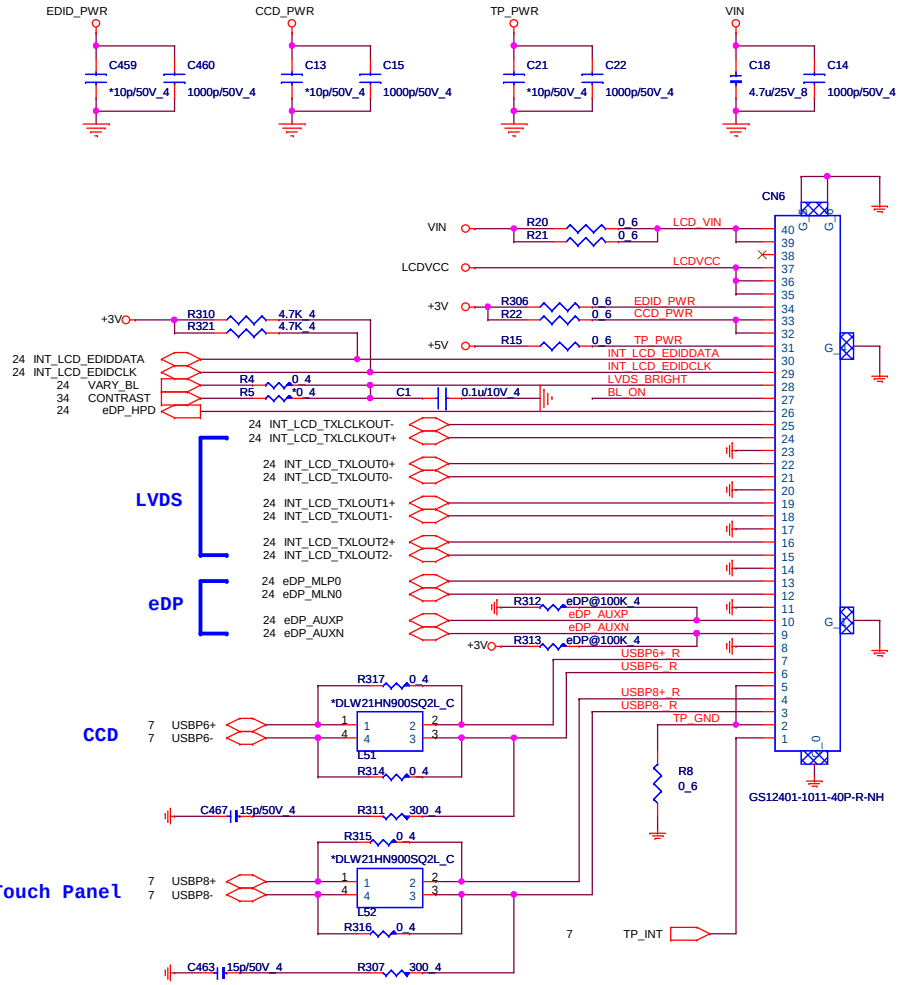
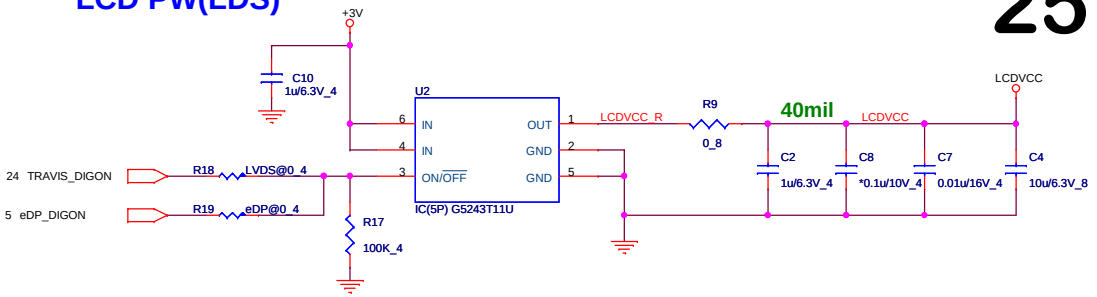
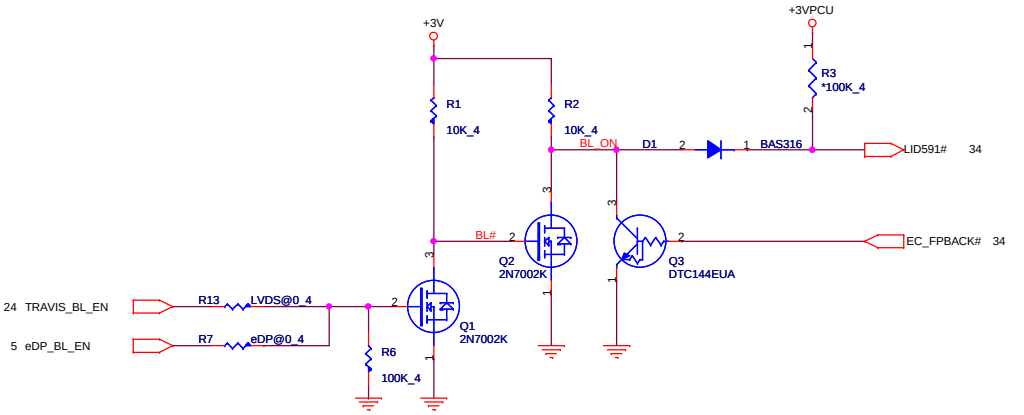
LVDS(LDS)



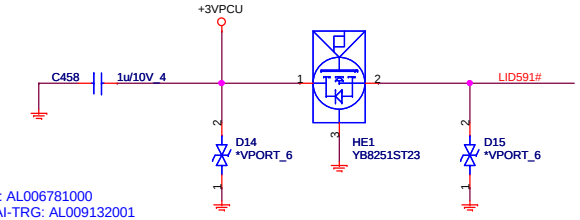
LCD PW(LDS)



Backlight Control(LDS)

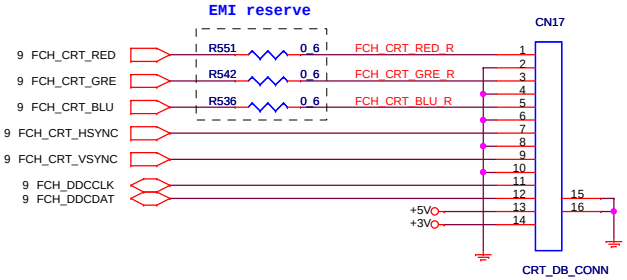


Lid Switch (HSR)



EM-6781-T3: AL006781000
APX9132H AI-TRG: AL009132001
AH9249NTR-G1: AL009249000

CRT DB



Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	LVDS&CCD&CRT DB&LID	A1A
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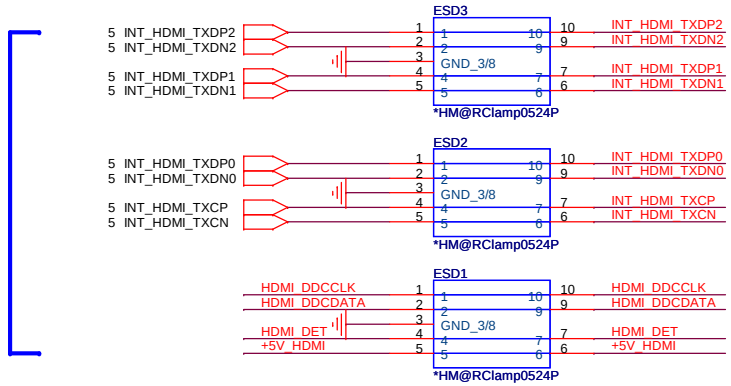
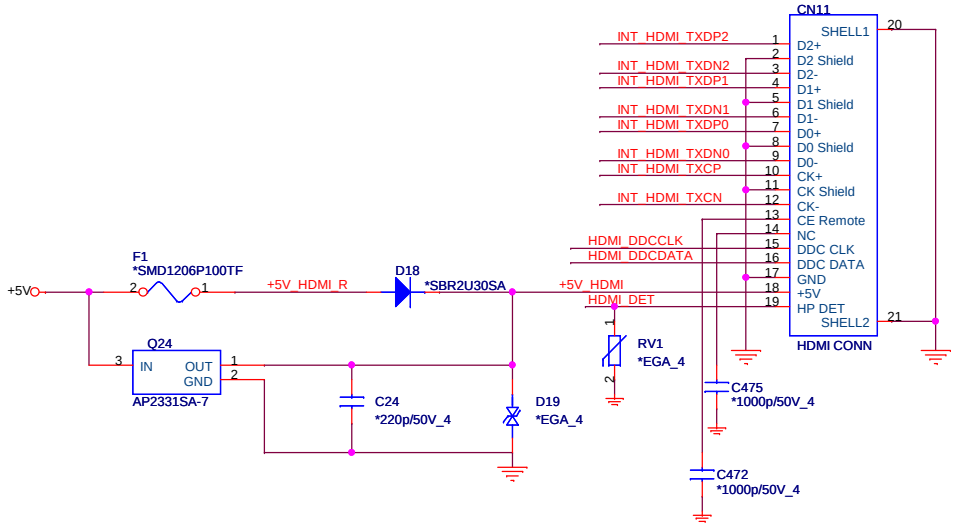
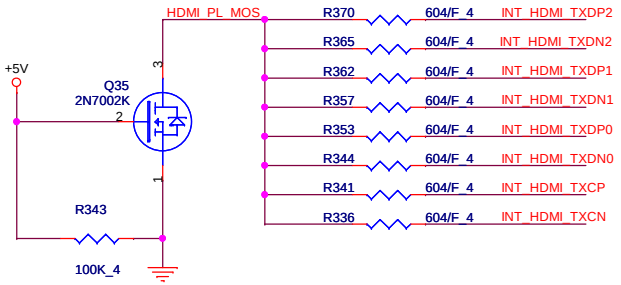
HDMI

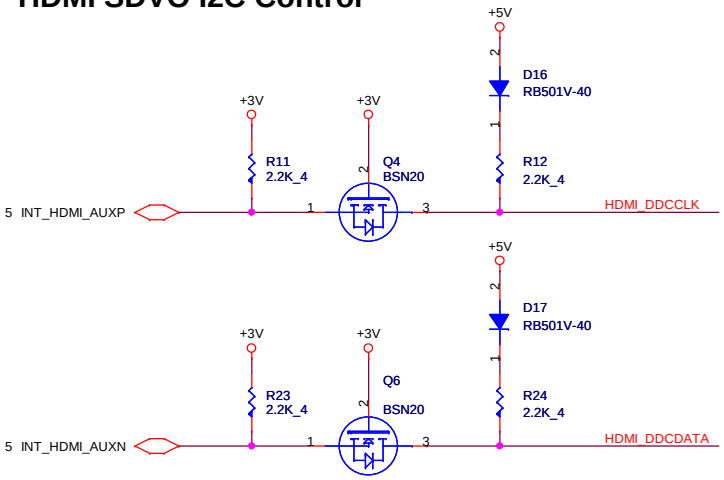
ESD



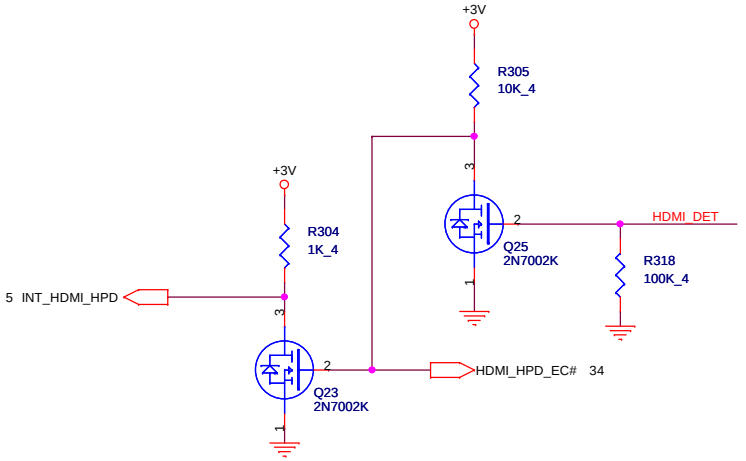




HDMI SDVO I2C Control

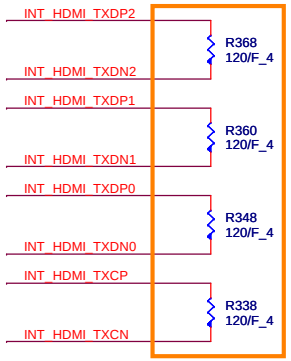


HDMI HPD SENSE



EMI reserve for HDMI(EMC)

Close connector



Quanta Computer Inc.

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	HDMI	A1A

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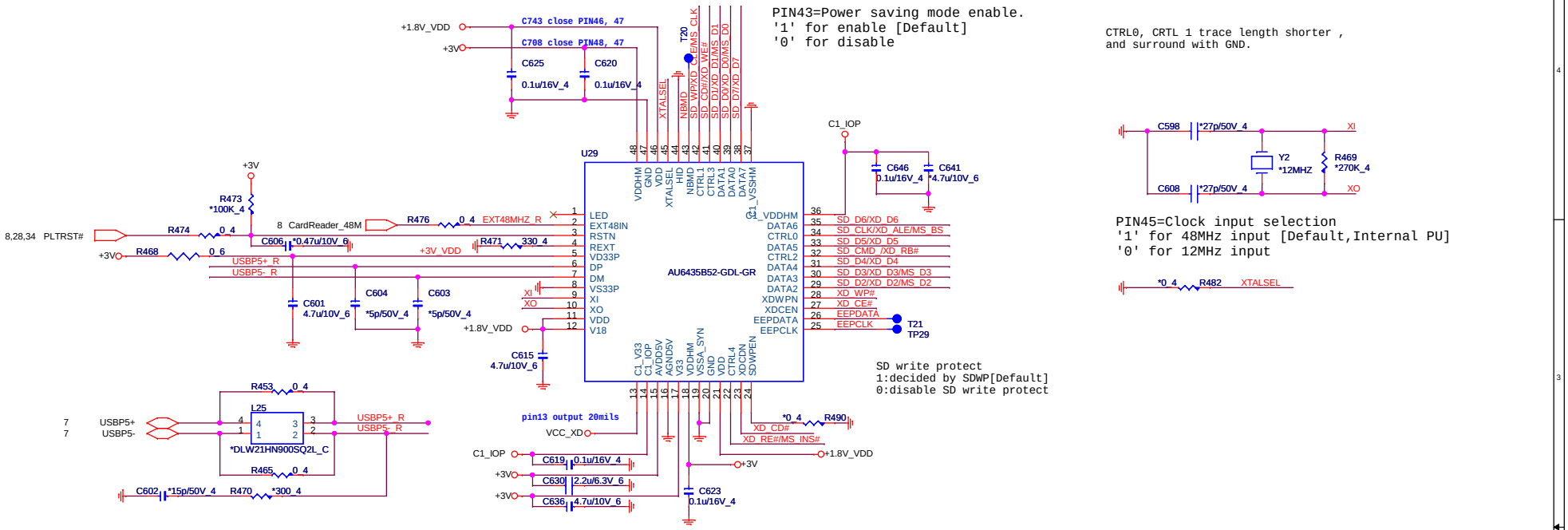
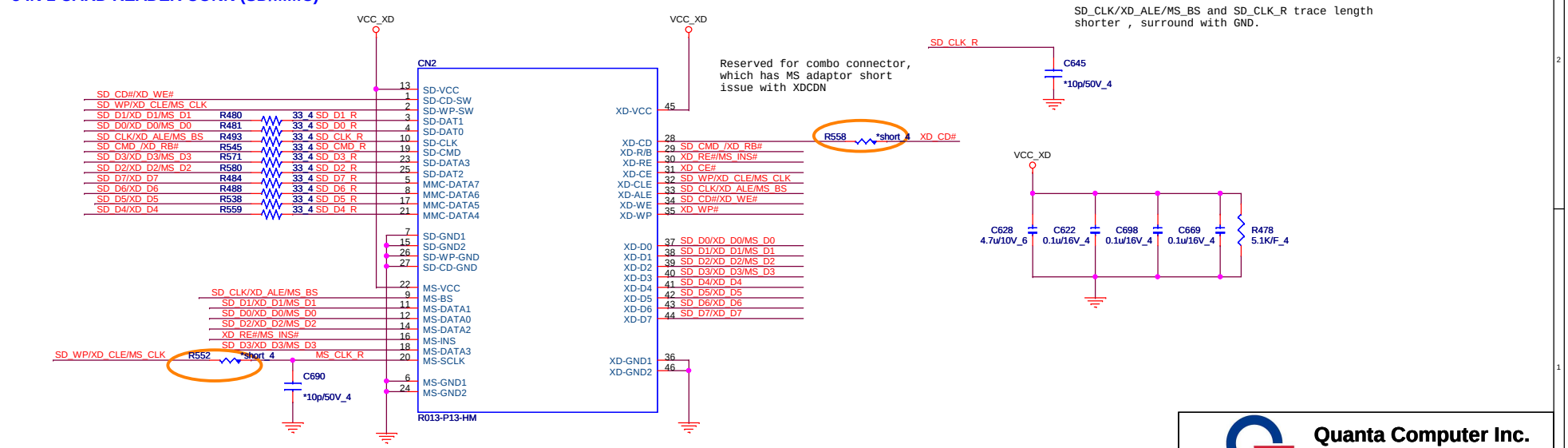
5 in 1 CARD READER IC (SD,MMC,xD,MS)



5 IN 1 CARD READER CONN (SD/MMC)



Quanta Computer Inc.			
PROJECT : ZRP			
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	CardReader (5 IN 1)		A1A
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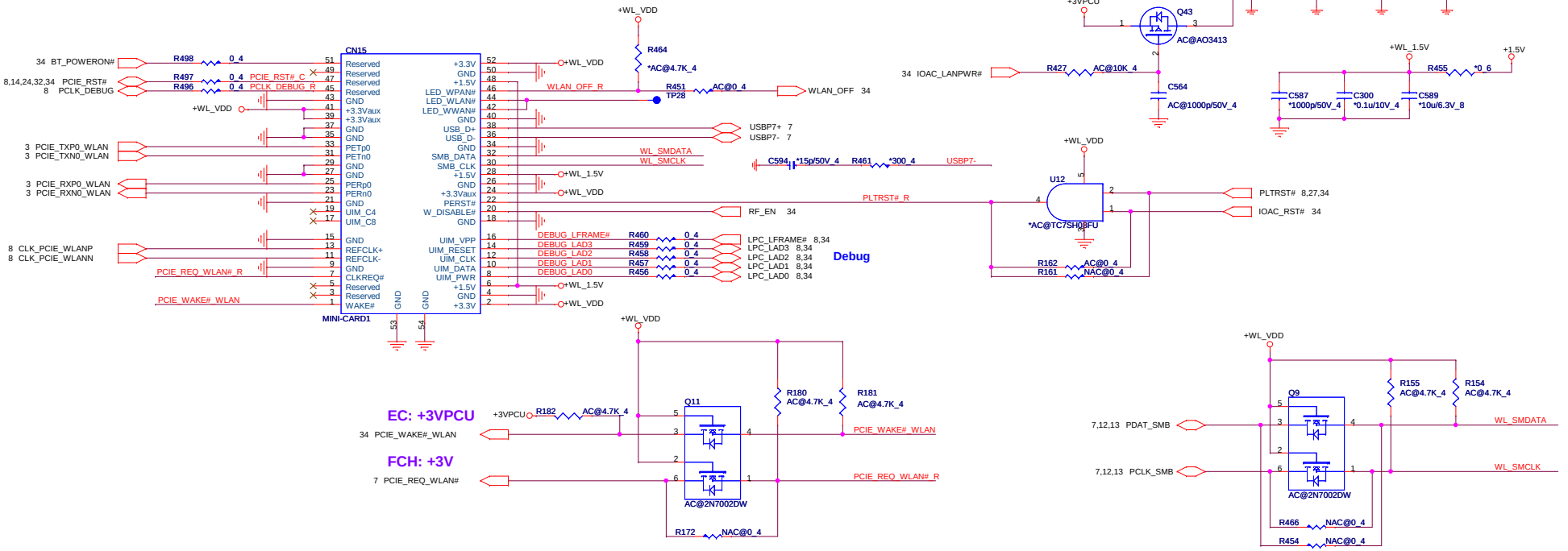
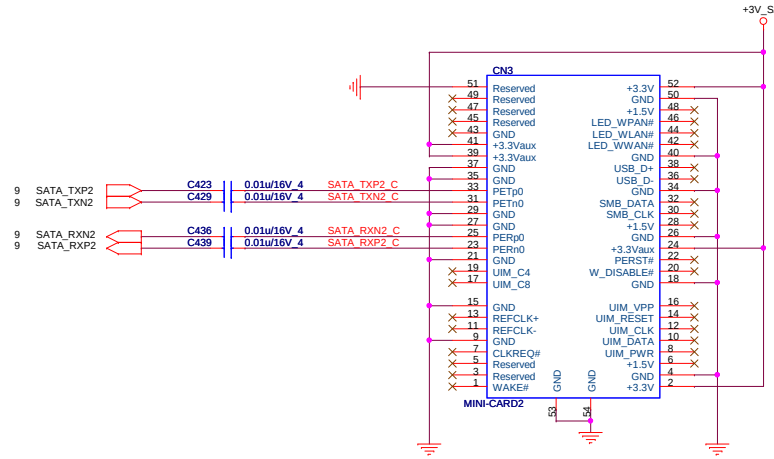
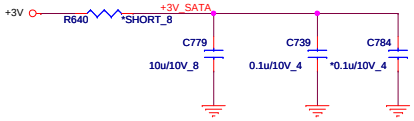
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



MINI-CARD SSD





rating = 1000mA @ 128G

Quanta Computer Inc.		
PROJECT : ZRP		
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	MINI PCIE(WLAN/SSD)	A1A
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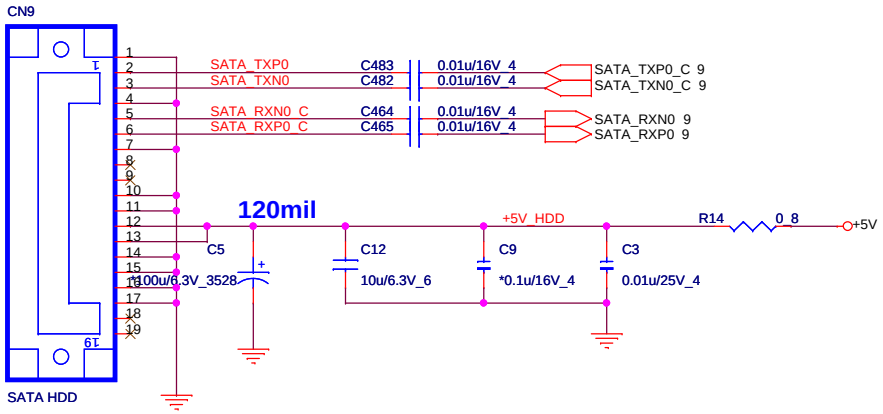
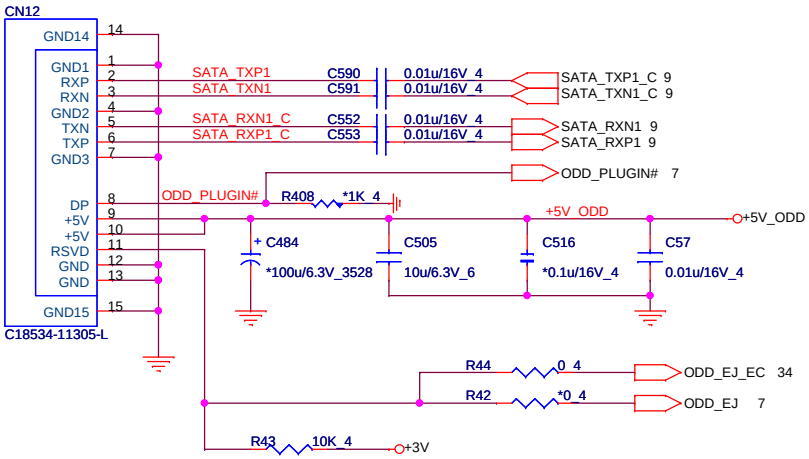
SATA HDD

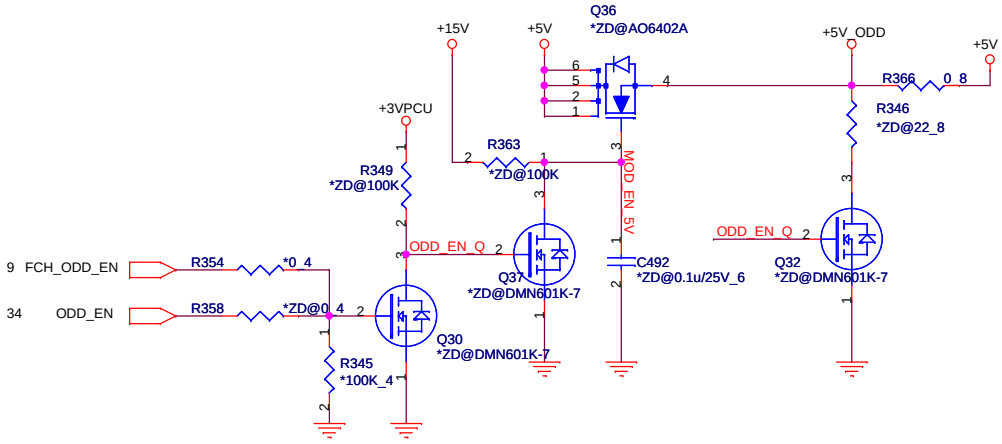
29



SATA ODD



Zero Power (ODD)



Quanta Computer Inc.

PROJECT : ZRP

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	SATA(HDD/ODD)	A1A
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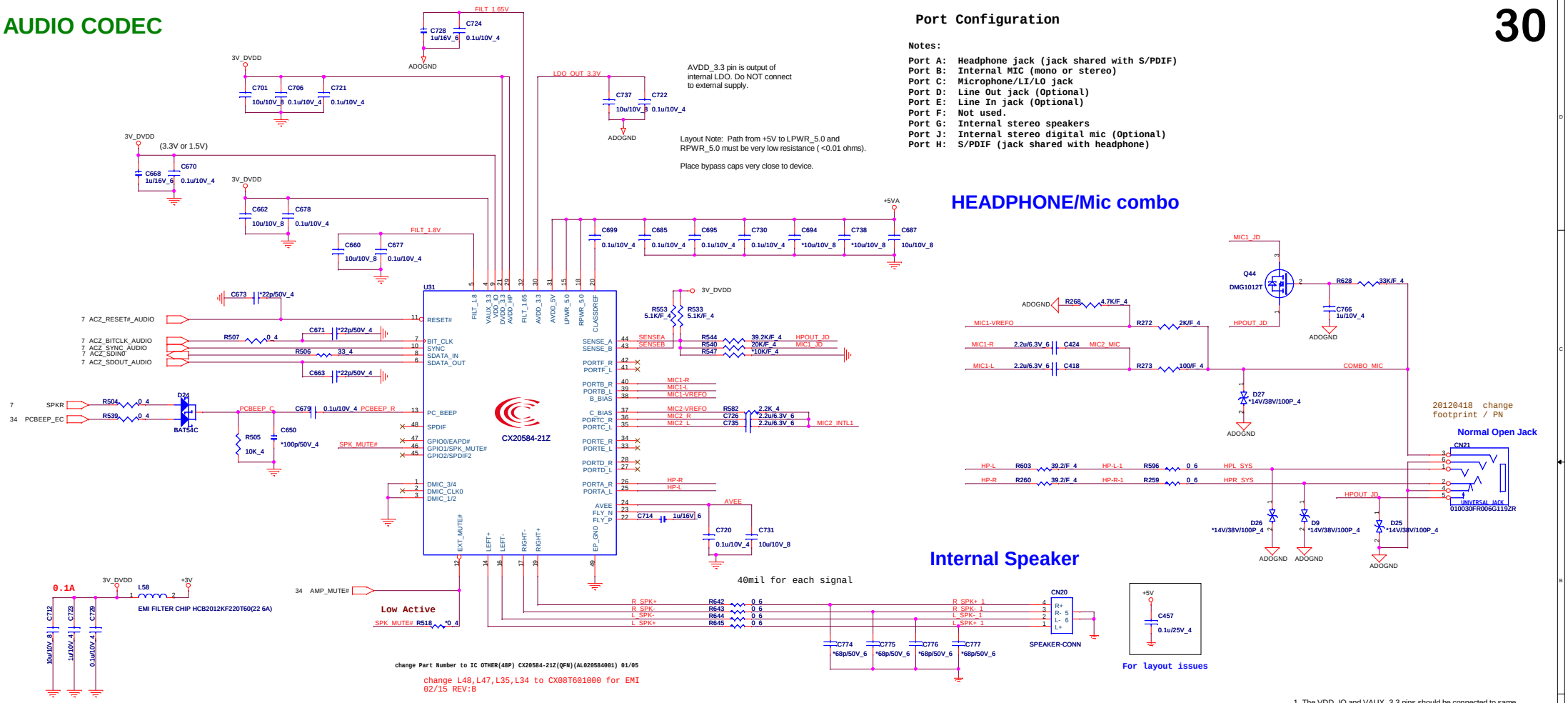
AUDIO CODEC

Port Configuration

Notes:

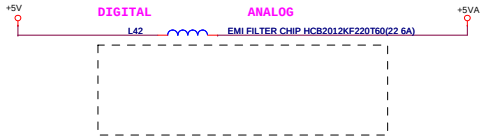
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

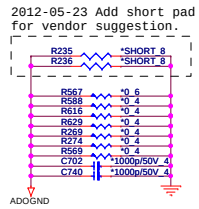


HEADPHONE/Mic combo

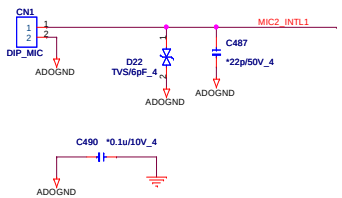
Internal Speaker

Power (ADO)





INT DIP AMIC array



1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.

2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.

3. C309, C310, C311 are optional.
Do not install unless needed for EMI/SI.

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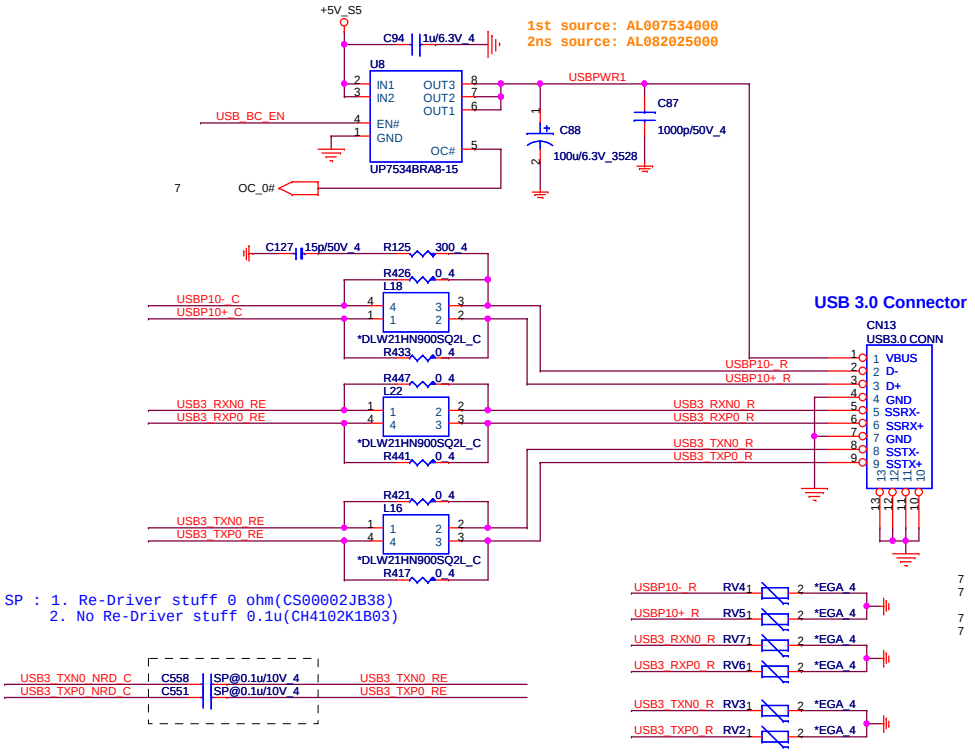
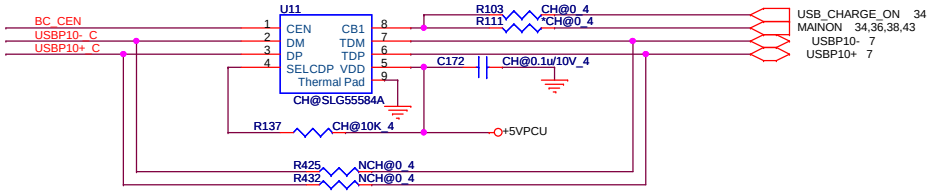
USB3.0/2.0

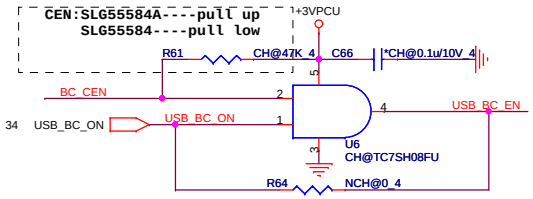


SP : 1. Re-Driver stuff 0 ohm(CS00002JB38)
2. No Re-Driver stuff 0.1u(CH4102K1B03)

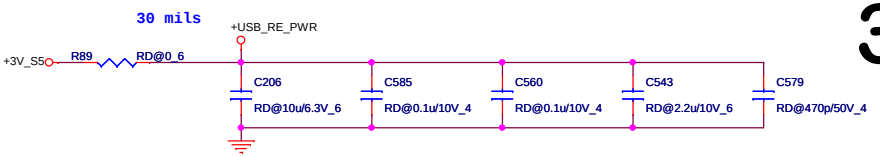
USB Charger to 3.0

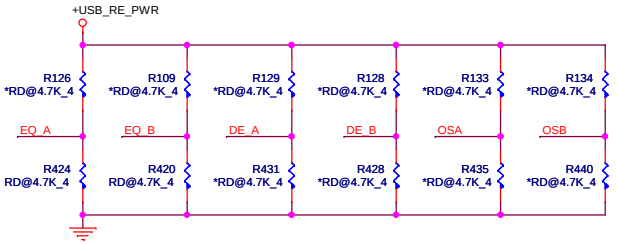
CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

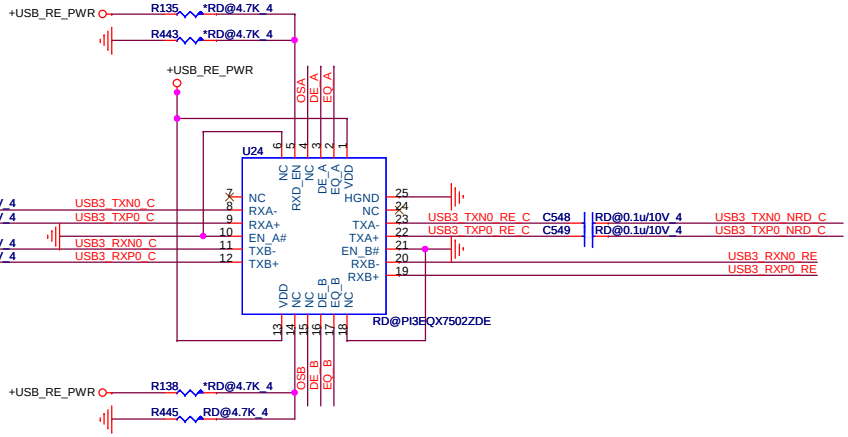


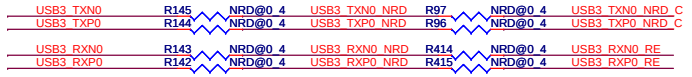


30 mils

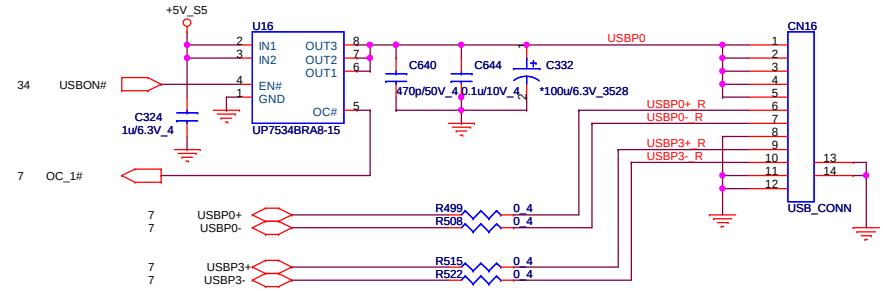








EXT. USB(USB)



Quanta Computer Inc.
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	INT&EXT USB	A1A

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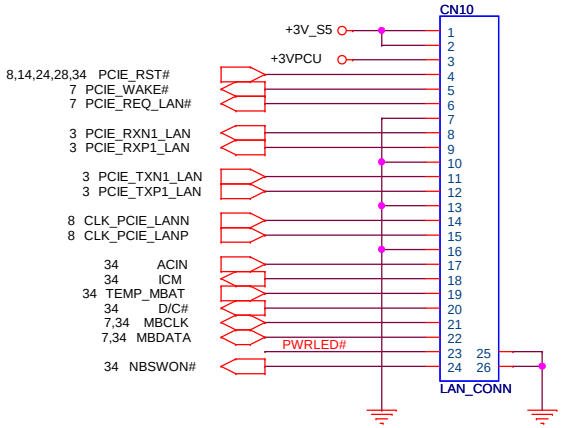
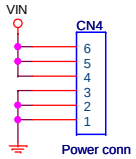
LAN& Charger DB

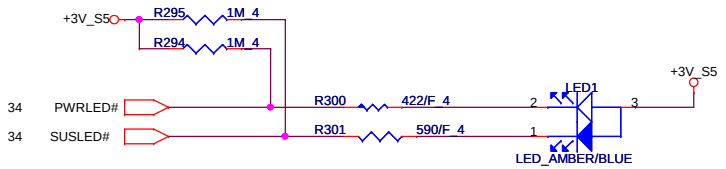


POWER M/B (DCD)

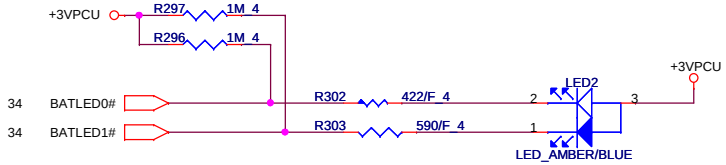


LED(UIF)

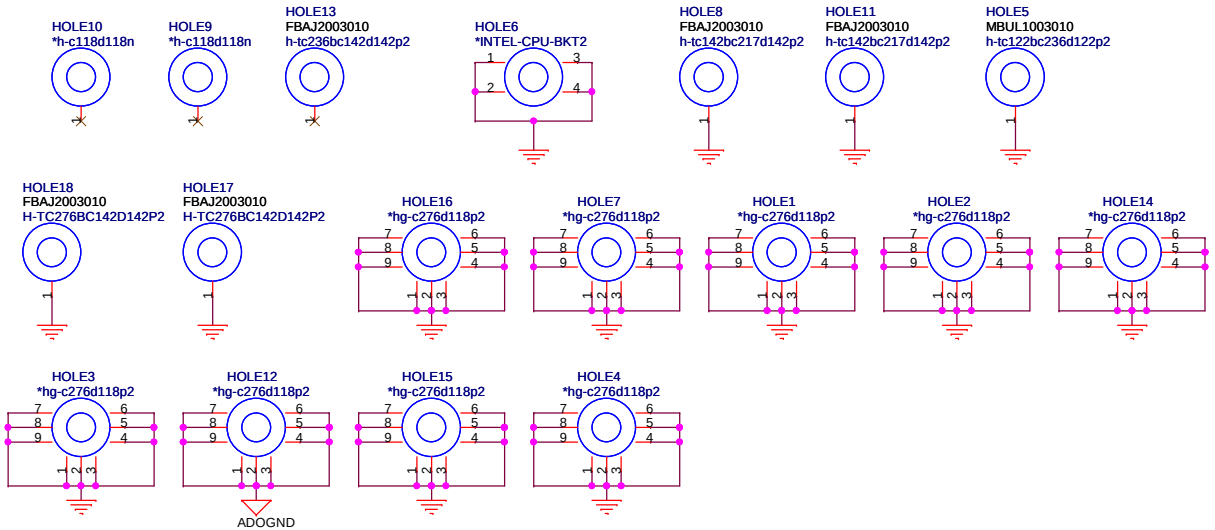
Power



Battery



HOLE(OTH)



EE RETURN-PATH CAPACITORS(EMC)

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	LAN DB/ LED/ EMI/ Hole	A1A

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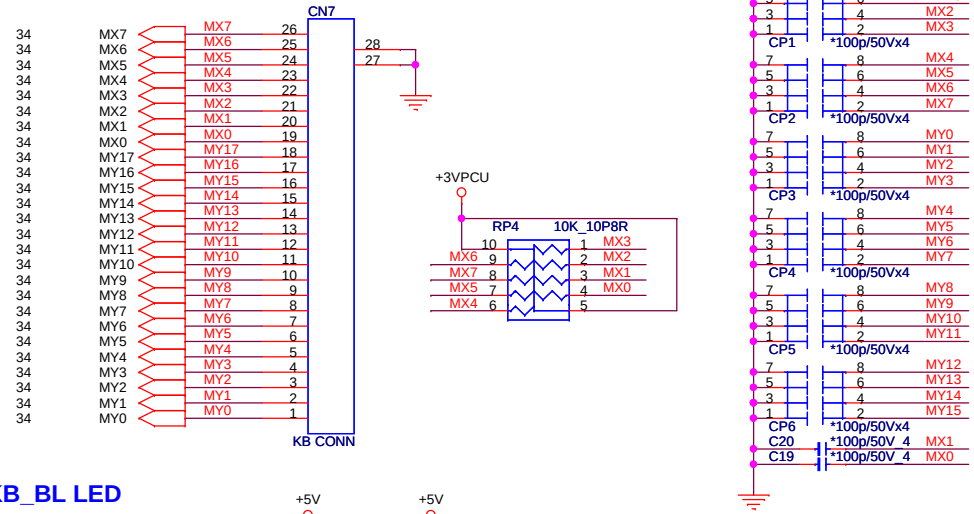
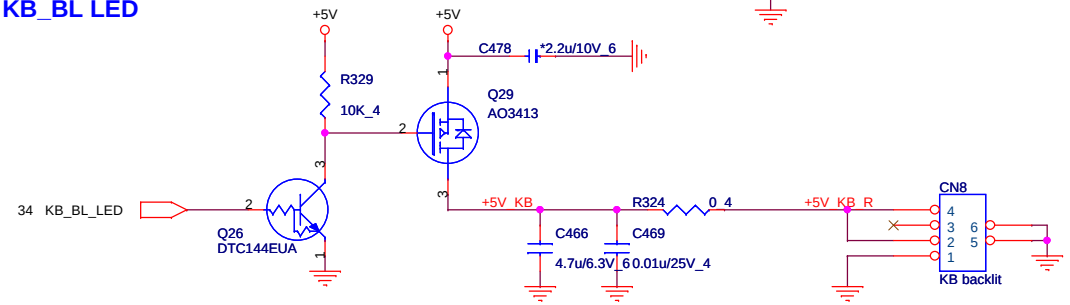
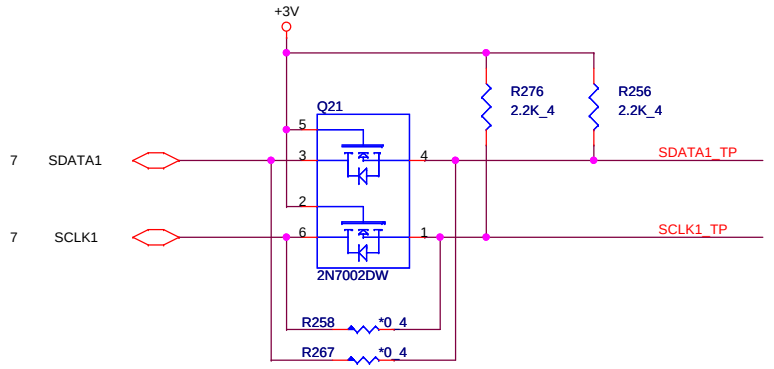
K/B(KBC)

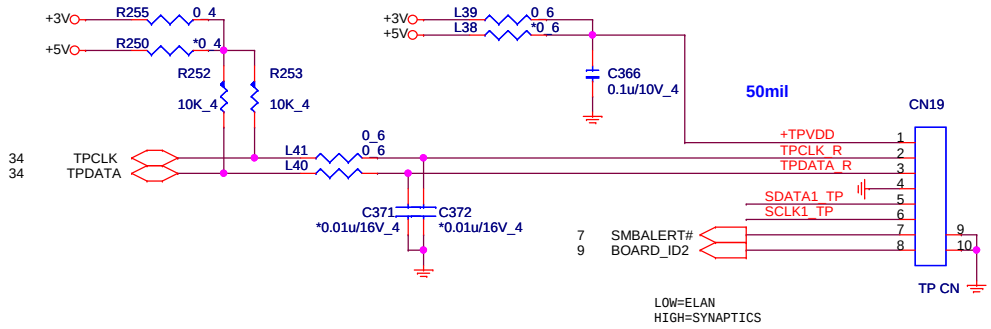


KB_BL LED



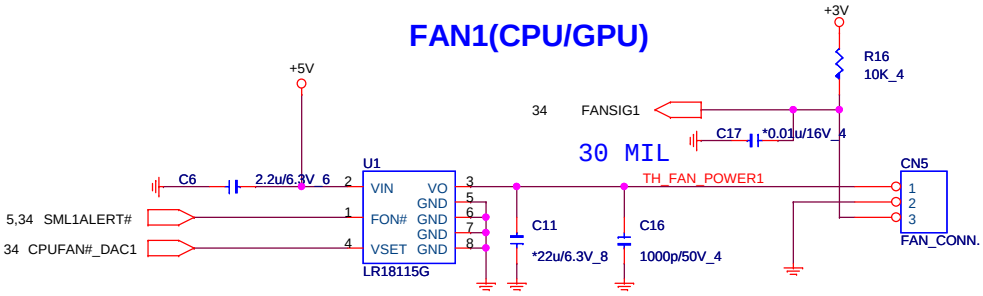
TOUCHPAD BOARD CONN(TPD)



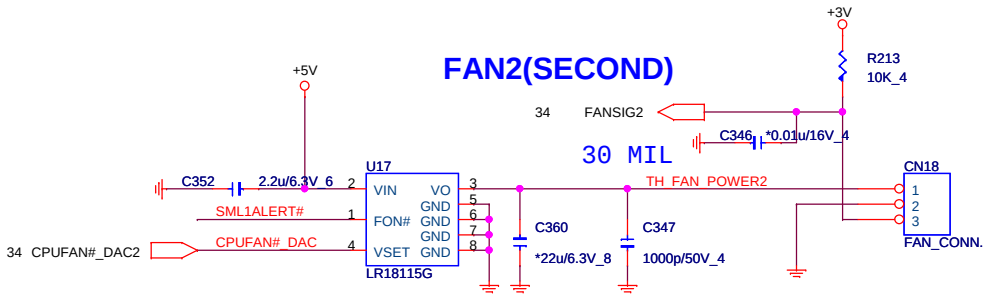


CPU FAN(THM)

FAN1(CPU/GPU)



FAN2(SECOND)



Quanta Computer Inc.

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	KB/TP/FAN	A1A
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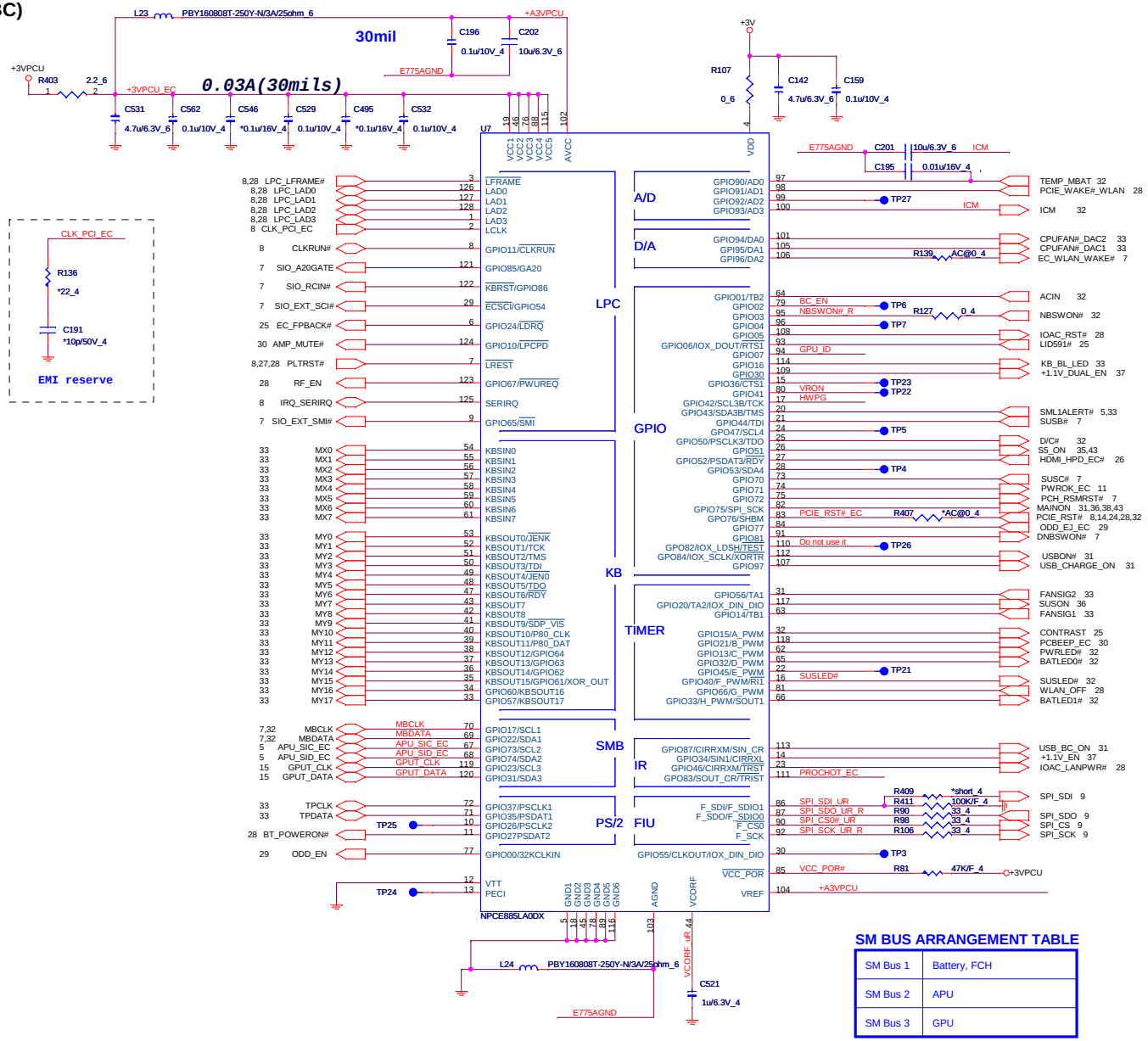
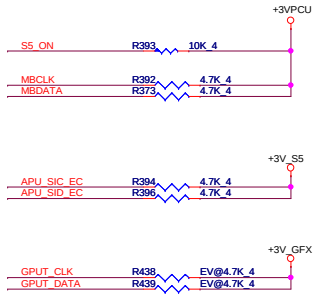
EC(KBC)

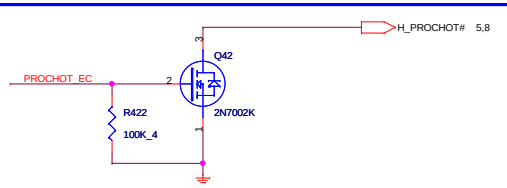


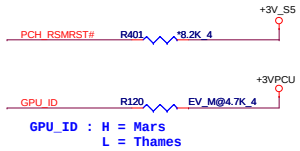
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery, FCH
SM Bus 2	APU
SM Bus 3	GPU

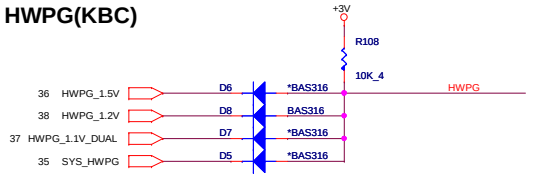
SM BUS PU(KBC)



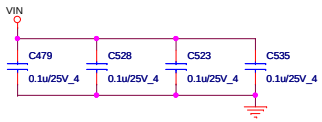




HWPG(KBC)

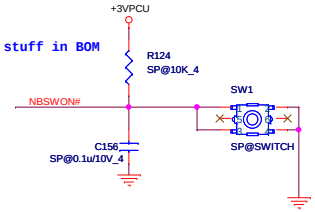


Placement for EC of VIN power plan



POWER-ON SWITCH (KBC)

SP: Debug use and MP no stuff in BOM



Quanta Computer Inc.
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Size	Document Number	Rev
	NPCE885/FLASH	A1A

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MAIND → MAIND 36,43

SYS_SHDN# → SYS_SHDN# 5,15,43

Ven=7.23V

+5VPCU
5 Volt +/- 5%
TDC : 6.25A
PEAK : 8.3A
OCP : 10A
Width : 250mil

+3VPCU
3.3 Volt +/- 5%
TDC : 4.2A
PEAK : 5.6A
OCP : 6.8A
Width : 180mil

OCP:10A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=10-(2.525/2)=8.74A
Vth=8.74A*14mOhm=122.32mV
R(Ilim)=(122.3mV*10)/10uA
~122.3K

OCP:8A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6.8-(1.9/2)=5.85A
Vth=5.85A*14mOhm=81.9mV
R(Ilim)=(81.9mV*10)/10uA
~81.9K

TDC : 2.25A
PEAK : 3A
Width : 100mil

TDC : 4A
PEAK : 5.4A
Width : 160mil

TDC : 2A
PEAK : 2.7A
Width : 80mil

TDC : 0.64A
PEAK : 0.85A
Width : 40mil

Quanta Computer Inc.	
PROJECT : ZRP	
Size	Document Number: SYSTEM 5V/3V (RT8223P) — Rev: A1A
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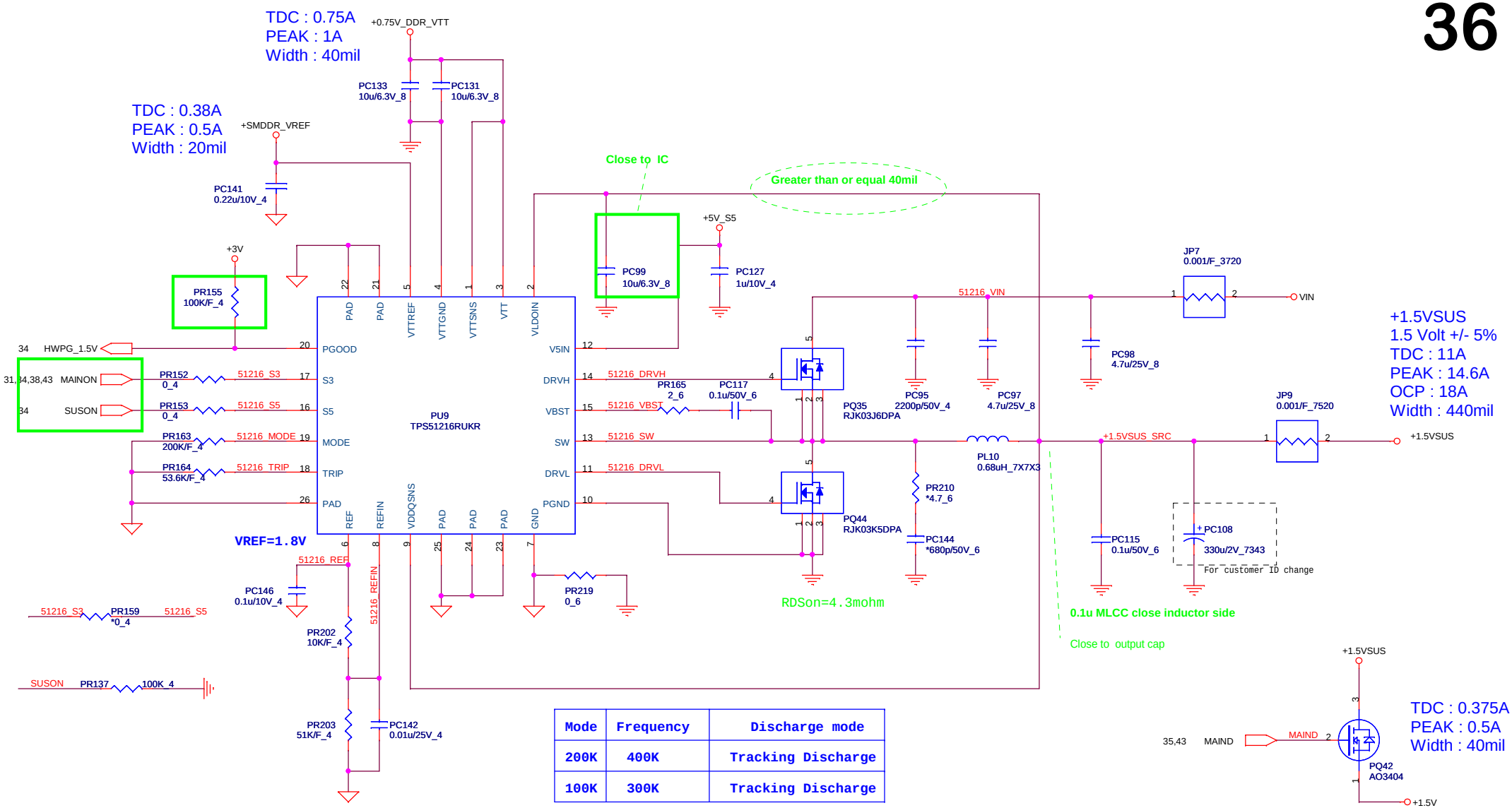
TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

OCP=18A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=18-(5.079/2)*4.3mohm
=0.06647V
Rlimit=0.06647/10uA*8~53.183Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	A1A

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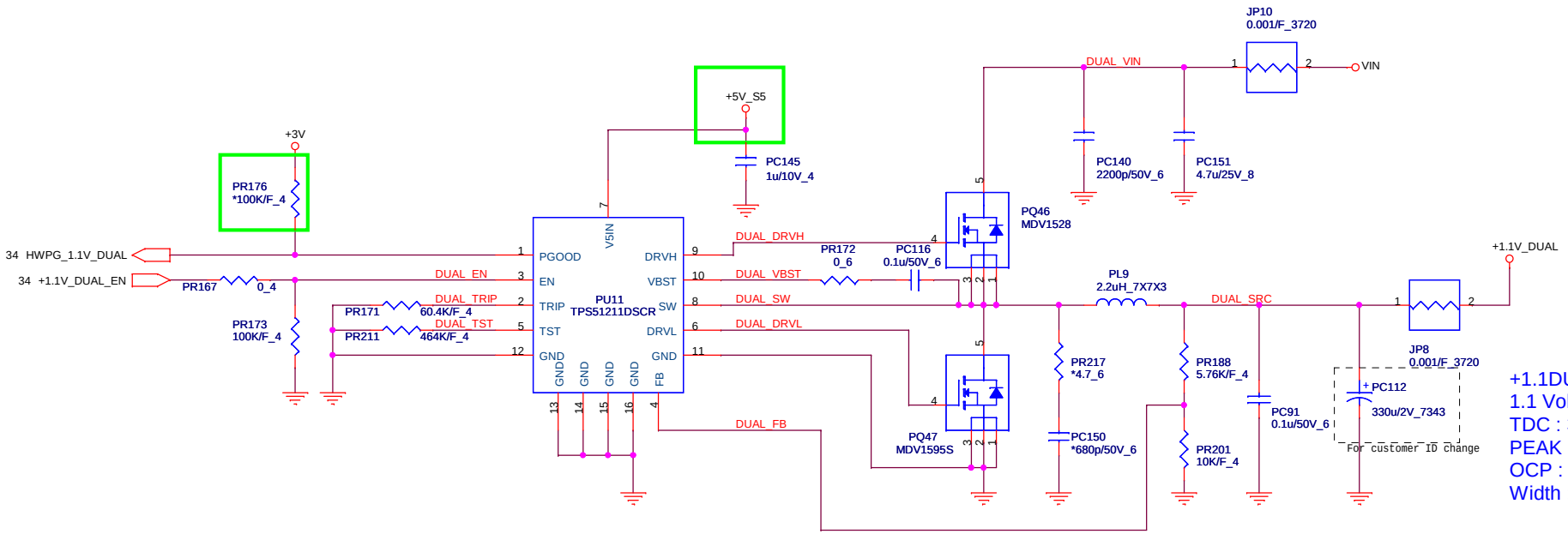
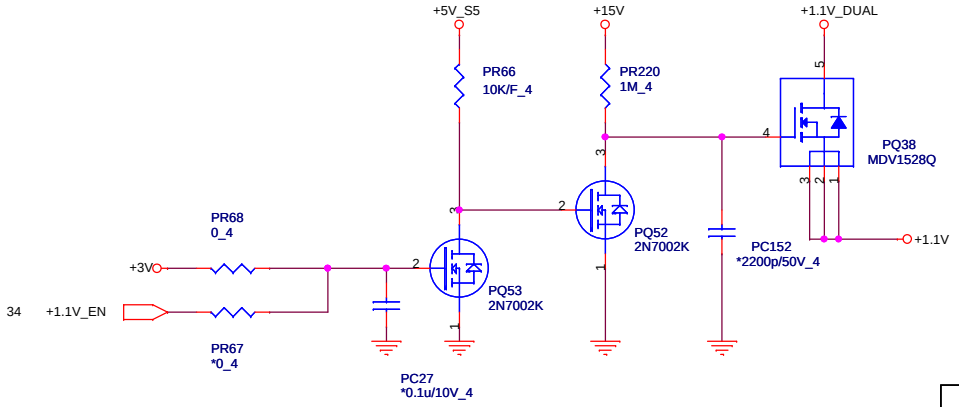


+1.1DUAL
1.1 Volt +/- 5%
TDC : 3.86A
PEAK : 5.2A
OCP : 6.2A
Width : 160mil

OCP=5A
L ripple current
=(19-1.1)*1.1/(2.2u*290k*19)
=1.624A
Vtrip=6.2-(1.624/2)*14mohm
=0.07542V
Rlimit=0.07542/10uA*8~60.34Kohm



+1.1V
TDC : 3A
PEAK : 4A
Width : 120mil

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	+1.1V_DUAL(TPS51211)	A1A
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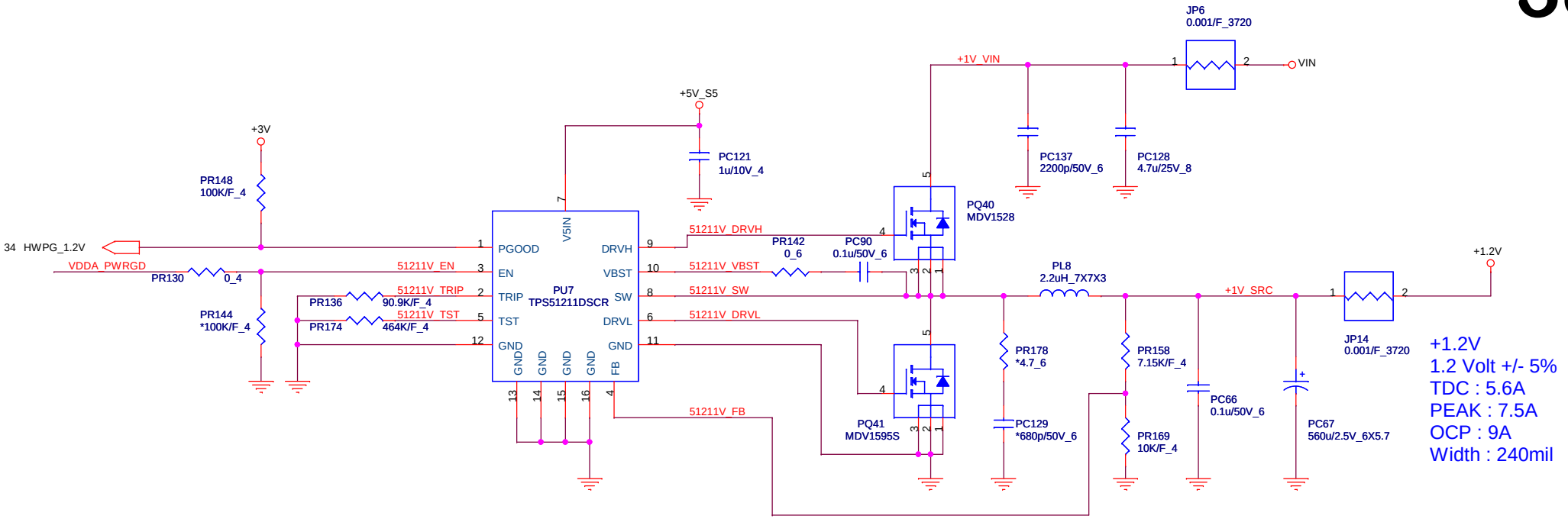
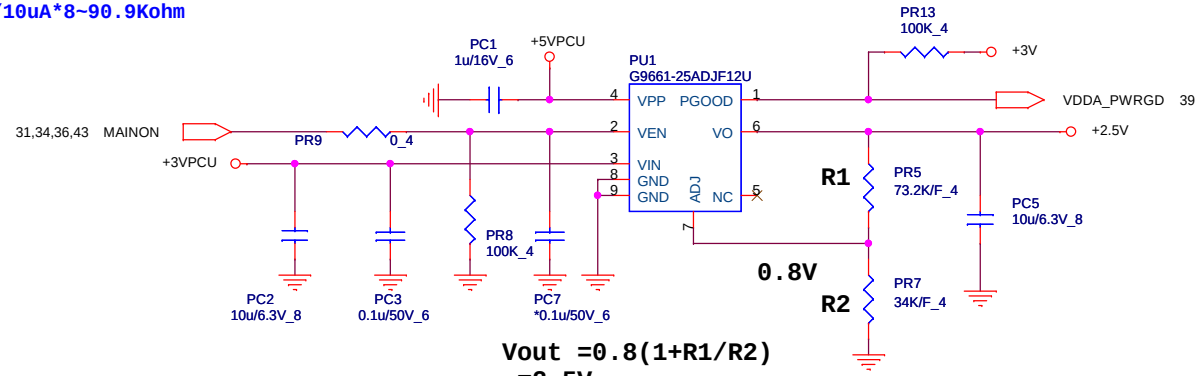


+1.2V
1.2 Volt +/- 5%
TDC : 5.6A
PEAK : 7.5A
OCP : 9A
Width : 240mil

OCP=9A
L ripple current
=(19-1.2)*1.05/(2.2u*290k*19)
=1.762A
Vtrip=9-(1.762/2)*14mohm
=0.1136V
Rlimit=0.1136/10uA*8~90.9Kohm



Vout =0.8(1+R1/R2)
=2.5V

+2.5V
2.5 Volt +/- 5%
TDC : 0.6A
PEAK : 0.75A
Width : 40mil

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	+1.2V(TPS51211)/+2.5V	A1A
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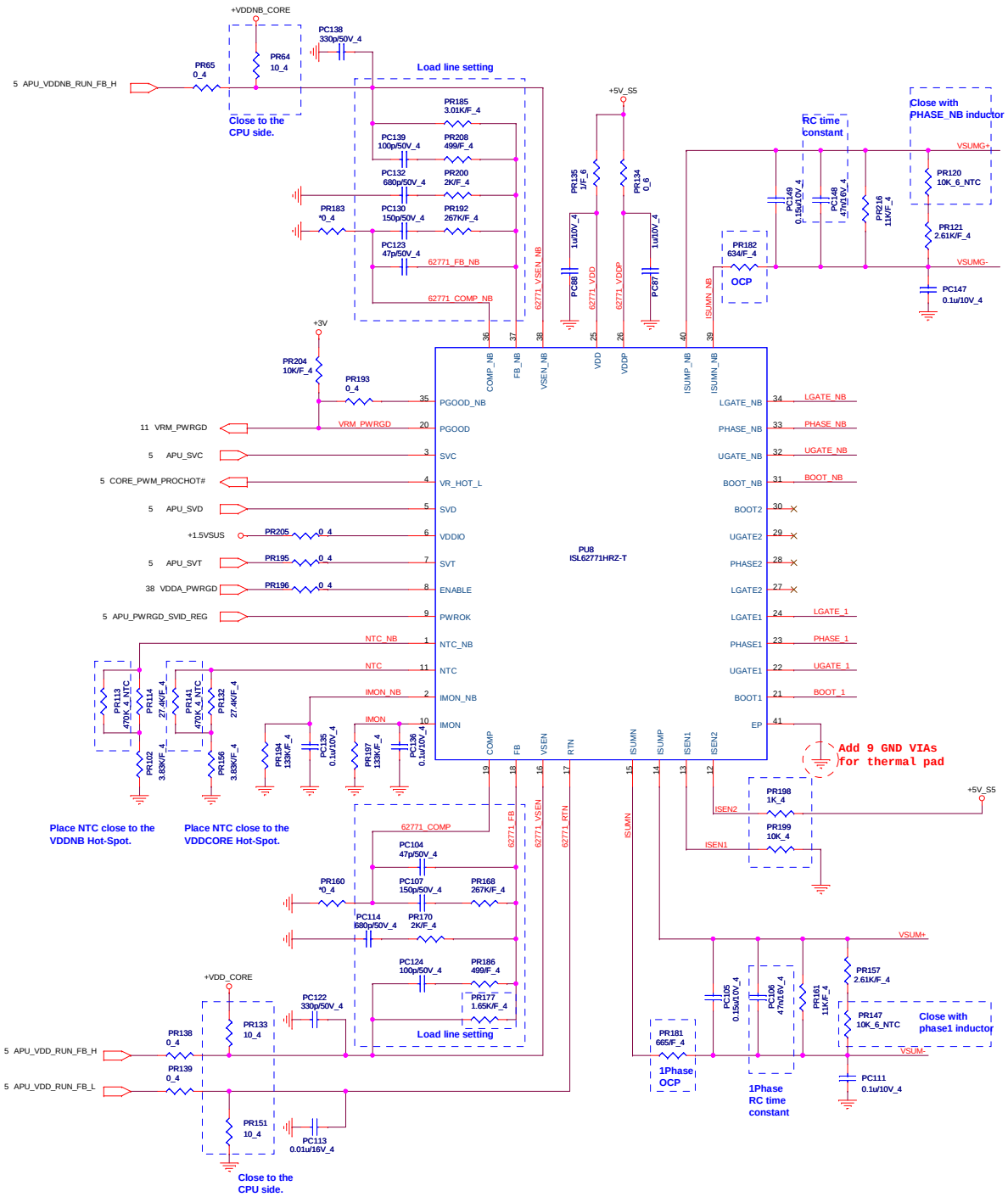
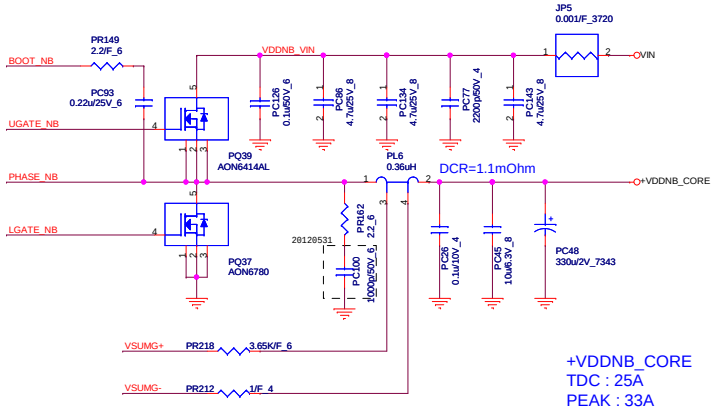
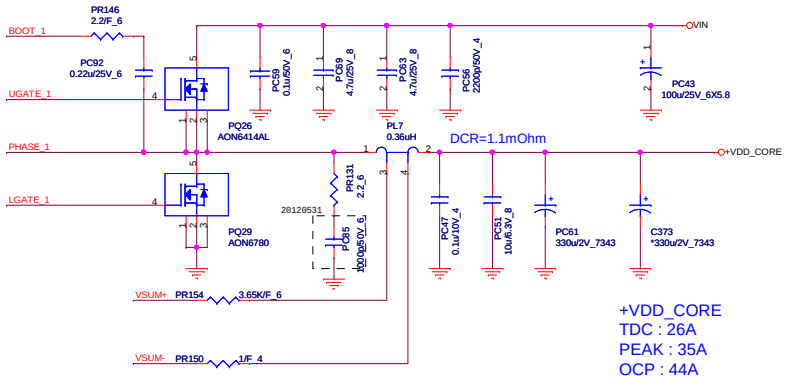




+VDDNB_CORE
TDC : 25A
PEAK : 33A
OCP : 42A
Width : 1320mil
Load Line = 4mV/A



+VDD_CORE
TDC : 26A
PEAK : 35A
OCP : 44A
Width : 1400mil
Load Line = 2.1mV/A

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PROJECT : ZRP		
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Default 0.85V POP PR163 ; DNP PR171
Default 0.9V

SP : Thames Pro,XT stuff PR171
Mars no stuff PR171

Thames(Pro,XT) VDDC VID TABLE

VDDC(V)	PWRCNTRL0 (VID4) (GPIO_15)	PWRCNTRL1 (VID3) (GPIO_20)
0.900	1	0
1.000	0	1

Mars VDDC VID TABLE

VDDC(V)	PWRCNTRL0 (VID4) (GPIO_15)	PWRCNTRL1 (VID3) (GPIO_20)	PWRCNTRL2 (VID2) (GPIO_16)	PWRCNTRL3 (VID1) (GPIO_29)	PWRCNTRL4 (VID0) (GPIO_30)
1.100	0	0	0	0	0
1.075	0	0	0	1	0
1.050	0	0	1	0	0
1.025	0	0	1	1	0
1.000	0	1	0	0	0
0.975	0	1	0	1	0
0.950	0	1	1	0	0
0.925	0	1	1	1	0
0.900	1	0	0	0	0
0.875	1	0	0	1	0
0.850	1	0	1	0	0
0.825	1	0	1	1	0
0.800	1	1	0	0	0

Check EN level

Parallel

Close to the GPU side.

Close to the VR side.

+VGPU_CORE
Countinue current:18A
Peak current:24A
OCP minimum 28A
Loadline=1.5mV/A

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	+VGPU CORE(TPS51728)	A1A

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+1.8V_GFX
1.8 Volt +/- 5%
TDC : 1.4A
PEAK : 1.9A
Width : 60mil

V0=0.8*(R1+R2)/R2

1V/+/-5%
TDC : 1.65A
PEAK : 2.2A
Width : 80mil

Vout = (1+Rg/Rh)*0.5
=1V (for Pro & XT)

Rh change to 110/F_4 (CS11102FB18)
is 0.95V for Mars

SP : Thames Pro,XT Rh=100ohm(CS11002FB22)
Mars Rh=110ohm(CS11102FB18)

TDC : 1.65A
PEAK : 2.2A
Width : 80mil

TDC : 0.05A
PEAK : 0.06A
Width : 20mil

Quanta Computer Inc.
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Size	Document Number	Rev
	GPU_POWER/+1.8V_GPU	A1A
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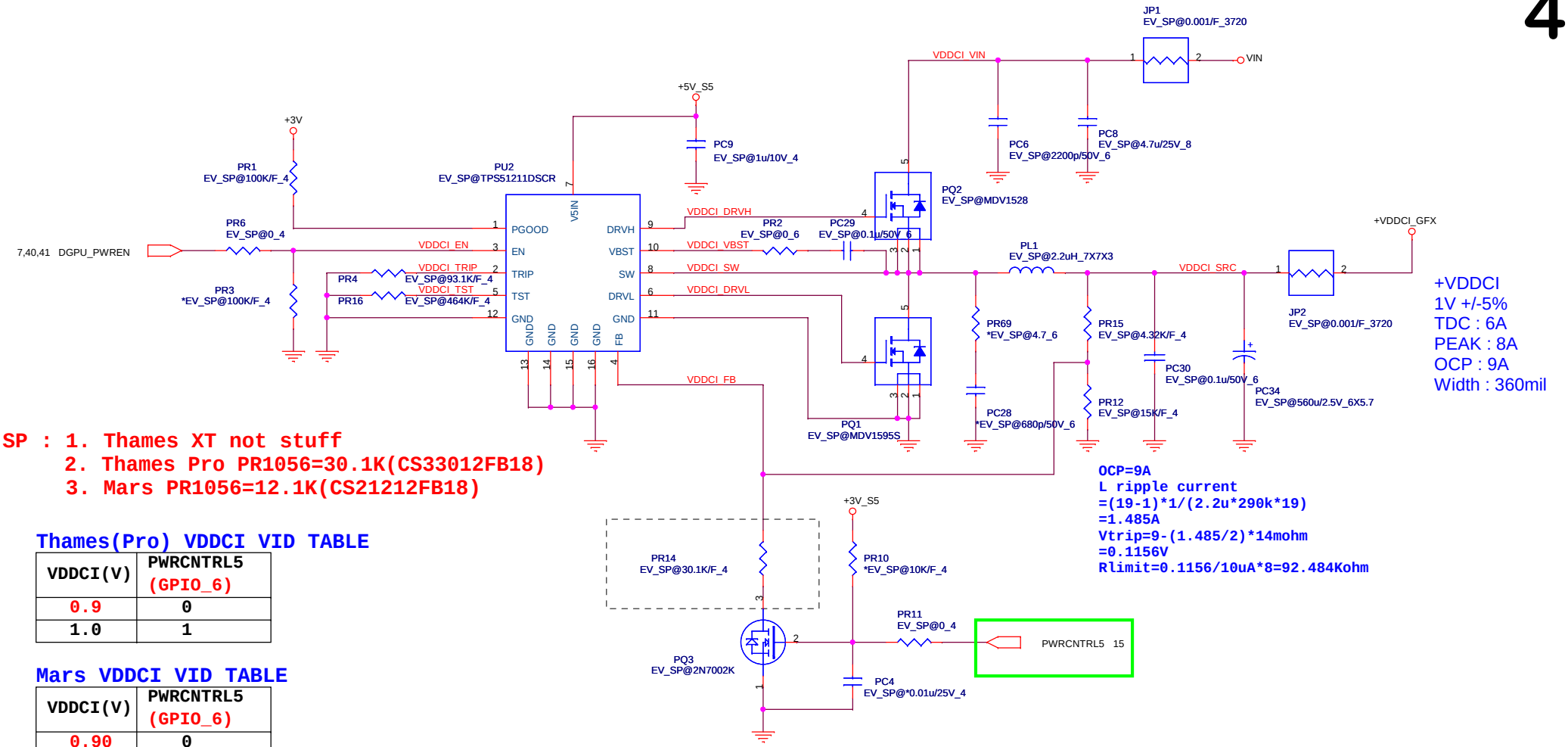

+VDDCI
1V +/-5%
TDC : 6A
PEAK : 8A
OCP : 9A
Width : 360mil

SP : 1. Thames XT not stuff
2. Thames Pro PR1056=30.1K(CS33012FB18)
3. Mars PR1056=12.1K(CS21212FB18)

OCP=9A
L ripple current
=(19-1)*1/(2.2u*290k*19)
=1.485A
Vtrip=9-(1.485/2)*14mohm
=0.1156V
Rlimit=0.1156/10uA*8=92.484Kohm

Thames(Pro) VDDCI VID TABLE

VDDCI(V)	PWRCNTRL5 (GPIO_6)
0.9	0
1.0	1

Mars VDDCI VID TABLE

VDDCI(V)	PWRCNTRL5 (GPIO_6)
0.90	0
0.95	1

PR1056 change to 12.1K/F_4
(CS21212FB18) for Mars 0.95V

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Size	Document Number	Rev
	VDDCI(TPS51518)	A1A
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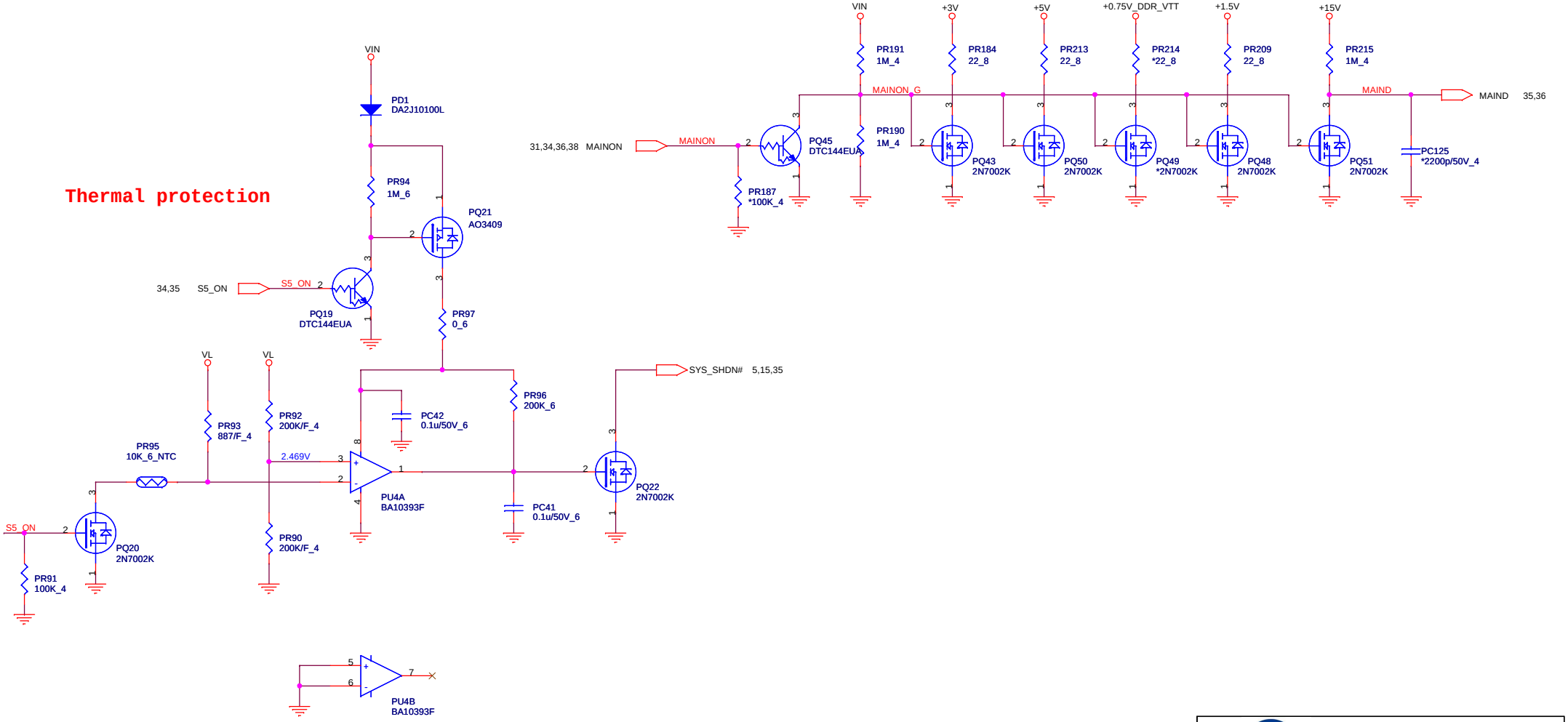
Thermal protection



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZRP		
Size	Document Number: Discharge/Thermal	Rev: A1A
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MODEL	REV	CHANGE LIST
ZRP M/B	A	First Release

Model / Page	ZRP MB BOARD	
	From	To
1		
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ZRP	PCBA NO :	REV: A	DOC. NO :
APPROVED BY :	CHECK BY :	DRAWING BY :	DATE :

Quanta Computer Inc.

PROJECT : ZRP

Size	Document Number	Rev
	CHANGE LIST	A1A
Date: Tuesday, May 29, 2012	Sheet 44 of 44	