

# Compal Confidential

## VAWGA/B Schematics Document

### AMD "Kabini" Platform

### AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun

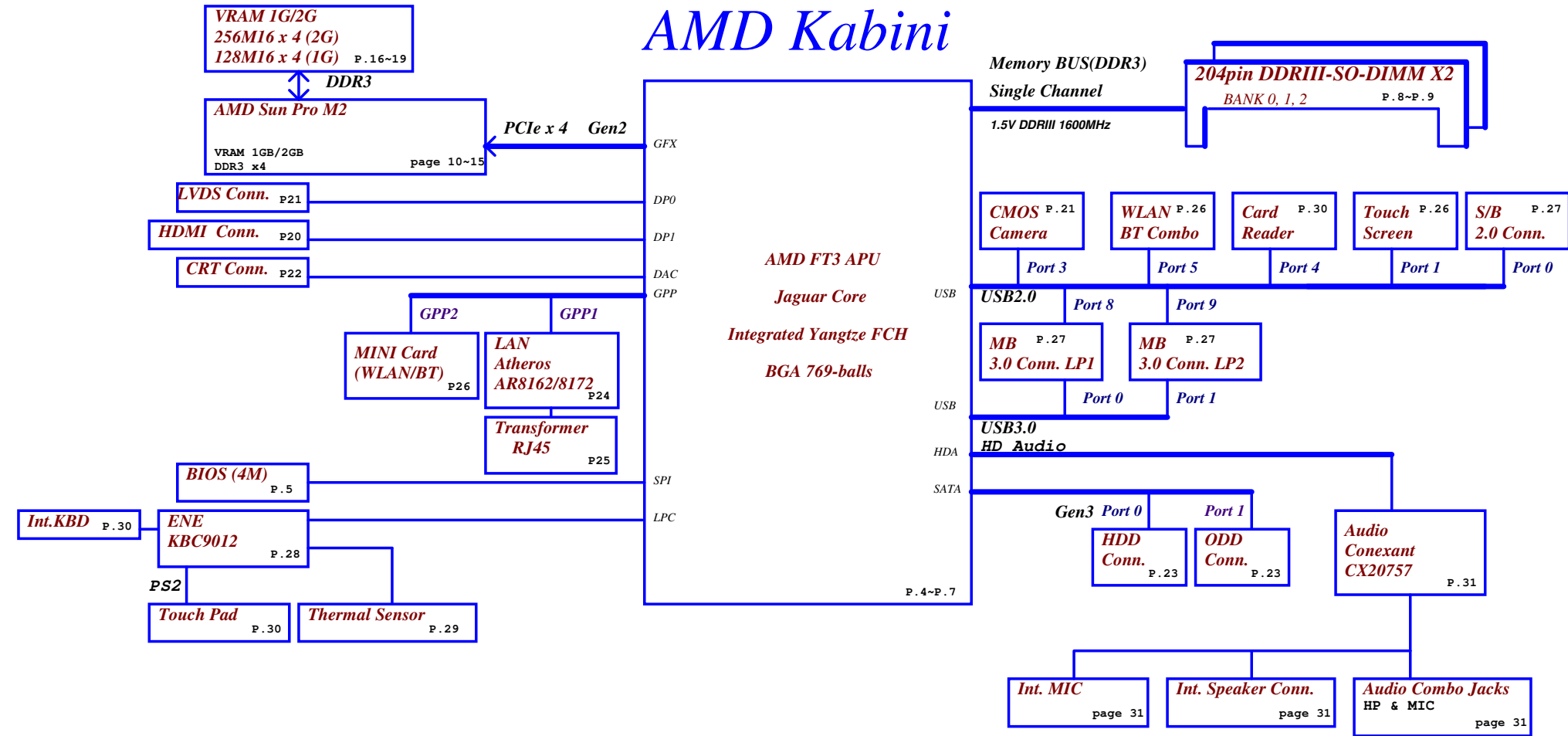
LA-9911P REV: 1.0

2013-04-01

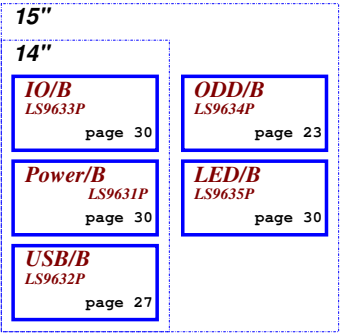
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Model Name : VAWGA/B



Sub-board



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.5VGS	1.5V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
		0	RIGHT USB
		1	Touch Screen
		2	
		3	Camera
		4	CardReader
		5	WLAN/BT Combo
		6	LEFT USB (for colay)
		7	LEFT USB (for colay)
	XHCI	0	LEFT USB3.0
		1	LEFT USB3.0

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

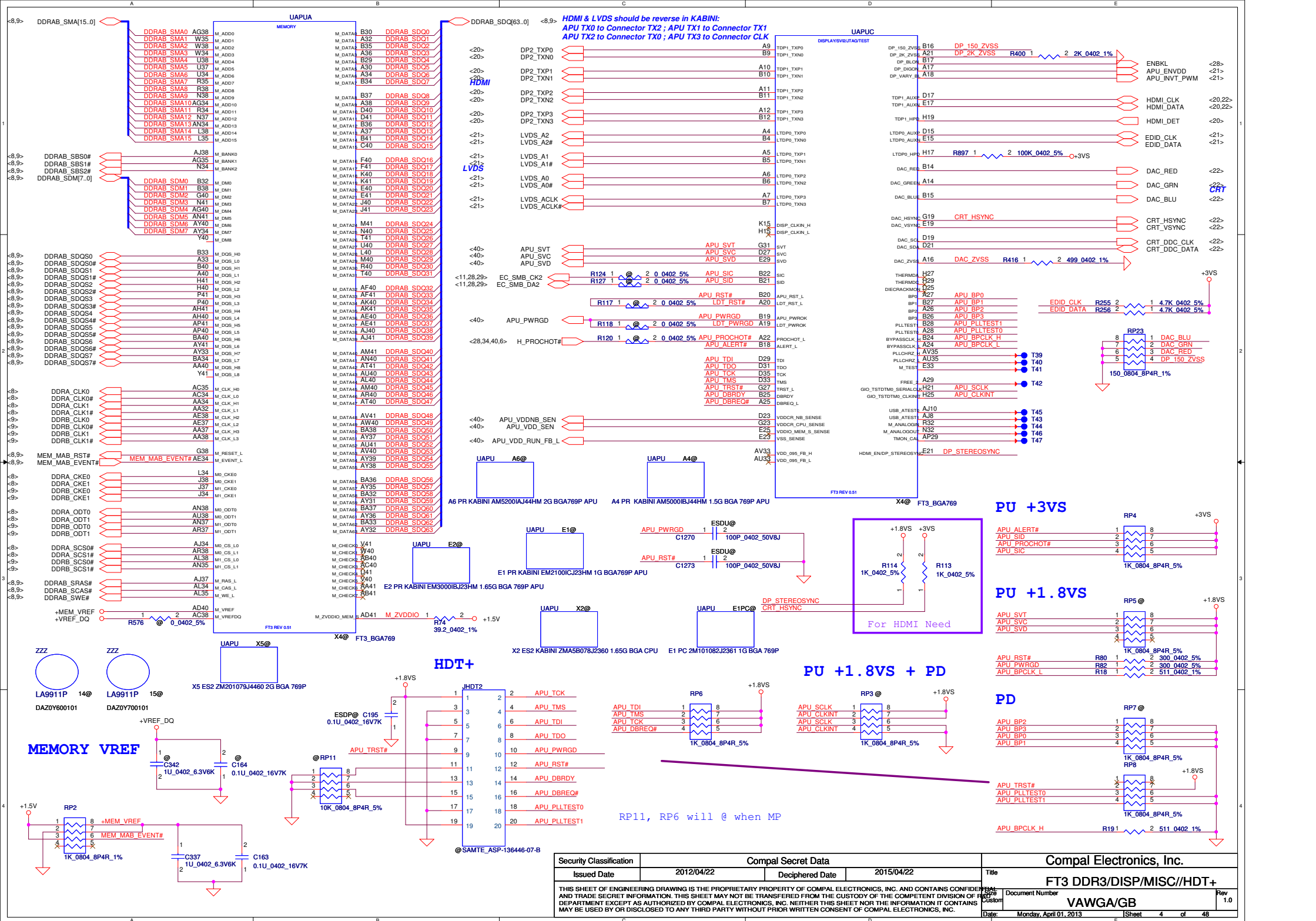
USB OC MAPPING

OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

BOM Structure Table

BOM Structure	BTO Item
A6@	A6 R3 BGA APU
A4@	A4 R3 BGA APU
E2@	E2 R3 BGA APU
E1@	E1 R3 BGA APU
E1PC@	E1 PC BGA APU
X4@	X4 ES2 BGA APU
X5@	X5 ES2 BGA APU
X2@	X2 ES2 BGA APU
EMICU@	CardReader EMI Un pop
EMICP@	CardReadear EMI pop
EMIUSB2RU@	Right USB2.0 port EMI un pop
EMIUSB2RP@	Right USB2.0 port EMI pop
USB2R@	Right USB2.0 port component
SUN@	SUN PRO GPU (R3 compal part)
MARS@	MARS XT GPU (R1 compal part)
14@	for 14" componect
15@	for 15" componect
PX@	Common VGA circuit
CMOS@	CMOS Camera part
HDMI@	HDMI part
EMIGASP@	Gastube
8162@	Ateros AR8162 LAN Chip
8172@	Ateros AR8172 LAN Chip
SWR@	LAN Switching mode
LDO@	LAN LDO mode
THERMAL@	Lenovo Thermal Sensor
ME@	ME part
UMA@	UMA part
@	Unpop
ZODD@	Zero Power ODD part
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component

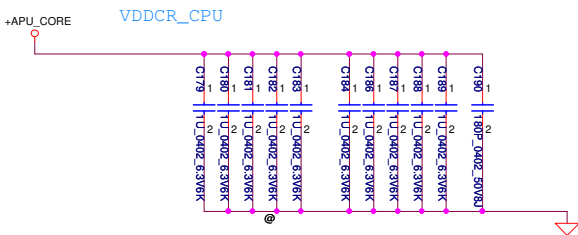
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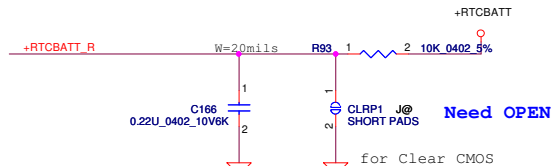


## CORE POWER OF APU

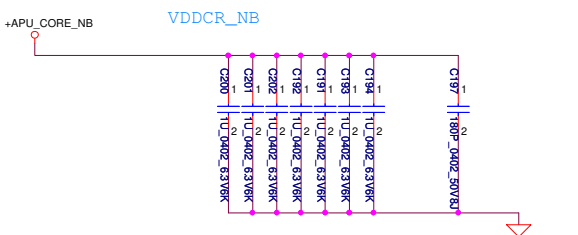


## RTC OF APU

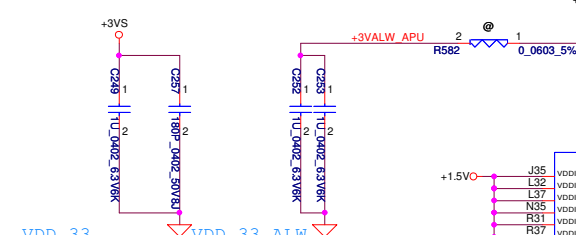
VDDBT\_RTC\_G



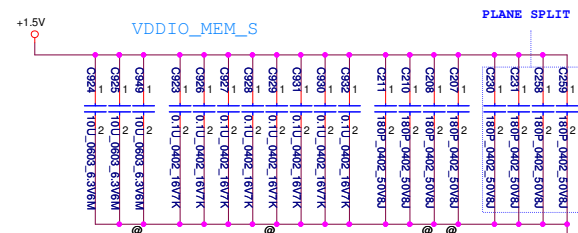
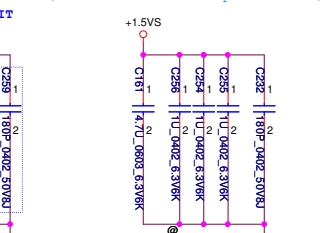
## INTEGRATED GPU POWER OF APU



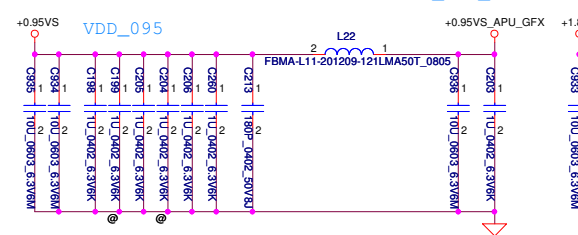
## +3VALW/+3VS OF APU



## +1.5V/+1.5VS OF APU

VDDIO\_AZ\_ALW  
(Could be S0 or S5 power rail)

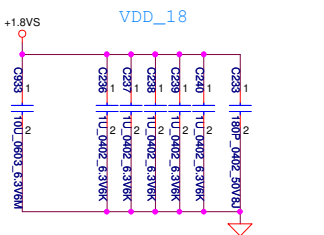
## +0.95VALW/+0.95VS OF APU



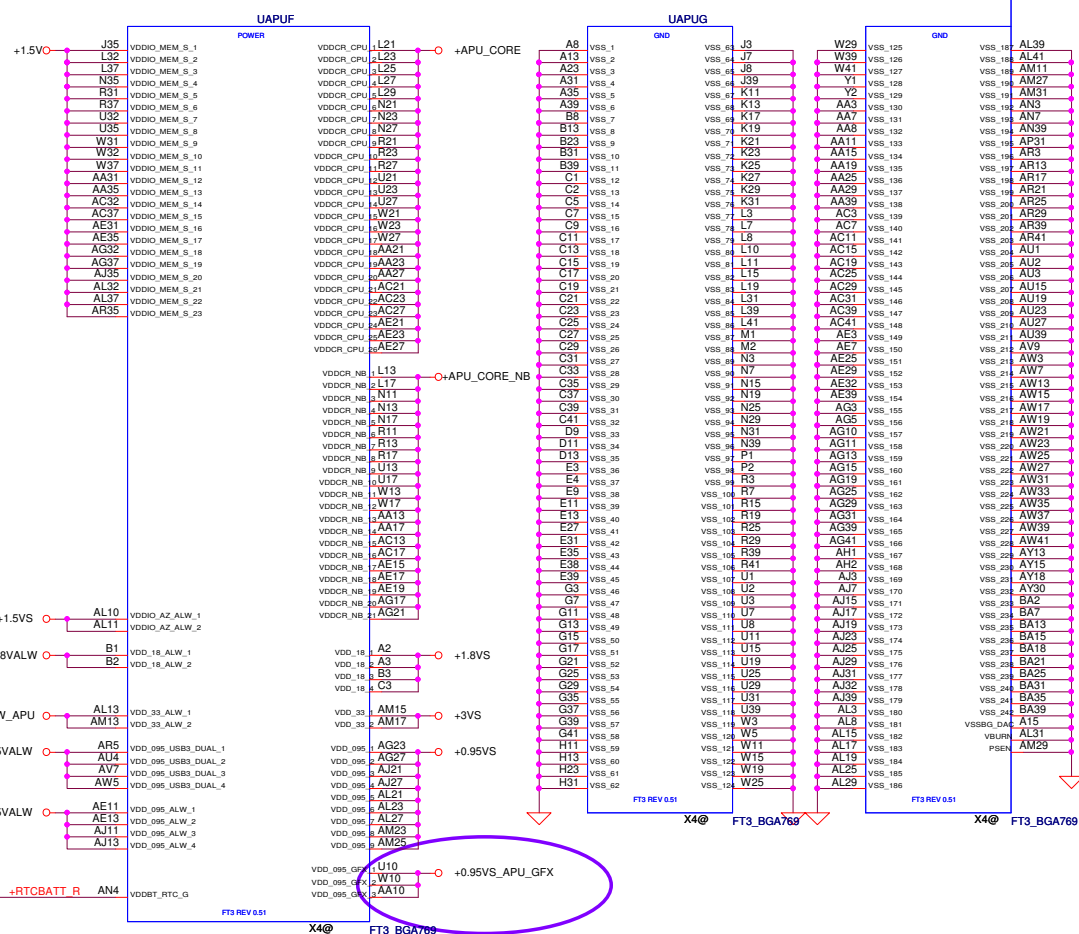
VDD\_095\_USB3\_DUAL

VDD\_095\_ALW

## +1.8VALW/+1.8VS OF APU

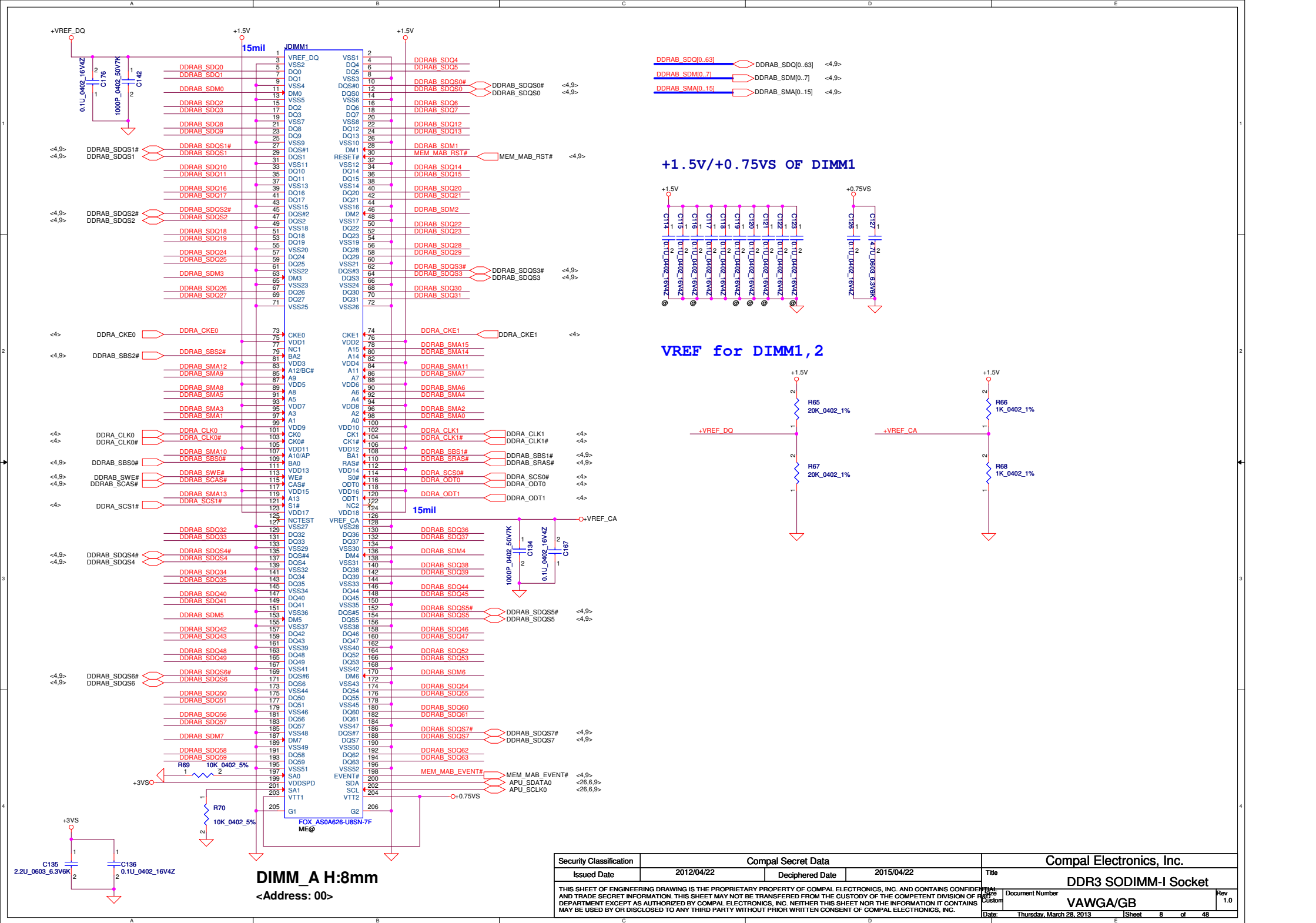


VDD\_18\_ALW

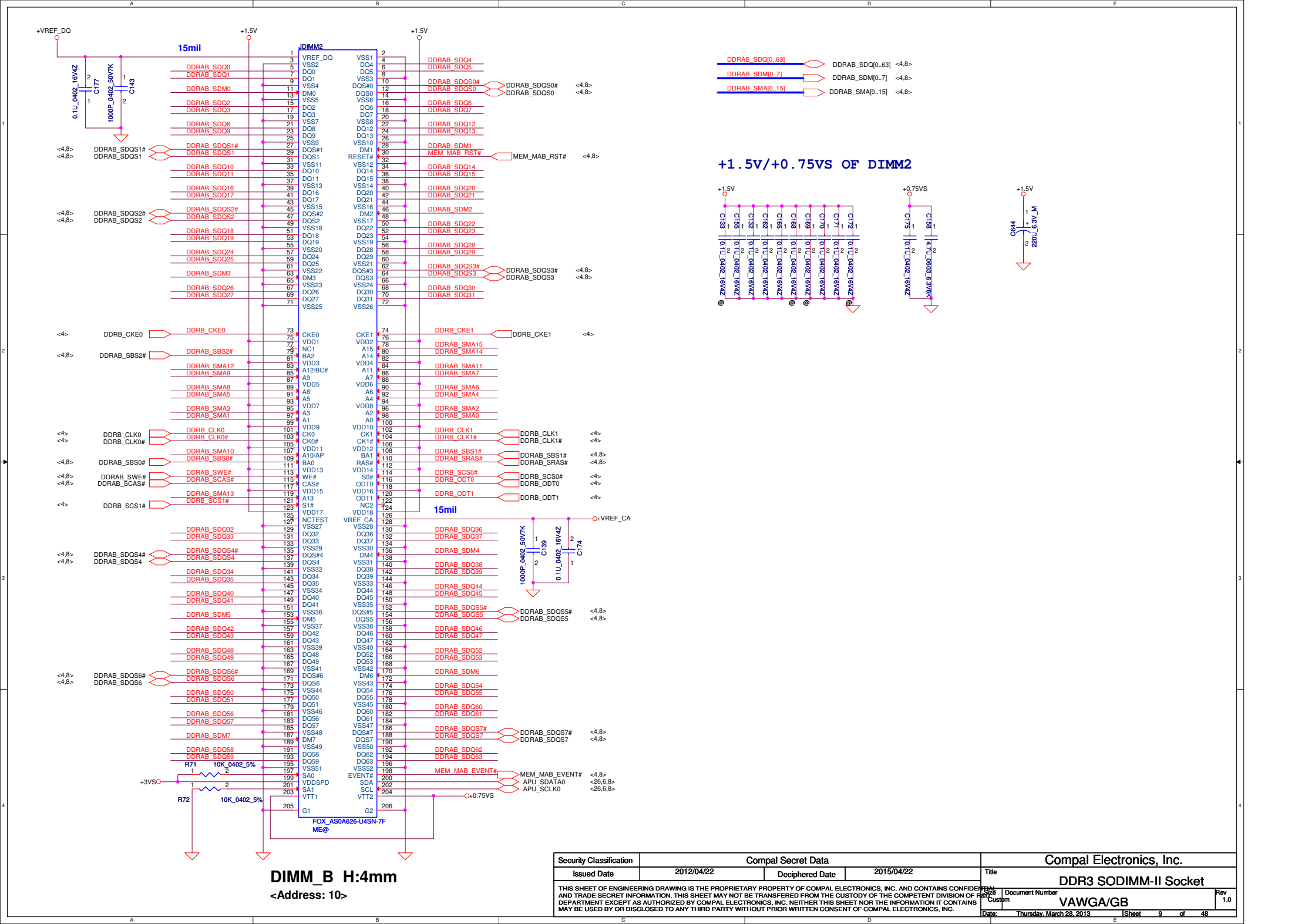


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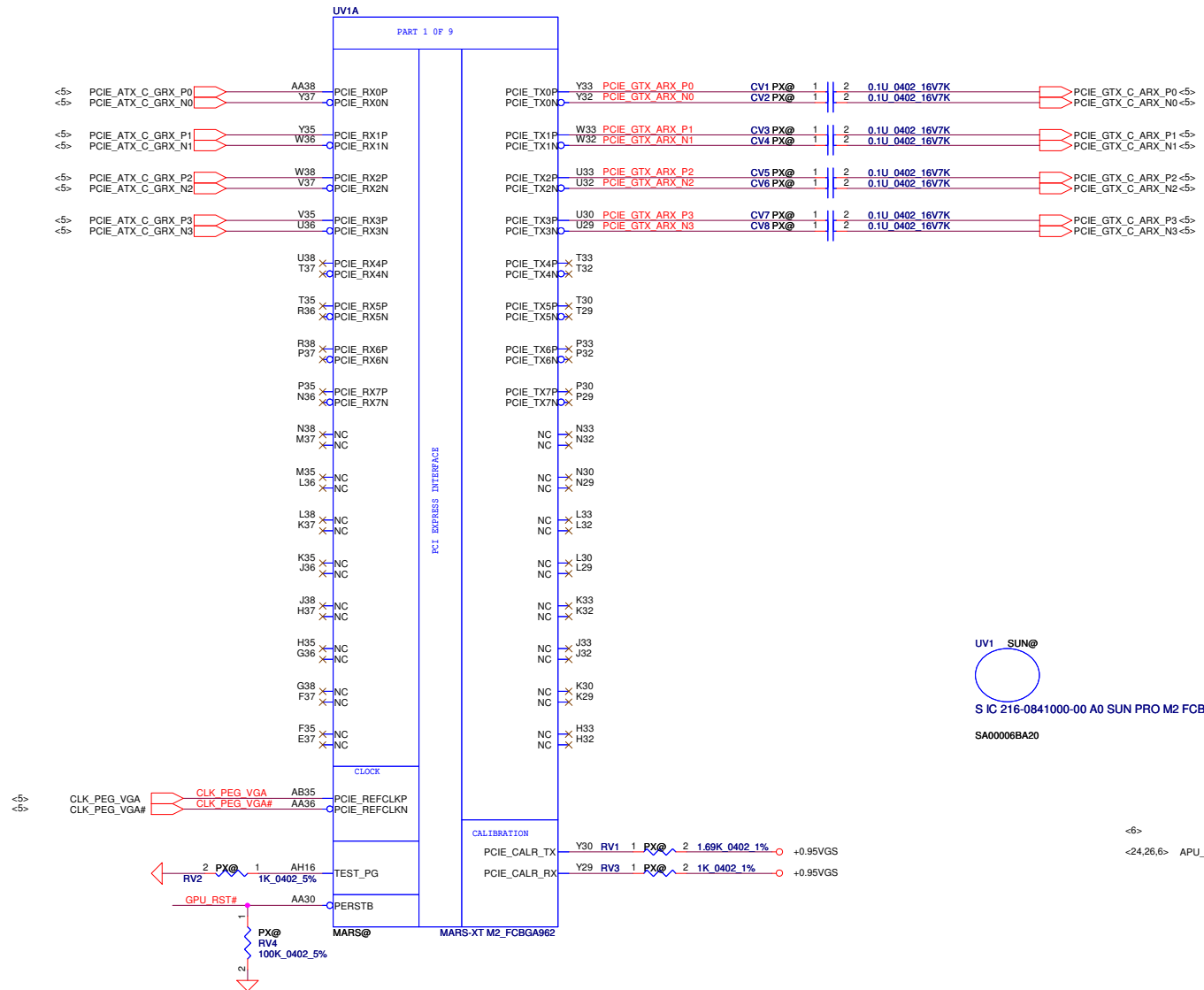




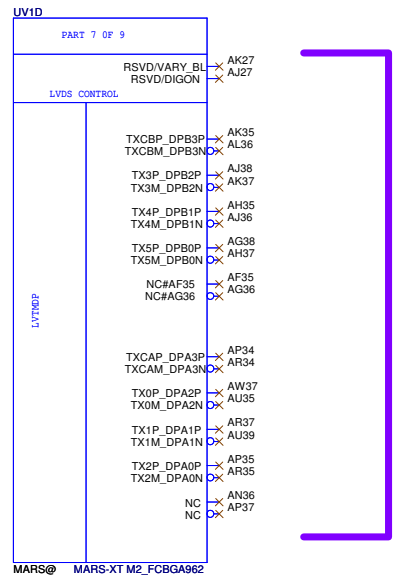




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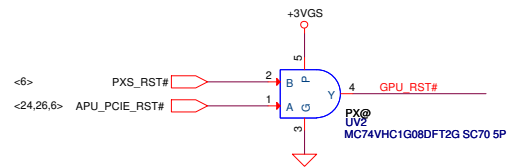


## LVDS Interface



SUN NC

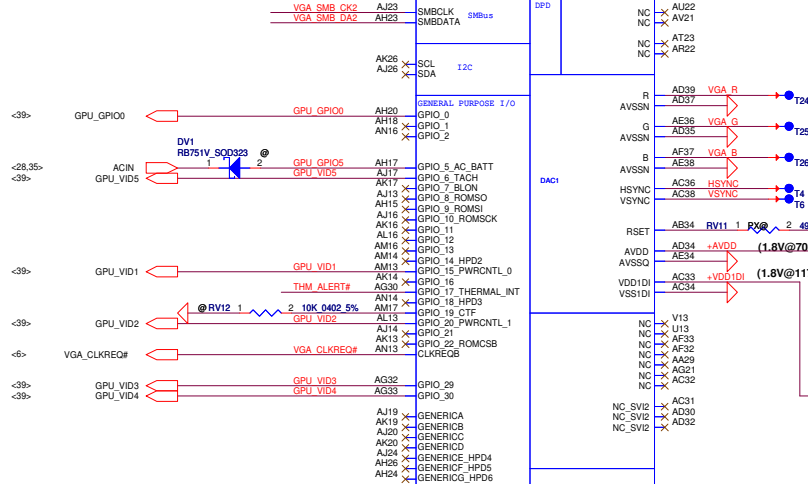
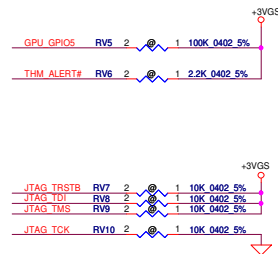
UV1 SUN@  
S IC 216-0841000-00 A0 SUN PRO M2 FCBGA 962P C38  
SA00006BA20



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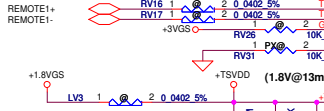
## STRAPS



0.60 V level, Please  
VREFG Divider and  
cap close to ASIC



GPIO 28 FDO	MLPS
H	Disable
L	Enable



TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE  
GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

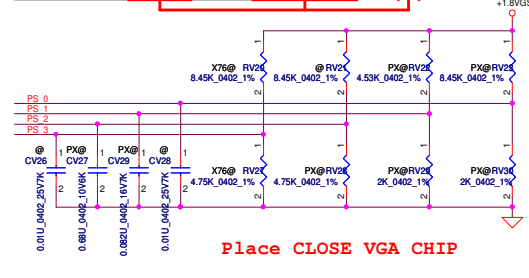
RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRs_ENB	PS_1[4]	Transmitter Power Savings Enable 0:20% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	0
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100-512Kbit M2SP05A (ST) 101-1Mbit M2SP10A (ST) 101-2Mbit M2SP20 (ST) 101-4Mbit M2SP40 (ST) 101-8Mbit M2SP80 (ST) 100-512Kbit Pm2SLV010 (Chingss) 101-1Mbit Pm2SLV010 (Chingss)	001 256MB
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1]	NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI	NC
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	NC
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	0
RESERVED	PS_1[2]	Reserved	1
RESERVED	NA	Reserved	NA
RESERVED	NA	Reserved (for Thames/Whisper/Seymour only)	NA
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

## MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	0 1	0 1 0	82 nF	4.53K	2K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 45

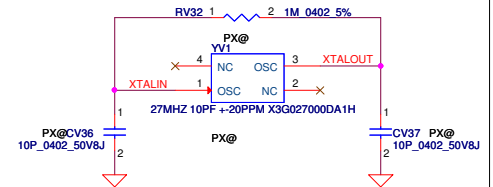
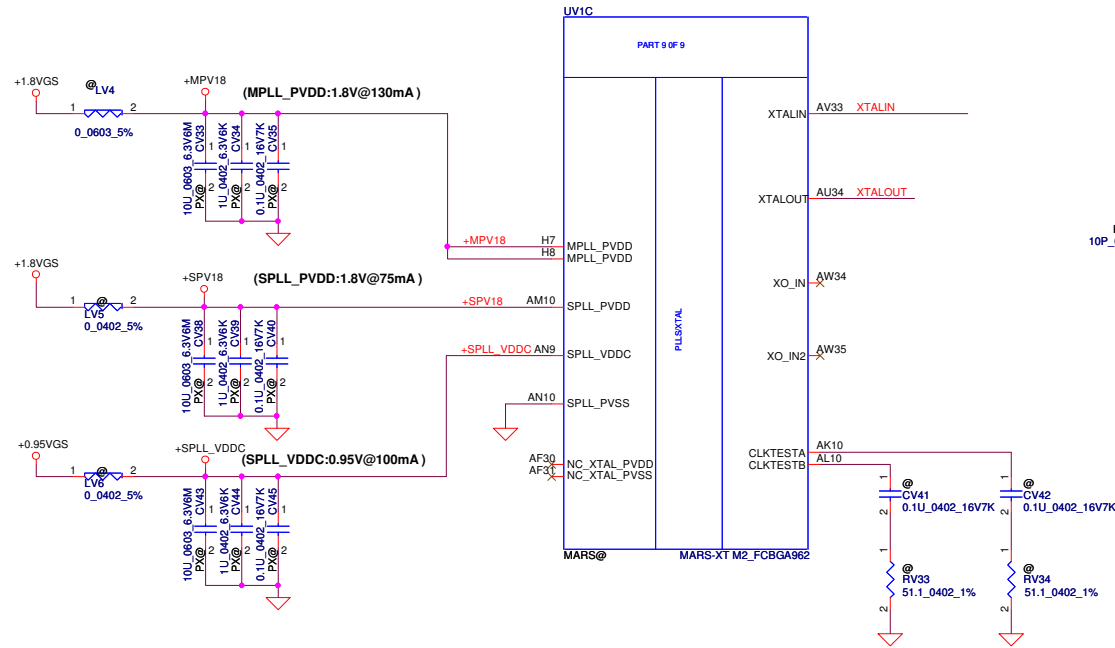


Place CLOSE VGA CHIP

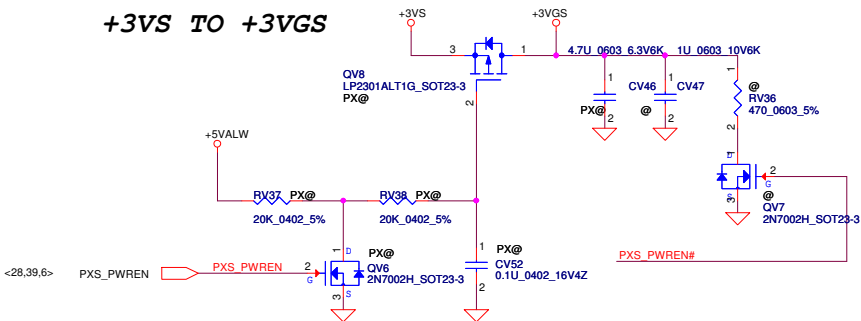
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

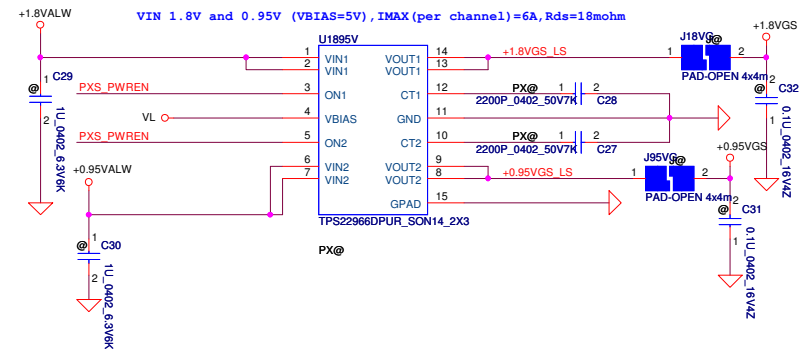
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



## +3VS TO +3VGS

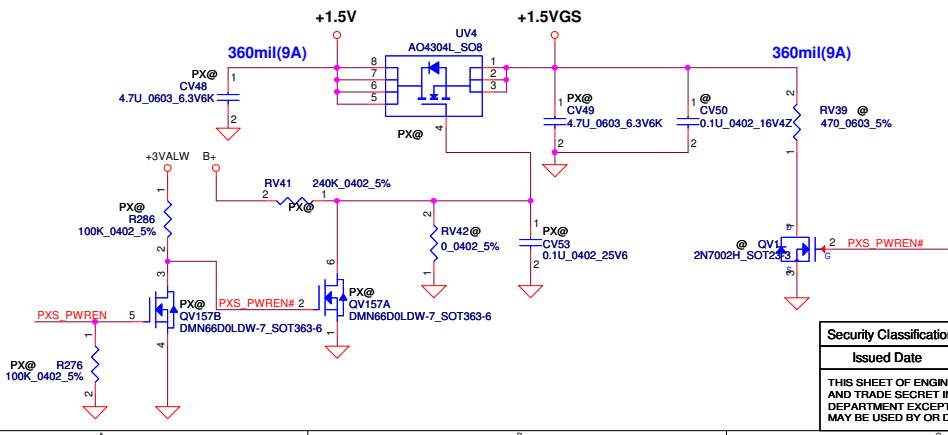


## +1.8VALW TO +1.8VGS +0.95VALW TO +0.95VGS Load switch

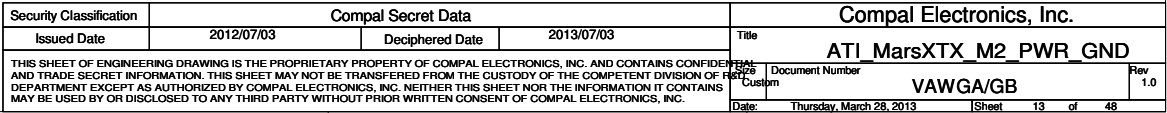


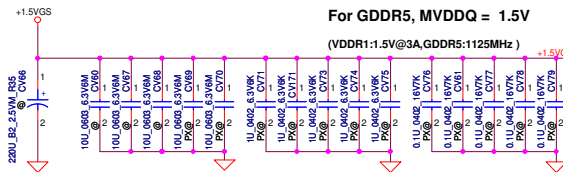
## +1.5V TO +1.5VGS

AO4430: Rds(on)=5.5mohm @ VGS=10V



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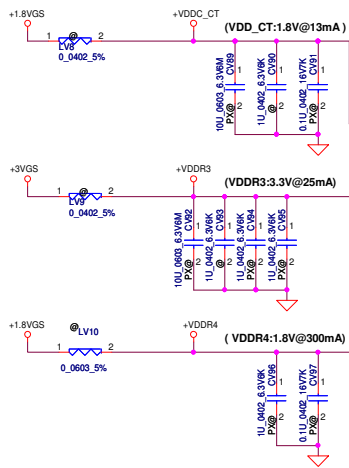


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

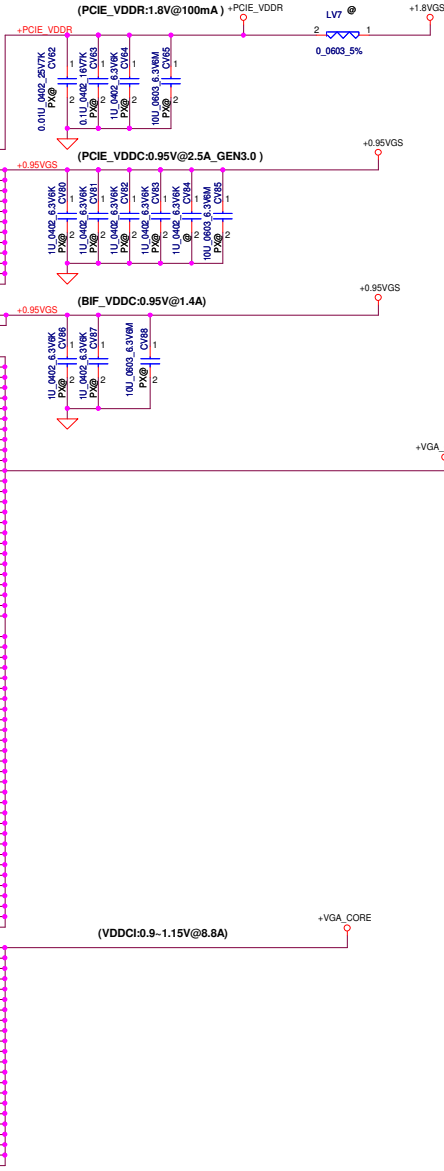
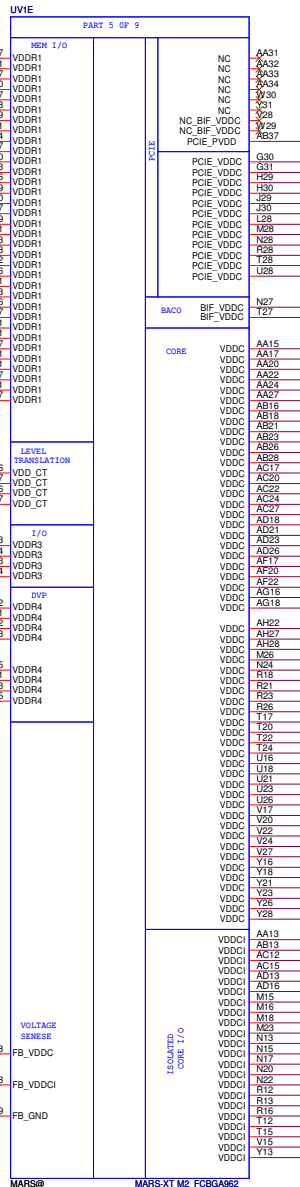
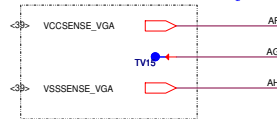
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



Route as differential pair

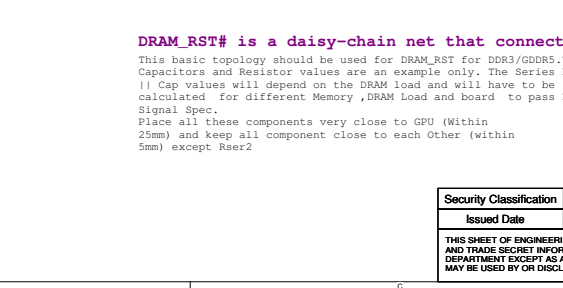
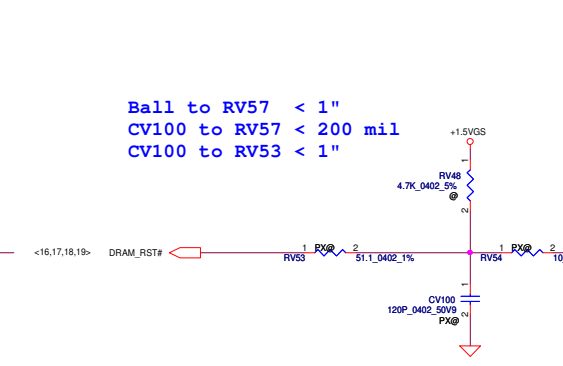
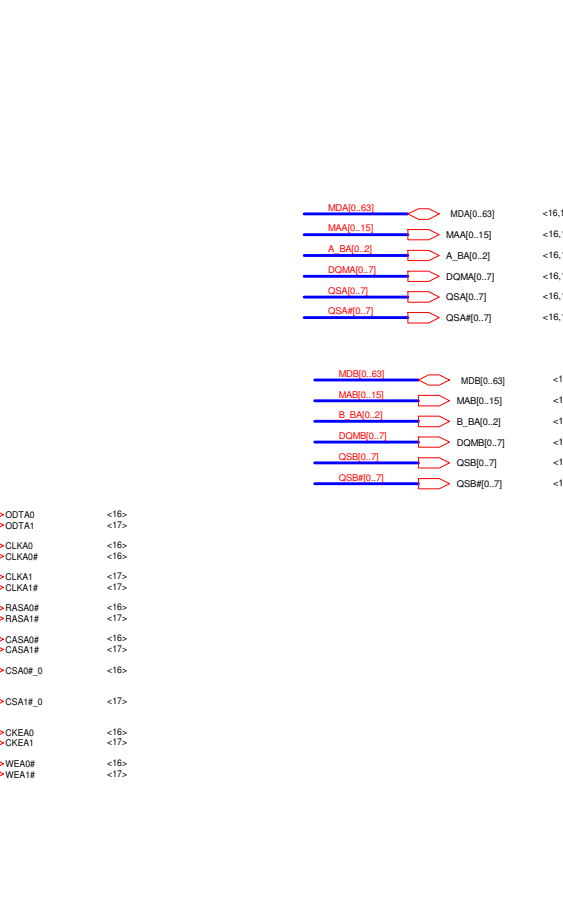
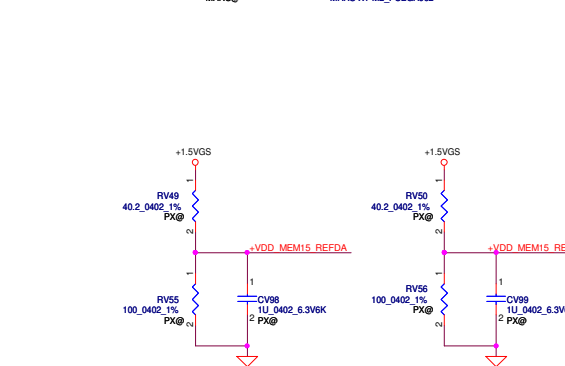
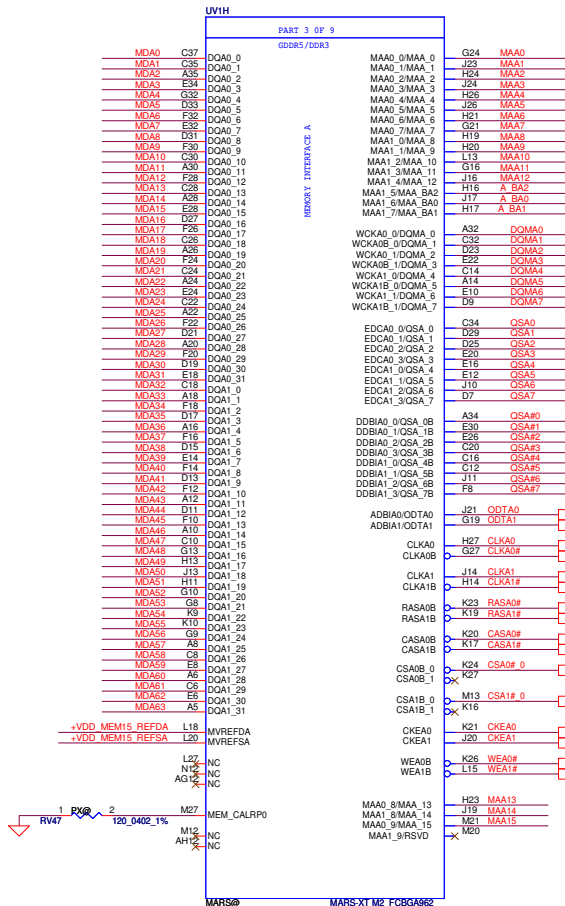


PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA\_CORE Cap in power side sheet






Ball to RV57 < 1"  
 CV100 to RV57 < 200 mil  
 CV100 to RV53 < 1"


**DRAM\_RST# is a daisy-chain net that connects to all VRAM**  
 This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.  
 Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2










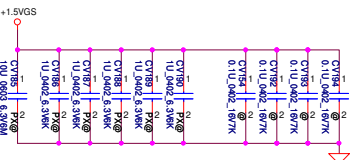
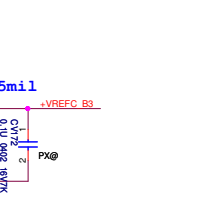
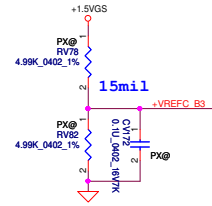
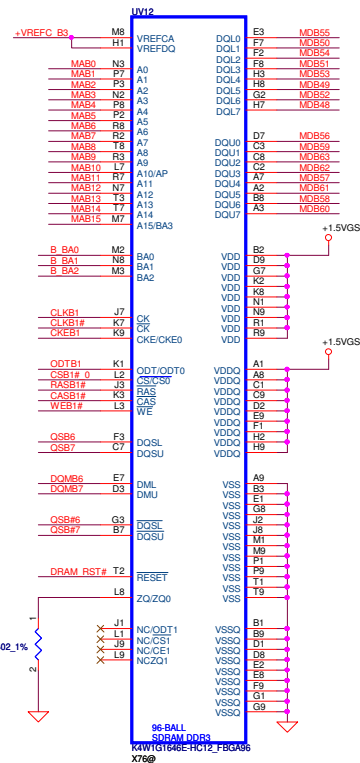
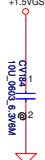
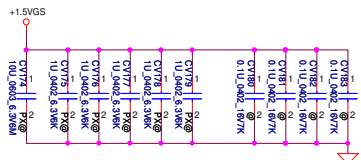
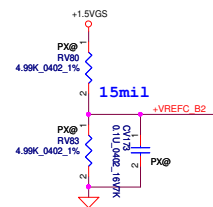
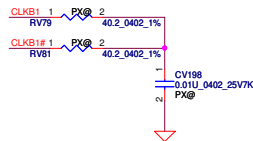
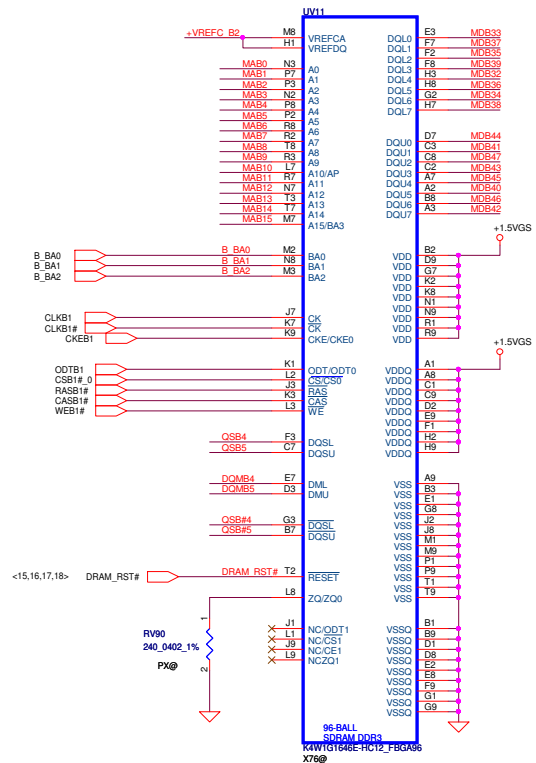
<15> MDB[32..63]  MDB[32..63]

<15,18> MAB[15..0]  MAB[15..0]

<15> DQMB[7..4]  DQMB[7..4]

<15> QSB[7..4]  QSB[7..4]

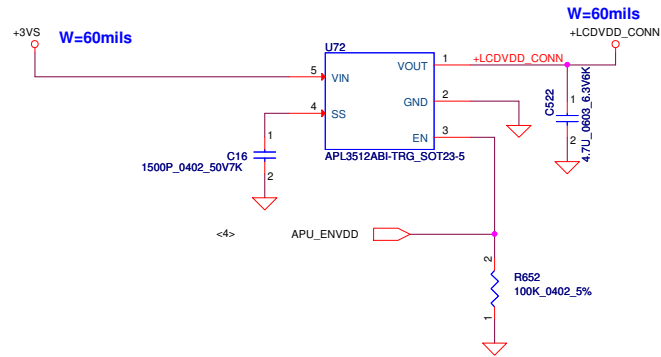
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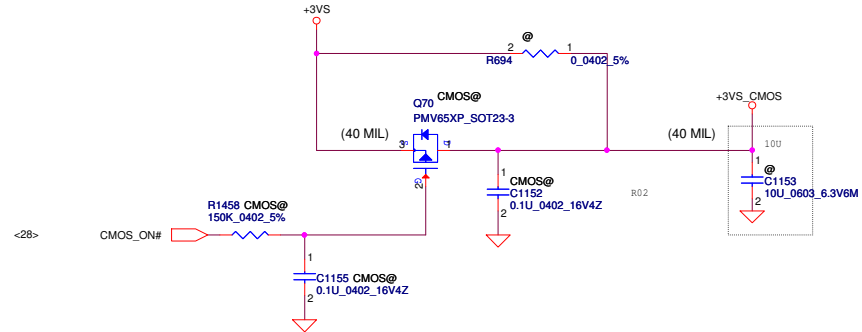




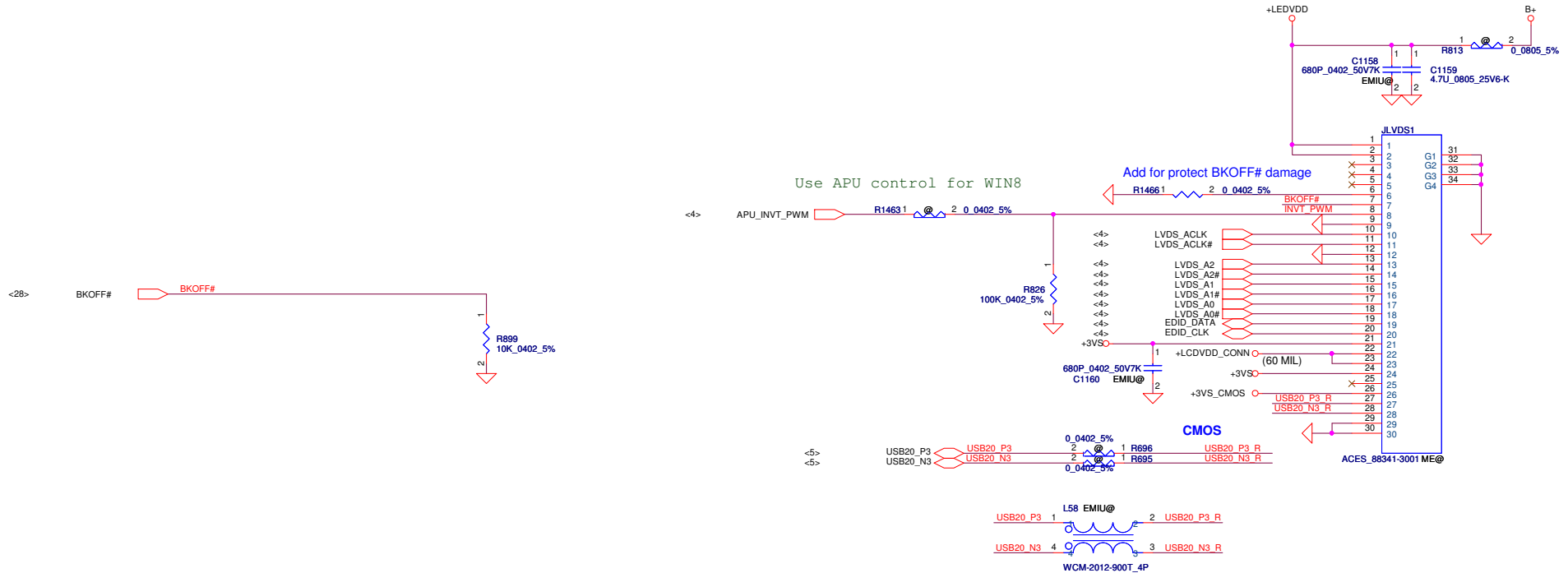
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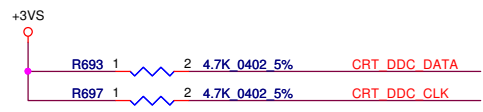
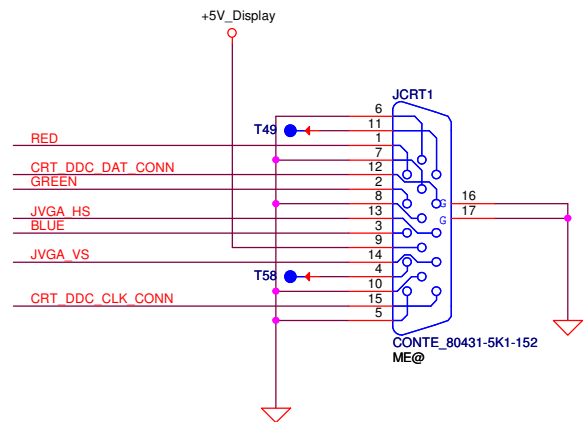
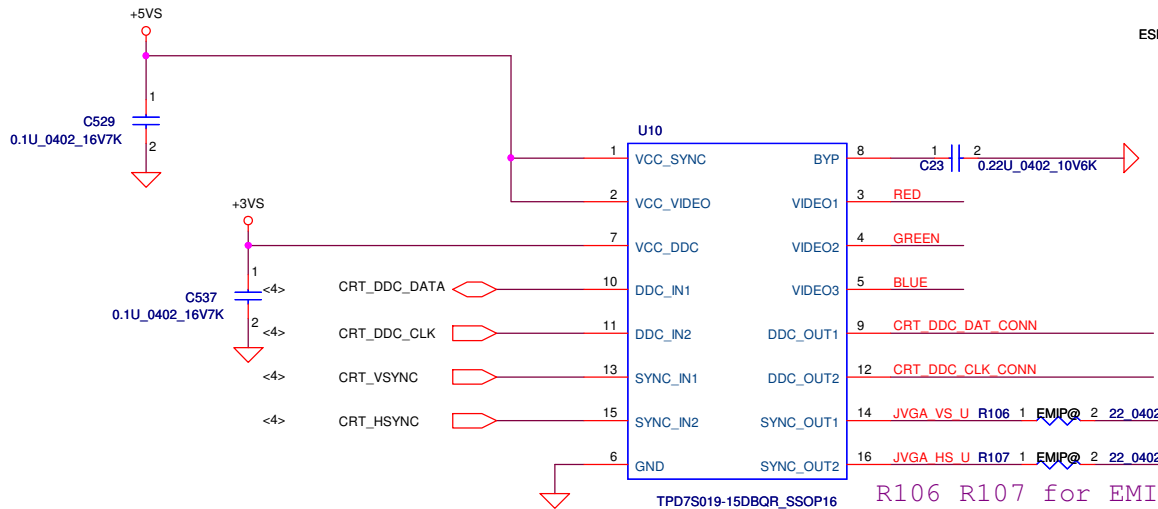
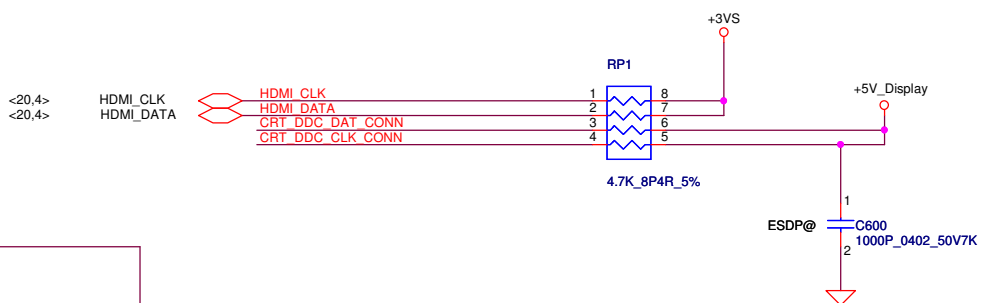
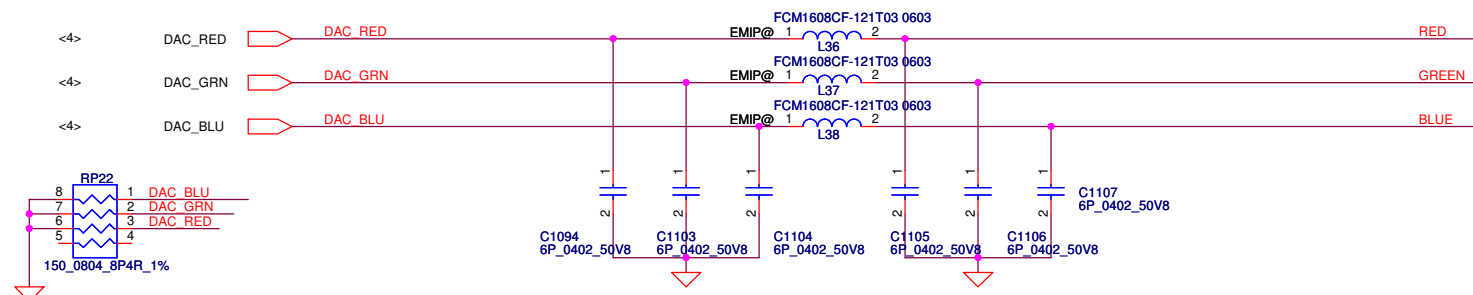
## CMOS Camera



## VGA LCD/PANEL BD. Conn.

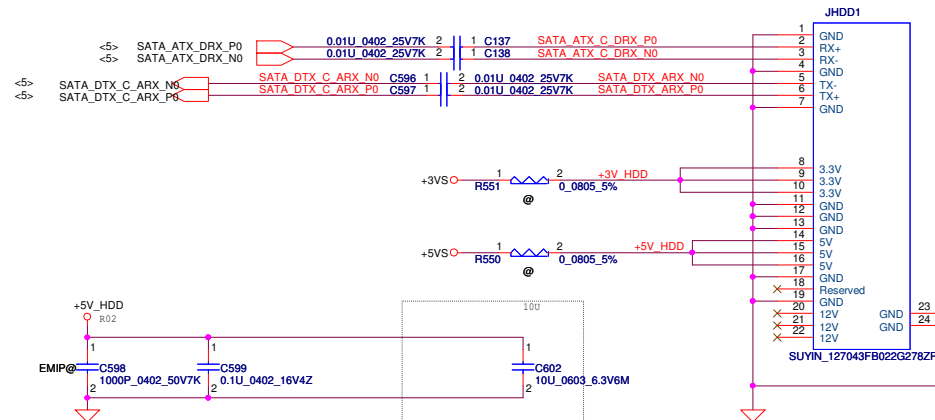


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				Date	Thursday, March 28, 2013
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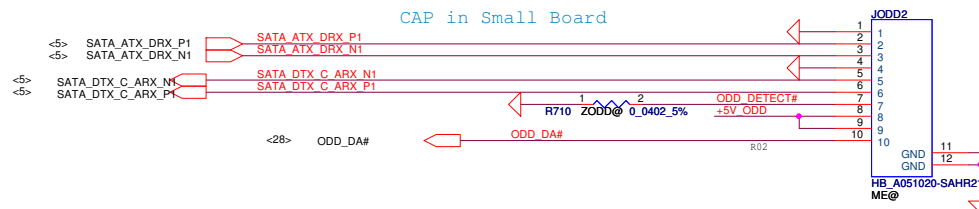


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								Size B	Document Number	Rev			
									VAWGA/GB	1.0			
								Date:	Thursday, March 28, 2013	Sheet	22	of	48

# SATA HDD Conn.

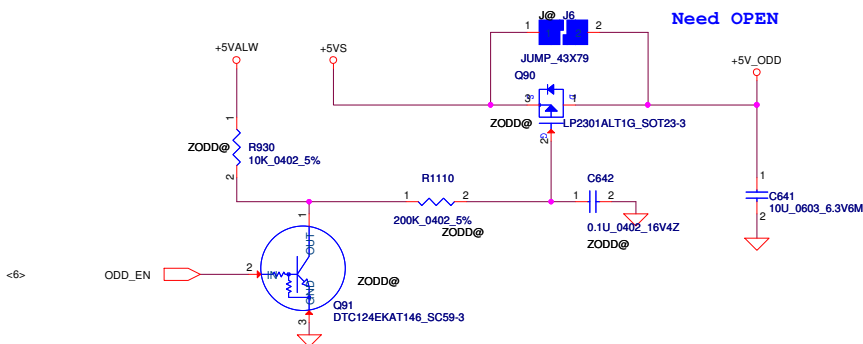


# FOR 15" SATA ODD FFC Conn.

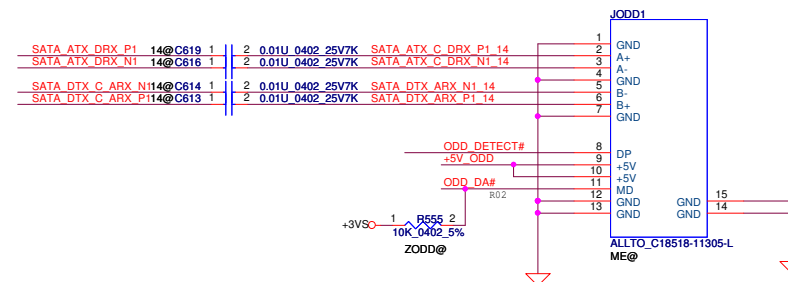


Co-lay

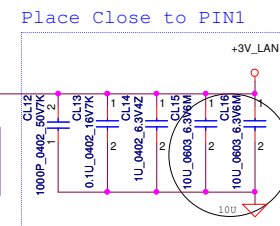
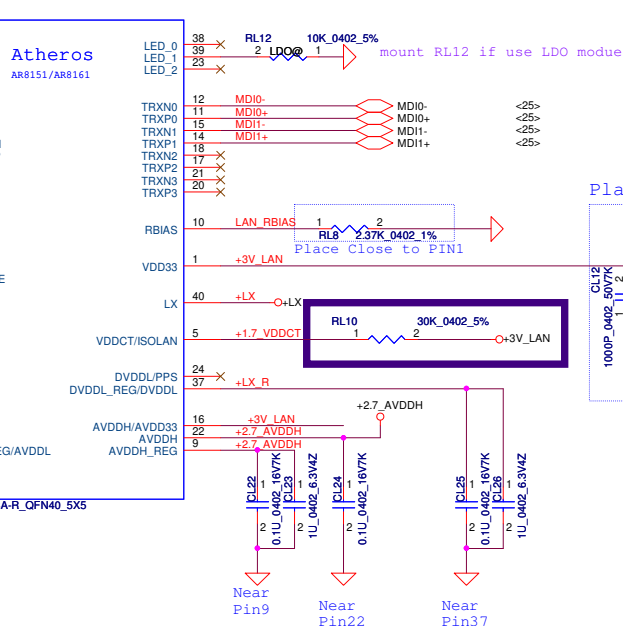
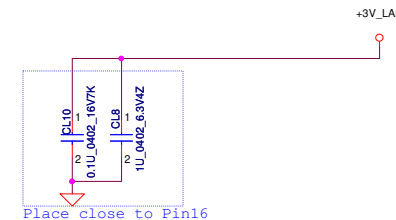
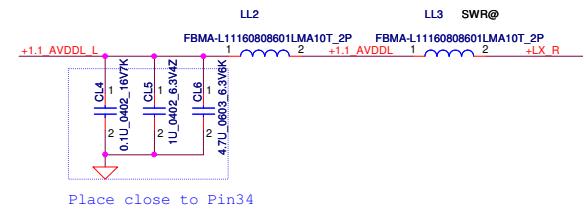
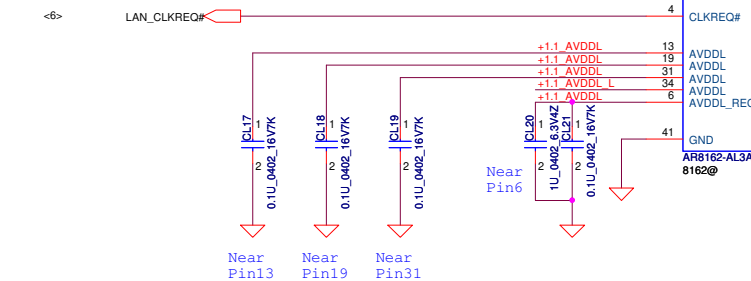
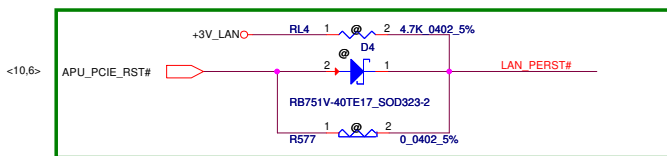
# ODD Power Control



# FOR 14" SATA ODD Conn.

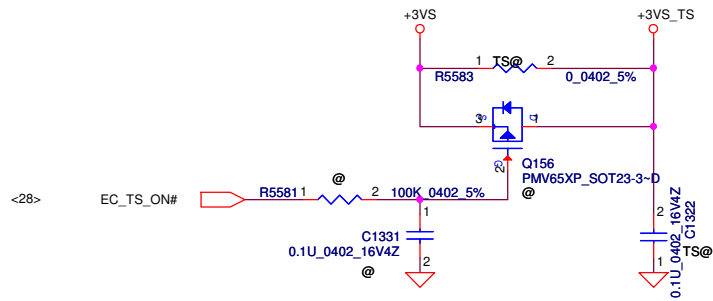


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						Document Number		VAWGA/GB		Rev 1.0	
						Date: Thursday, March 28, 2013				Sheet 23 of 48	

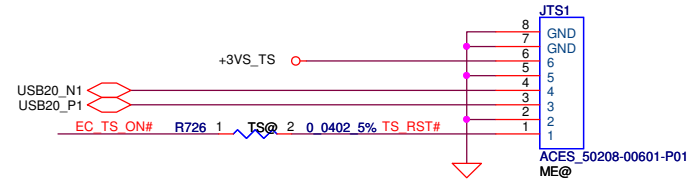


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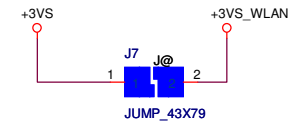
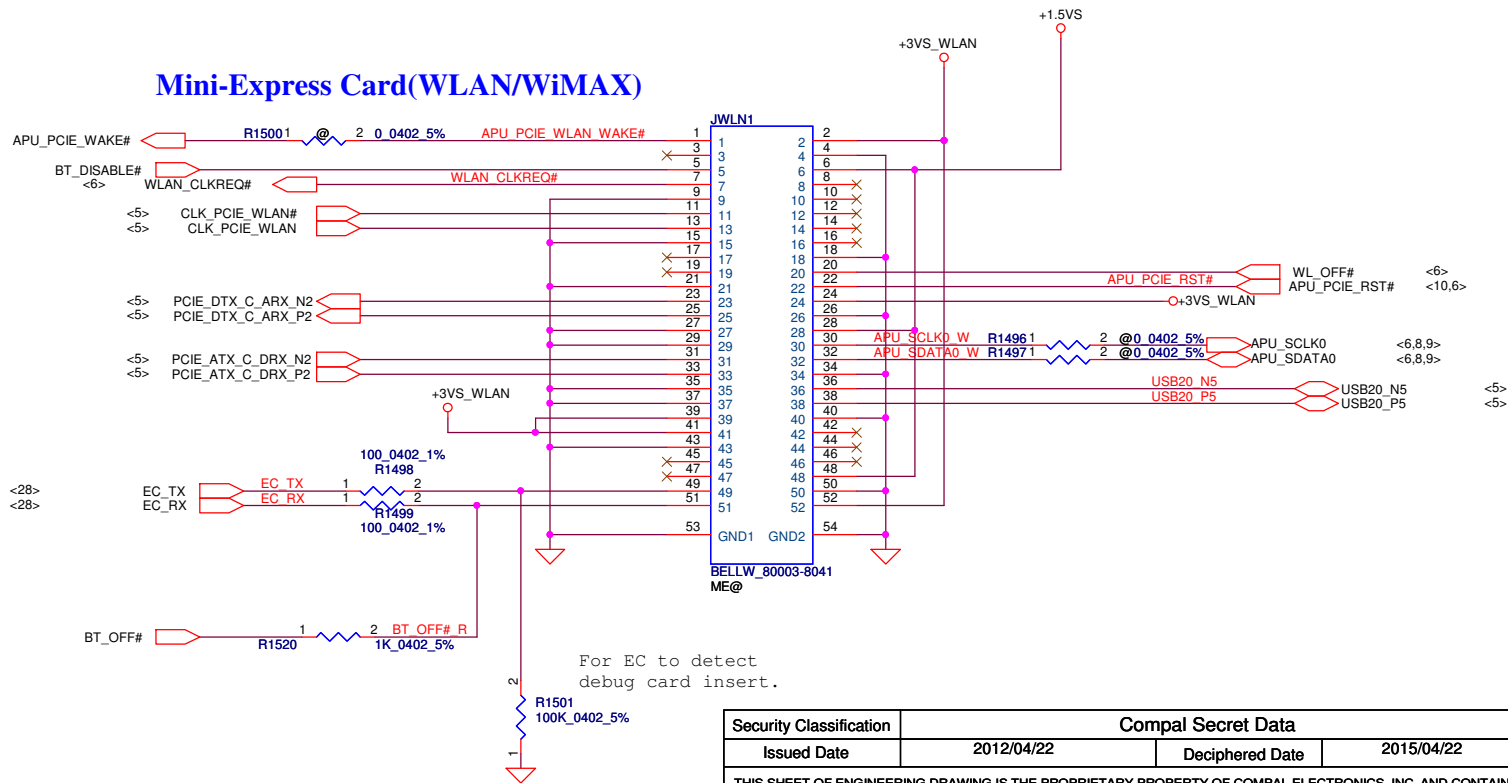




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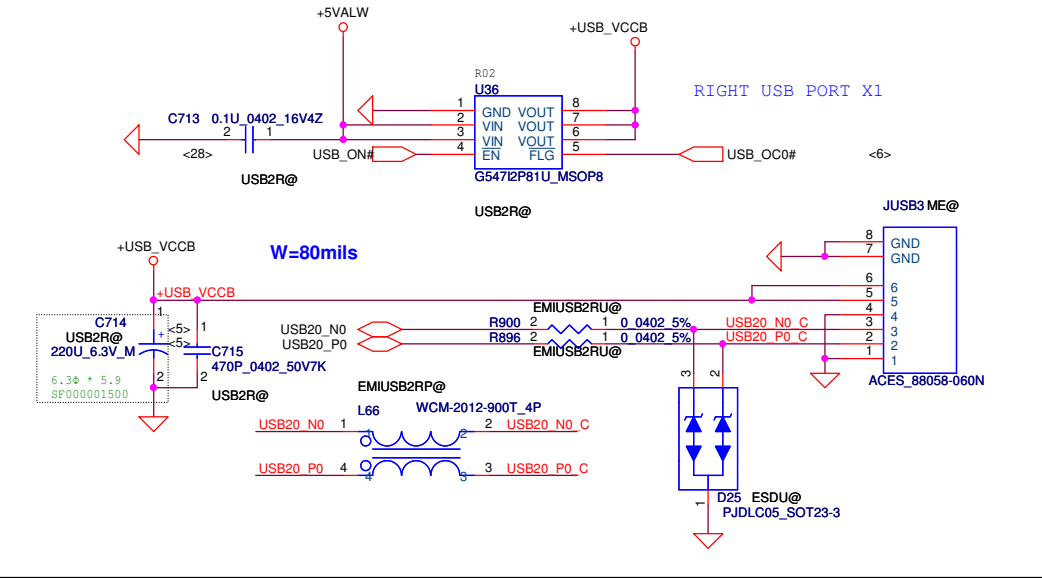
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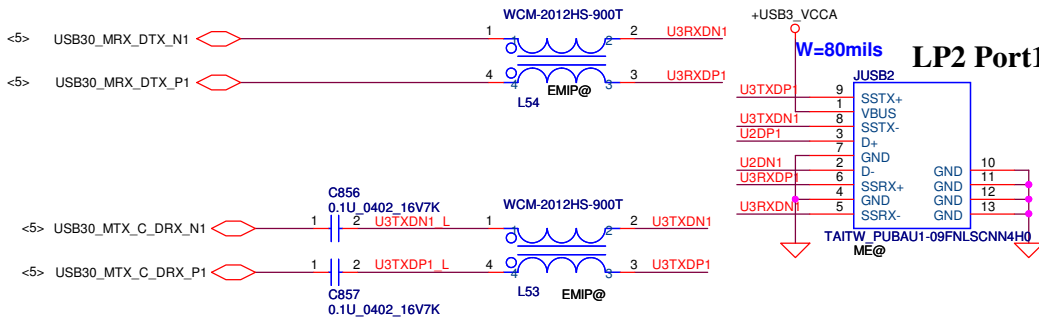
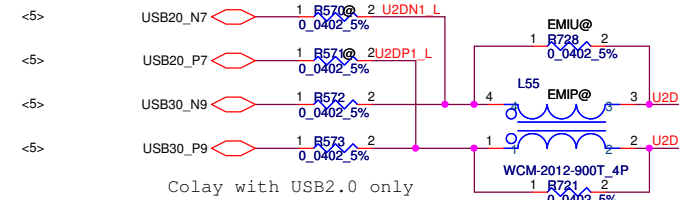
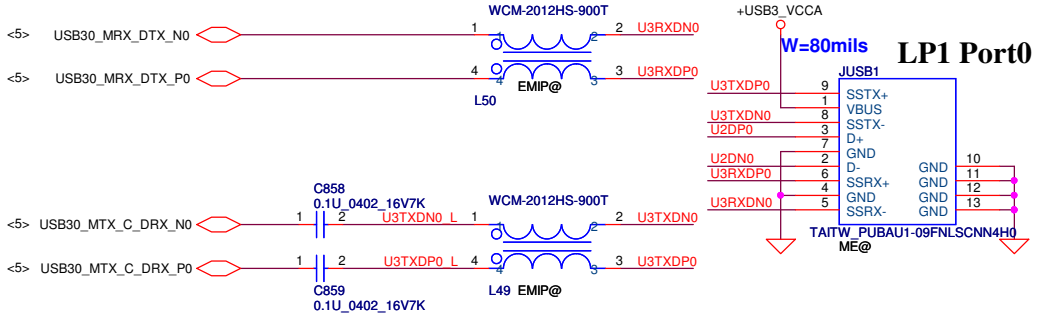
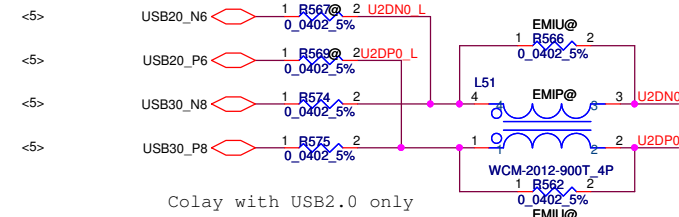
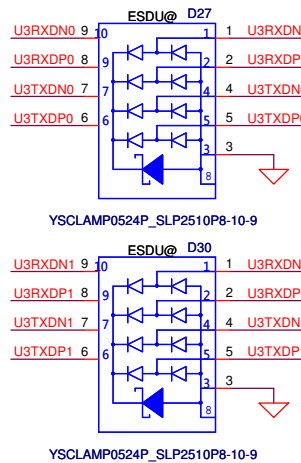
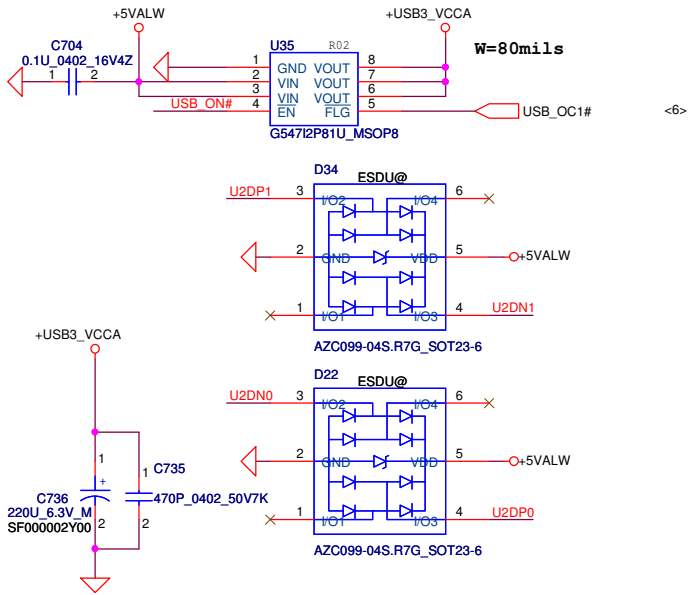
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										Document Number	
										VAWGA/GB	
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										Rev 1.0	



# Right Ext.USB Conn.

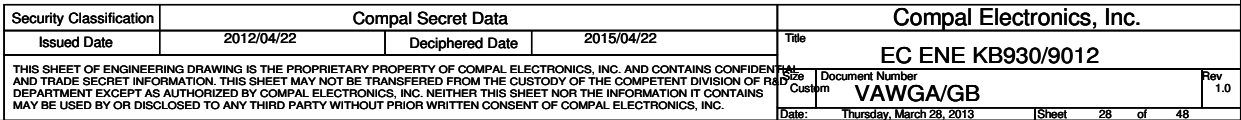


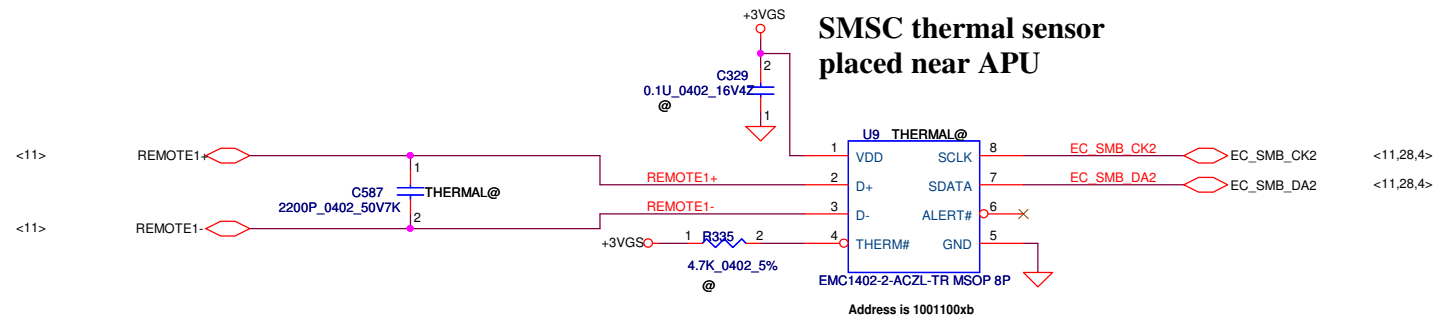
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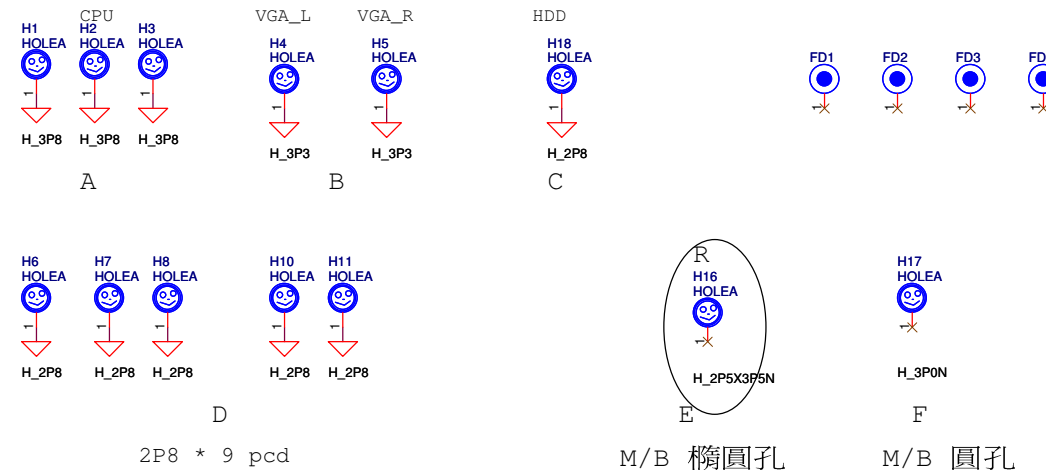
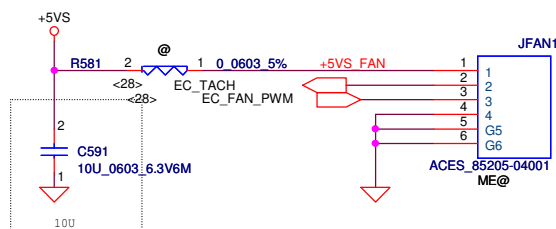
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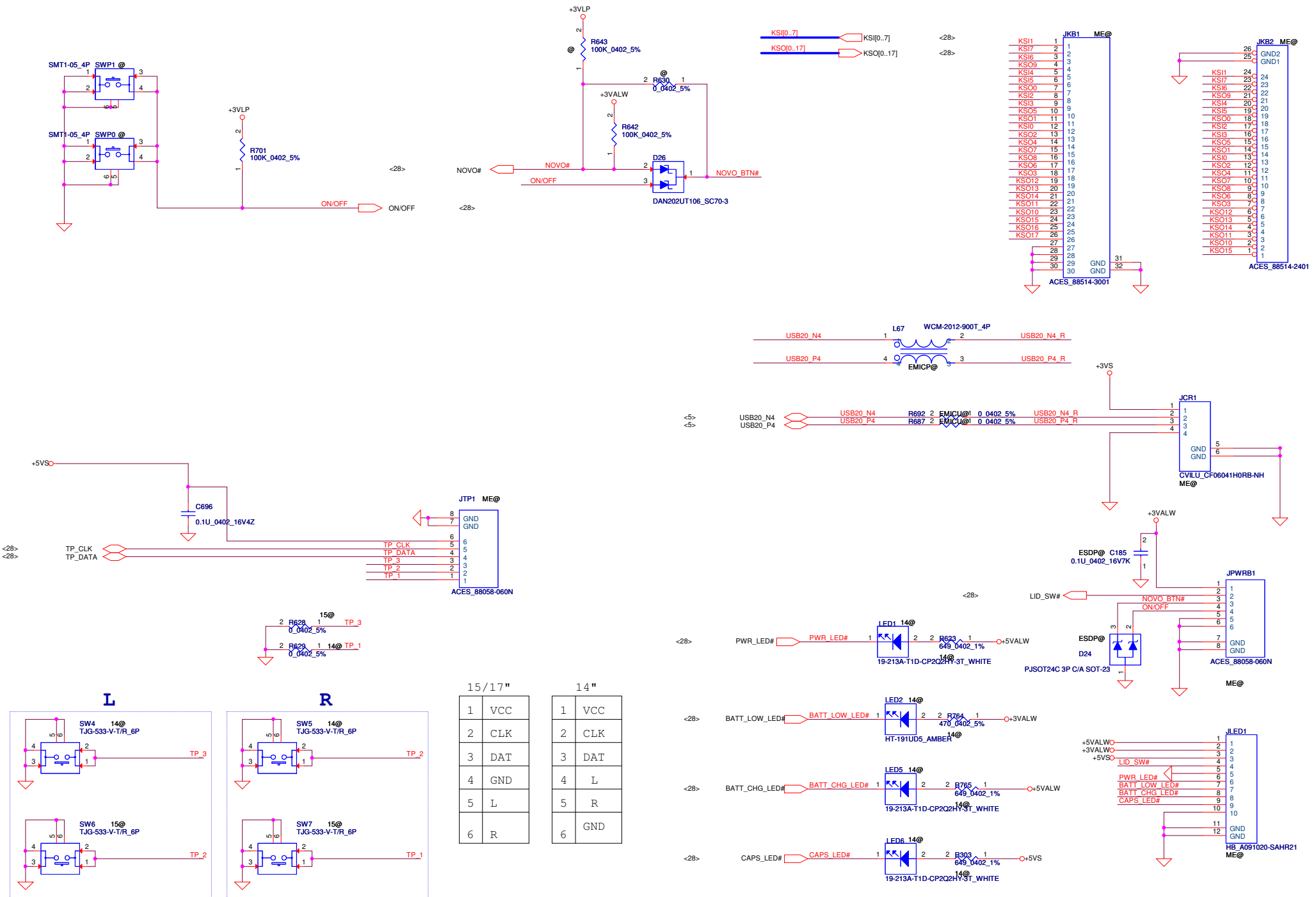


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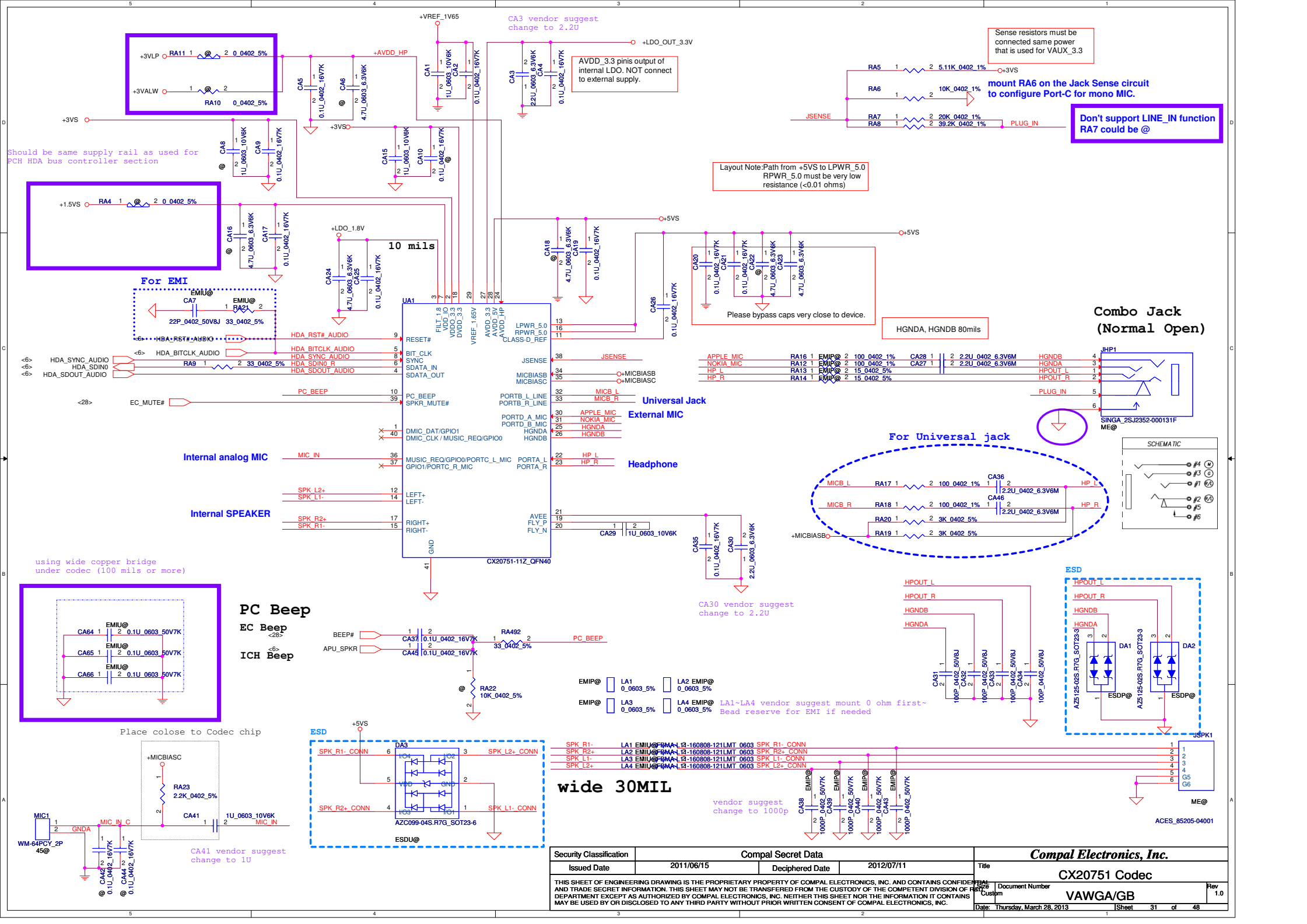
## FAN1 Conn



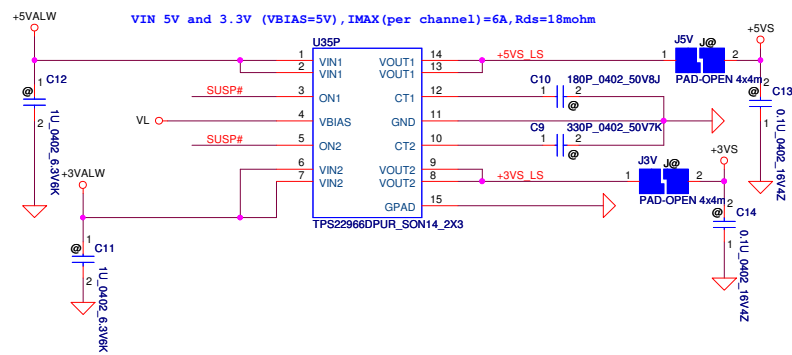
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				Date: Thursday, March 28, 2013	Sheet 29 of 48



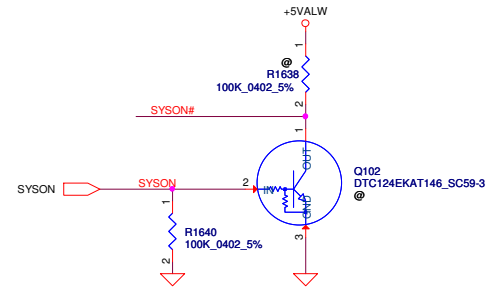
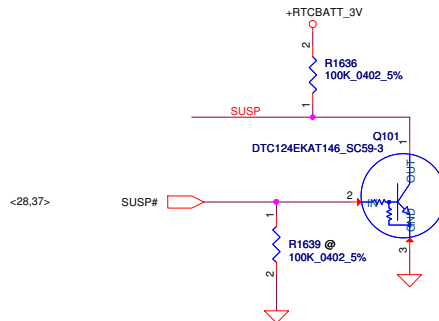
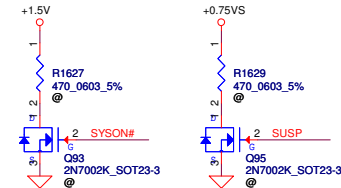
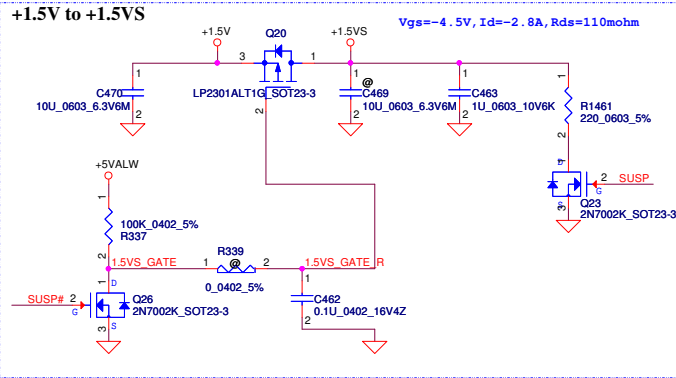
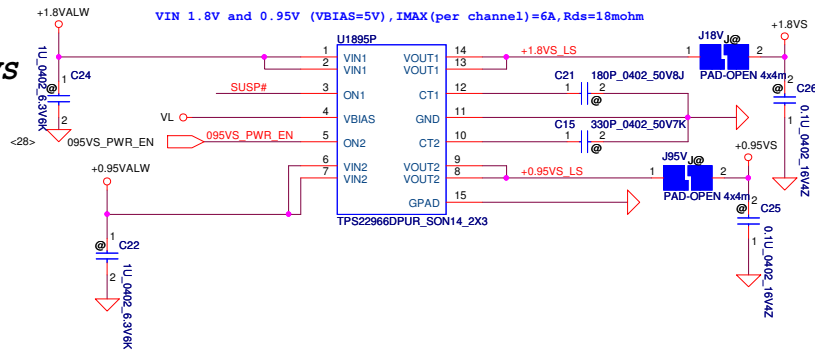
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								Docuement Number		Rev					
								VAWGA/GB		1.0					
								Date		Thursdav, March 28, 2013		Sheet		30 of 48	



**+5VALW TO +5VS**  
**+3VALW TO +3VS**  
**Load switch**

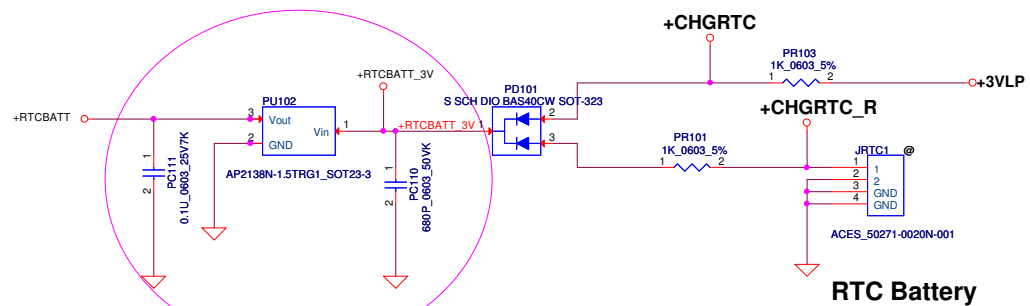
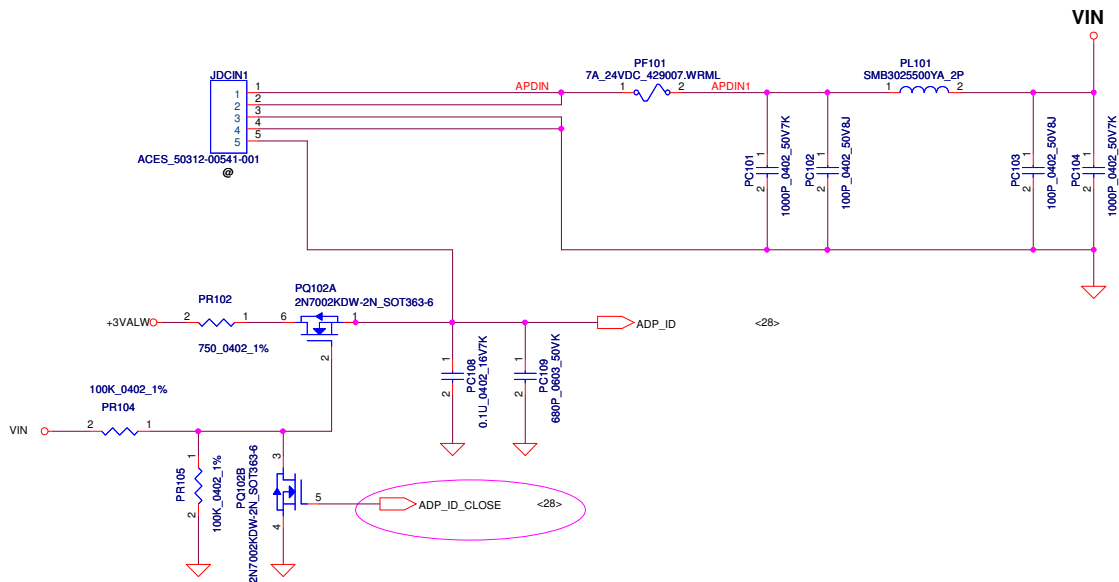


**+1.8VALW TO +1.8VS**  
**+0.95VALW TO +0.95VS**  
**Load switch**



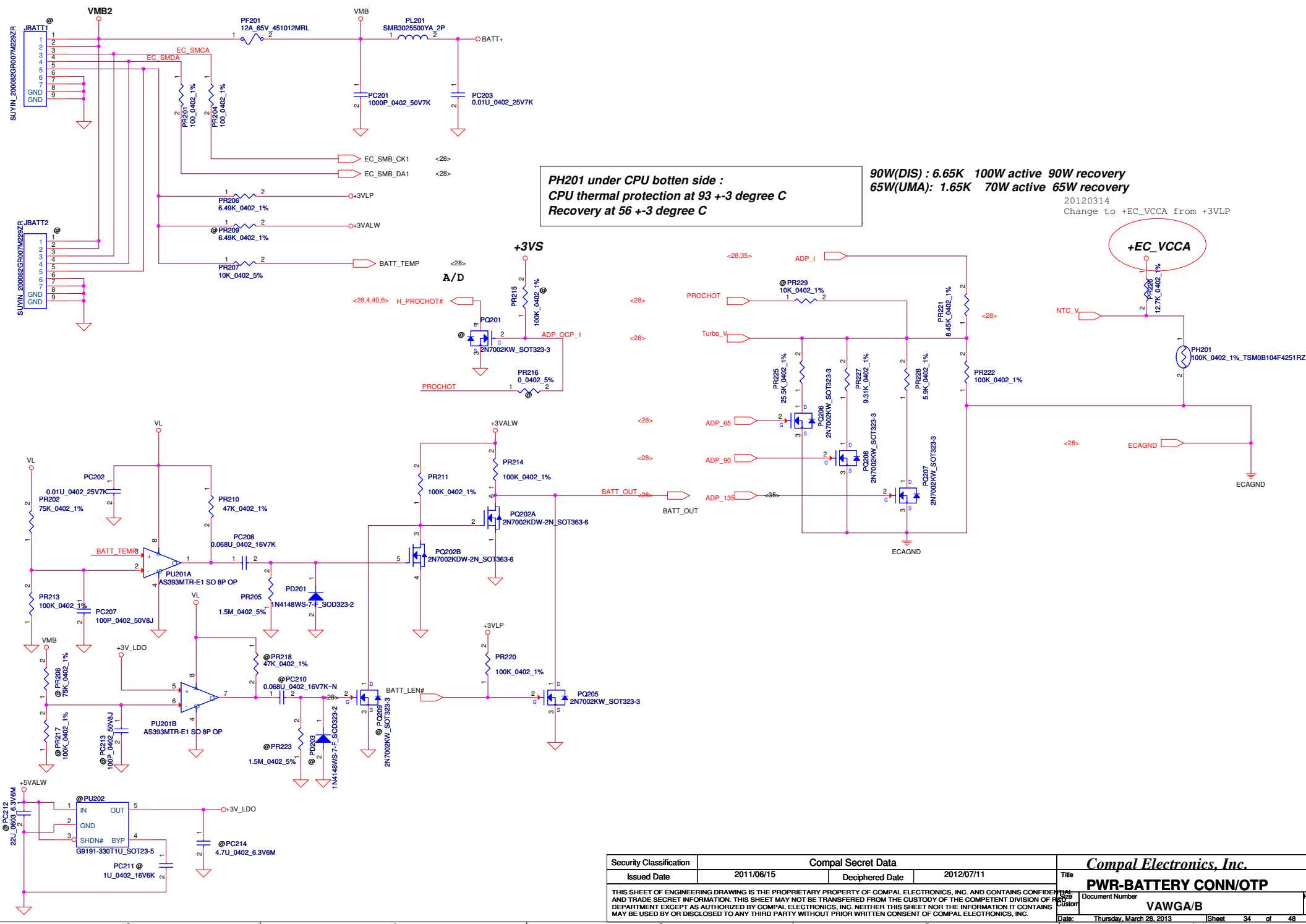
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Document Number													
VAWGA/GB													
Rev 1.0													
Date		Thursday, March 28, 2013		Sheet		32 of 48							



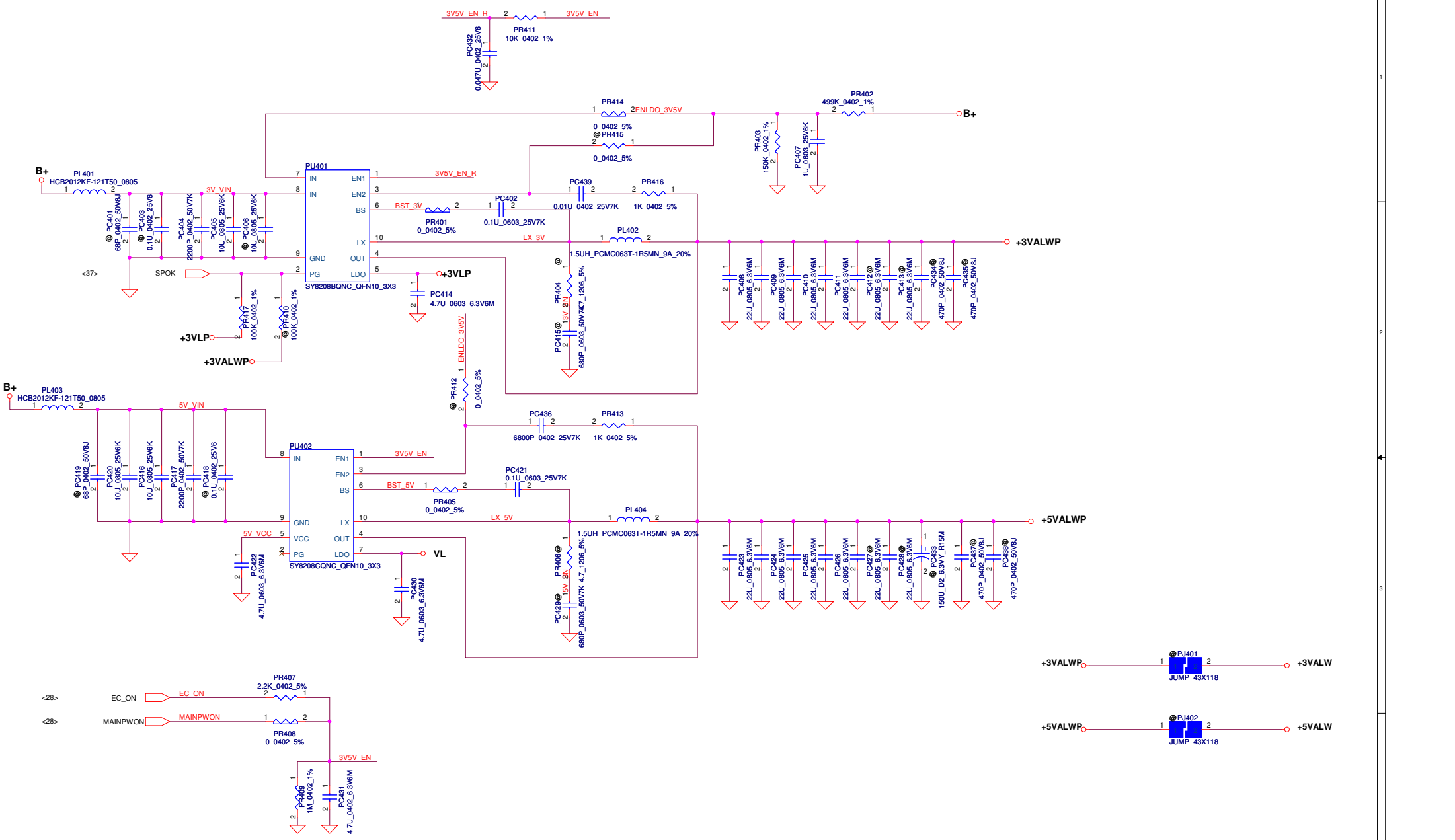


Need use +3.3V transfer to +1.5V LDO to APU side for Kaibini

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				Date:	Thursday, March 28, 2013
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				VAWGA/GB	1.0
Date: Thursday, March 28, 2013				Sheet	48



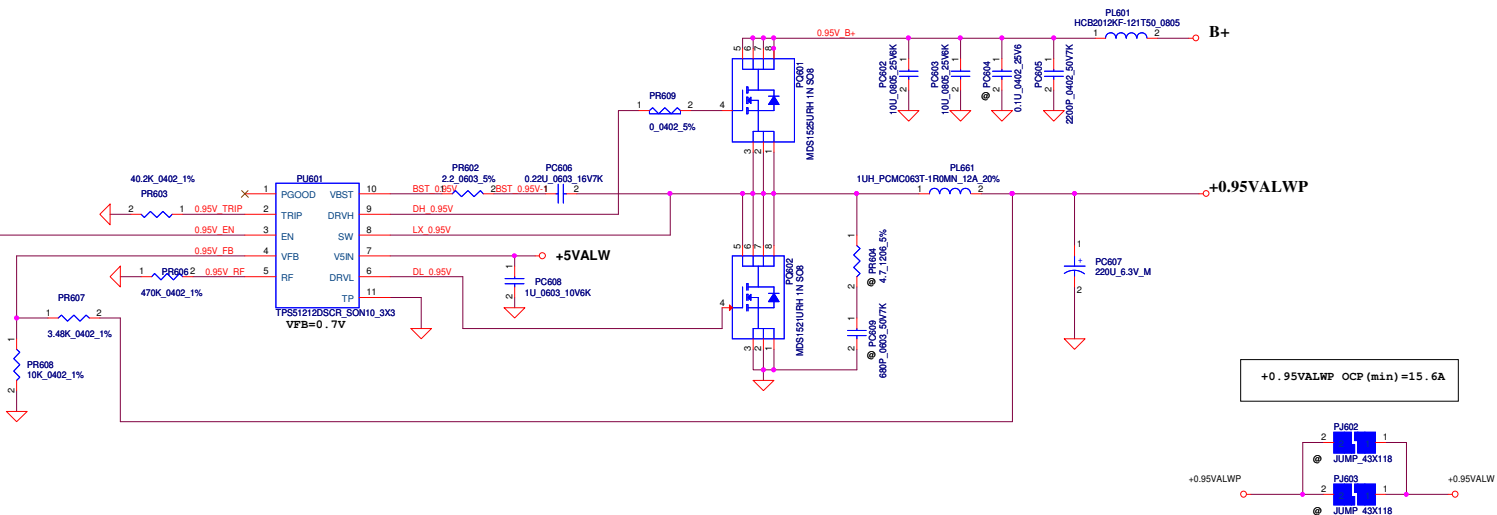
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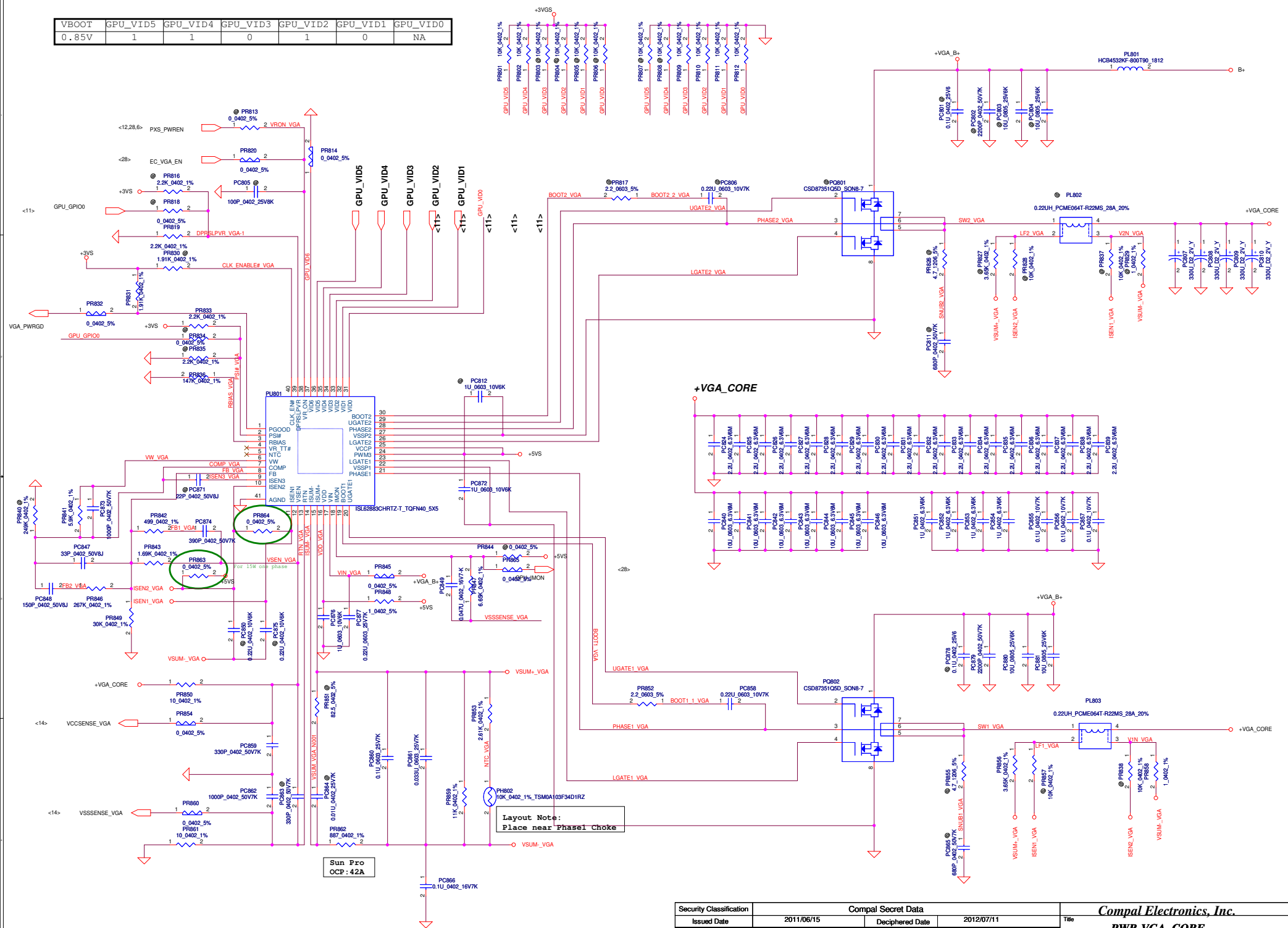
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SPOK

PR605 reserve

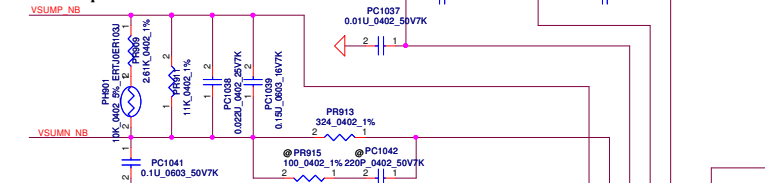


VBOOT	GPU_VID5	GPU_VID4	GPU_VID3	GPU_VID2	GPU_VID1	GPU_VID0
0.85V	1	1	0	1	0	NA

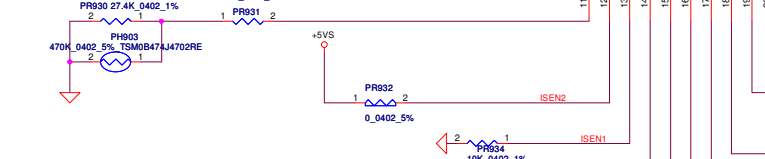
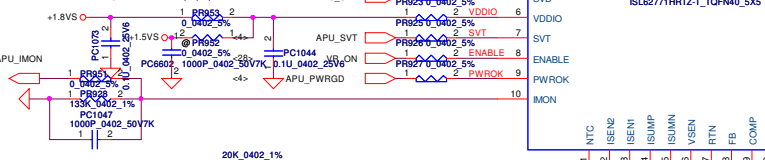
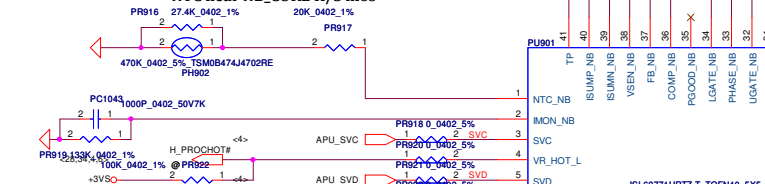


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				Size	Document Number	Rev
				C	VAWGA/GB	1.0
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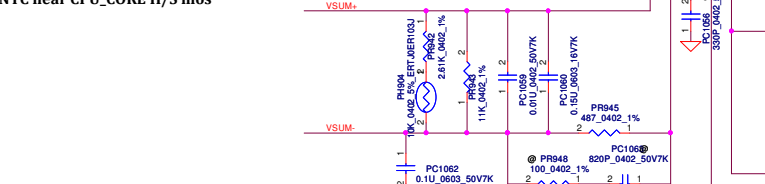
2011/10/21  
NTC near phase 1 choke



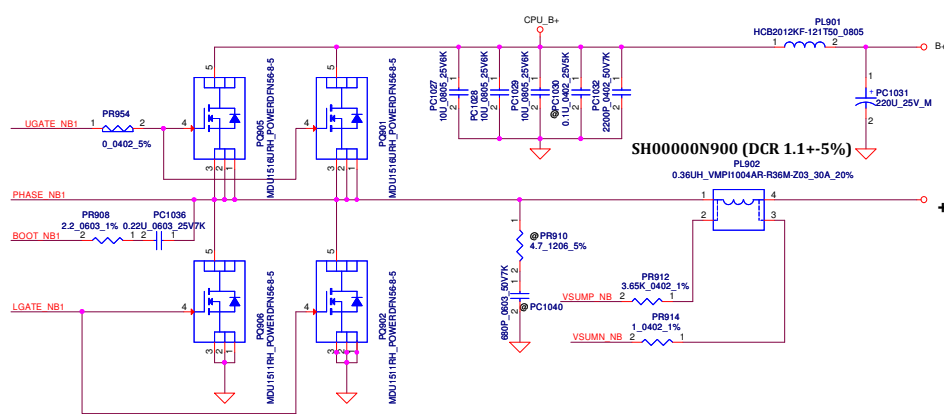
2011/10/21  
NTC near NB\_CORE H/S mos



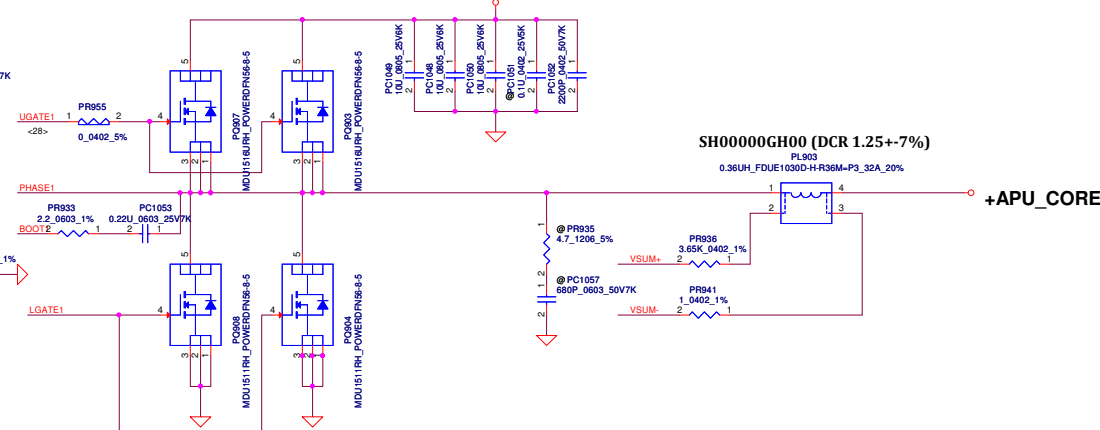
2011/10/21  
NTC near CPU\_CORE H/S mos



2011/10/21  
NTC near phase 1 choke

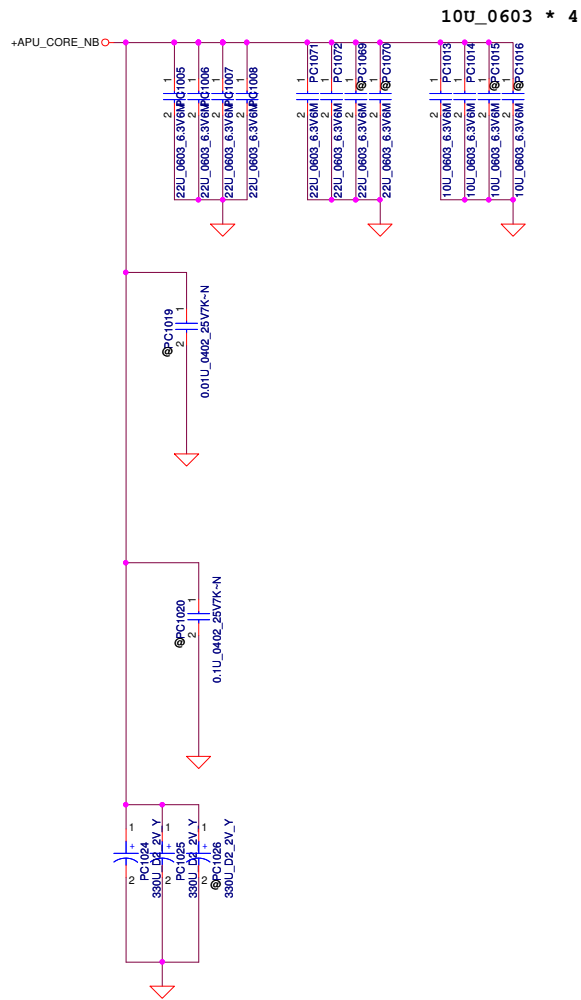
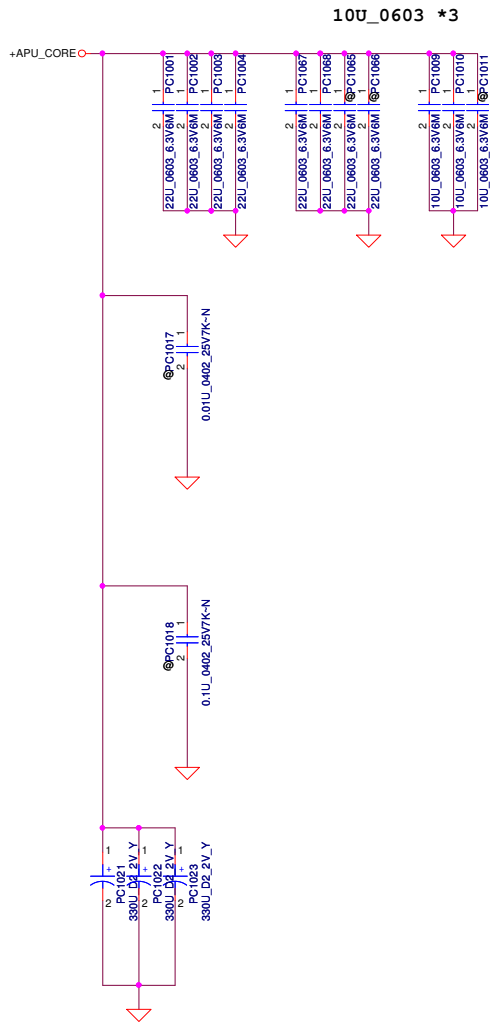


2012/10/30  
Load Line:VDD-->4m  
VDDNB-->4.0m



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				Date	Thursday, March 28, 2013	Sheet 41 of 48

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

## Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For share rom	28	Change SYS_PWRGD_EC from pin 86 to pin 32	12/17	DVT
2	For 095VS_PWR_EN pull down	28	Add R207	12/17	DVT
3	For VBIAS first raise up	12, 32	Change U1895V, U35P, U1895P VBIAS from +5VALW to VL	12/17	DVT
4	For follow VIWGP design	27	Change JUSB3 pin define	12/18	DVT
5	For Audio Precision	31	Change CA36, CA46 from 1U to 2.2U	12/21	DVT
6	For SYS_PWRGD_EC pull down	28	Add R208	12/24	DVT
7	For share rom	28	Change R1575, R1576 to 100K	12/24	DVT
8	For reserve EC +3VL	28 05	Add J11, J12 and modify +3VALW to +3V_EC	12/24	DVT
9	For share ROM	05	modify ROM net-name & resistor value	12/24	DVT
10	For common VIWGP design	22	modify R106, R107 to 22ohm	12/24	DVT
11	For power S3 reduction	28	Change EC_INVT_PWM to ADP_ID_CLOSE	12/25	DVT
12	For common VIWGP design	23	Change JODD1 symbol	12/27	DVT
13	For reserve wake on wlan function	26	Add R1500	12/27	DVT
14	For 1.5VS discharge	32	Change R339 to 0ohm, mount Q23 & R1461	12/29	DVT
15	For AMD suggest	4	Change R576 to 0ohm	12/29	DVT
16	For VGA sequence	12	Delete R123 & C40, change C28, C27 to 2200P	12/29	DVT
17	For +3VALW APU Power Consumption	7	Add R582	01/03	DVT
18	For ESD request	22 28 40	Add C600, C601, PC6601, PC6602	01/03	DVT
19	For no support DC wake & LID function	28	Pull high only SMB & RST use +3V_EC, other use +3VALW	01/04	DVT
20	For reserve cost down experiment	30	Add R630, R643	01/04	DVT
21	For Common VIWGP	30	Change SW4, SW5, SW6, SW7 footprint	01/04	DVT
22	For instant plug/unplug AC has beep sound	31	@RA22	01/04	DVT
23	For Crystal Capactance fine tune	5 6 12	Modify C794, C795, C682, C686, CV36, CV37 value	01/09	DVT

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## Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For EMI request	30	Change L67 to EMICP@, Change R692,R687 to EMICU@	02/02	PVT
2	For Share ROM recoverable solution as original method	05	Add RP12	02/02	PVT
3	For BIOS post time	06	Pull high PXS_PWREN to +3VS by RP14	02/02	PVT
4	For ZiZi noise	31	Change AVDD_HP from +3VS to +3VLP	02/02	PVT
5	For follow KABINI latest CRB	04	@ R576,C164,C342	02/02	PVT
6	For APU control PWM only	21	Delete R1465	02/02	PVT
7	For Corret Net-name to prevet confuse	04 21	Change TL_INVT_PWM, TL_ENVDD to APU_INVT_PWM, APU_ENVDD	02/02	PVT
8	For Reserve DDC CLK DATA pull high	22	Add R693, R697	02/02	PVT
9	For Common Intel project	30	Change R623,R765,R303 to 620ohm	02/02	PVT
10	For Common Intel project	23	Reserve R551	02/02	PVT
11	For reduce BOM	31	Delete RA3, and Change RA4 to short-pad	02/05	PVT
12	For reduce BOM	26	Change R1498,R1499 from 0 ohm to 100 ohm	02/05	PVT
13	For reduce BOM	11 12 13 14	Change RV43, LV1, LV2, LV3, LV4, LV5, LV6, RV16, RV17, LV7, LV8, LV9, LV10 to short-pad	02/05	PVT
14	For better location	14 18 19	CV72 <-> CV171 ; CV60 <-> CV70 ; CV154 <-> CV191	02/05	PVT
15	For reduce BOM	21	Change R1463 from 0 ohm to short-pad	02/06	PVT
16	For better audio precision performance	31	Change CA27,CA28 from 1U to 2.2U	02/08	PVT
17	For reduce BOM & layout concern	07	Delete C195	02/16	PVT
18	For test point request	22	Add T49, T58 on JCRT1	02/18	PVT
19	For ESD request	25	Add C173, C178	02/18	PVT
20	For reduce BOM	05	Change R112, R115, R116, R119, R125, R126 to short-pad	02/18	PVT
21	For Crystal timing	06	Change C682 from 18P to 22P	02/20	PVT
22	For ESD request	30	Change D24 from ESDU@ to ESDP@, Part number from SCA00000E00 to SCA00001G00	02/23	PVT
23	For EMI request	21 27 30	Change L58,L51,L55,L66,L67 from SM070000K00 to SM070000Z00	02/23	PVT

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				Size	Document Number	Rev	
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Mars XT VRAM STRAP

2G

1G

Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
K4W2G1646E-BC1A SA000068U00	0	0	0	RV20 NC	RV27 4.75K
MT41J128M16JT-093G:K SA000067500	0	0	1	RV20 8.45K	RV27 2K
H5TQ2G63DFR-N0C SA000065300	0	1	0	RV20 4.53K	RV27 2K
H5TC2G63FFR-11C SA00006H400	1	0	0	RV20 4.53K	RV27 4.99K
K4W1G1646G-BC11 SA00004GS00	0	1	1	RV20 6.98K	RV27 4.99K
H5TQ1G63EFR-11C SA000041SB0	1	1	1	RV20 4.75K	RV27 NC

MS2G@ X7646738L01  
MM2G@ X7646738L02  
OLDMH2G@ X7646738L09  
NEWMH2G@ X7646738L10  
MS1G@ X7646738L03  
MH1G@ X7646738L04

SUN PRO VRAM STRAP

2G

1G

Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
K4W4G1646B-HC11 SA000068R00	0	0	0	RV20 NC	RV27 4.75K
MT41K256M16HA-107G:E SA000065D00	0	0	1	RV20 8.45K	RV27 2K
H5TQ4G63MFR-11C SA00006DG00	0	1	0	RV20 4.53K	RV27 2K
K4W2G1646E-BC1A SA000068U00	0	1	1	RV20 6.98K	RV27 4.99K
MT41J128M16JT-093G:K SA000067500	1	1	0	RV20 3.4K	RV27 10K
H5TC2G63FFR-11C SA00006H400	1	0	0	RV20 4.53K	RV27 4.99K
H5TQ2G63DFR-N0C SA000065300	1	1	1	RV20 4.75K	RV27 NC

SS2G@ X7646738L05  
SM2G@ X7646738L06  
SH2G@ TBD  
SS1G@ X7646738L07  
SM1G@ X7646738L08  
NEWSH1G@ X7646738L13  
OLDSH1G@ X7647538L01

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(3.3VGS)

PCIE\_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD\_CT(1.8V)

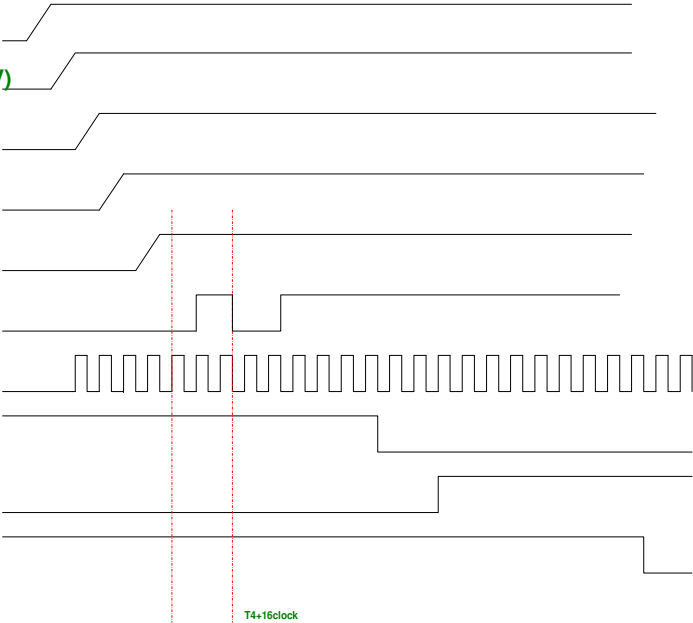
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REFCLK

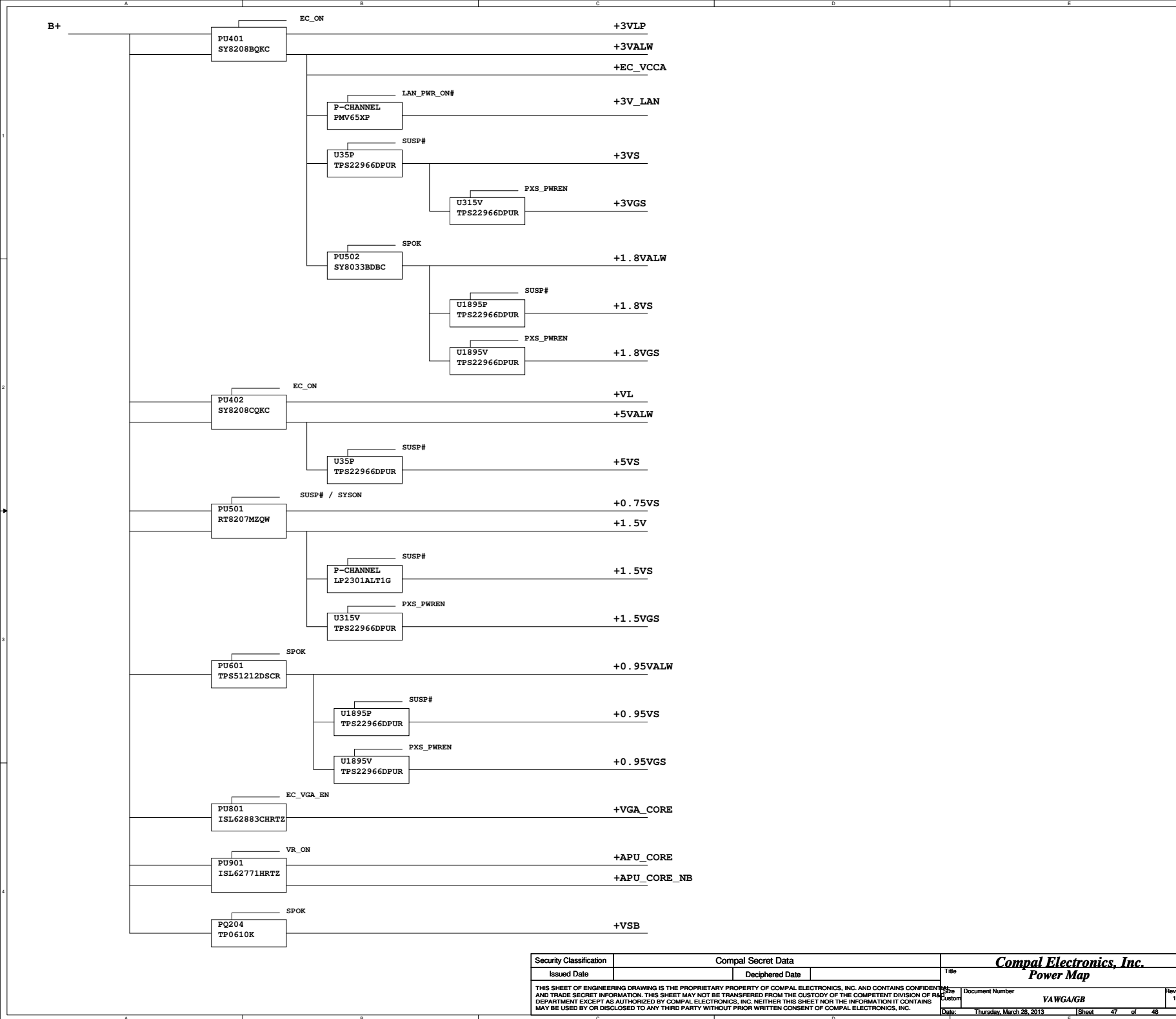
Straps Reset

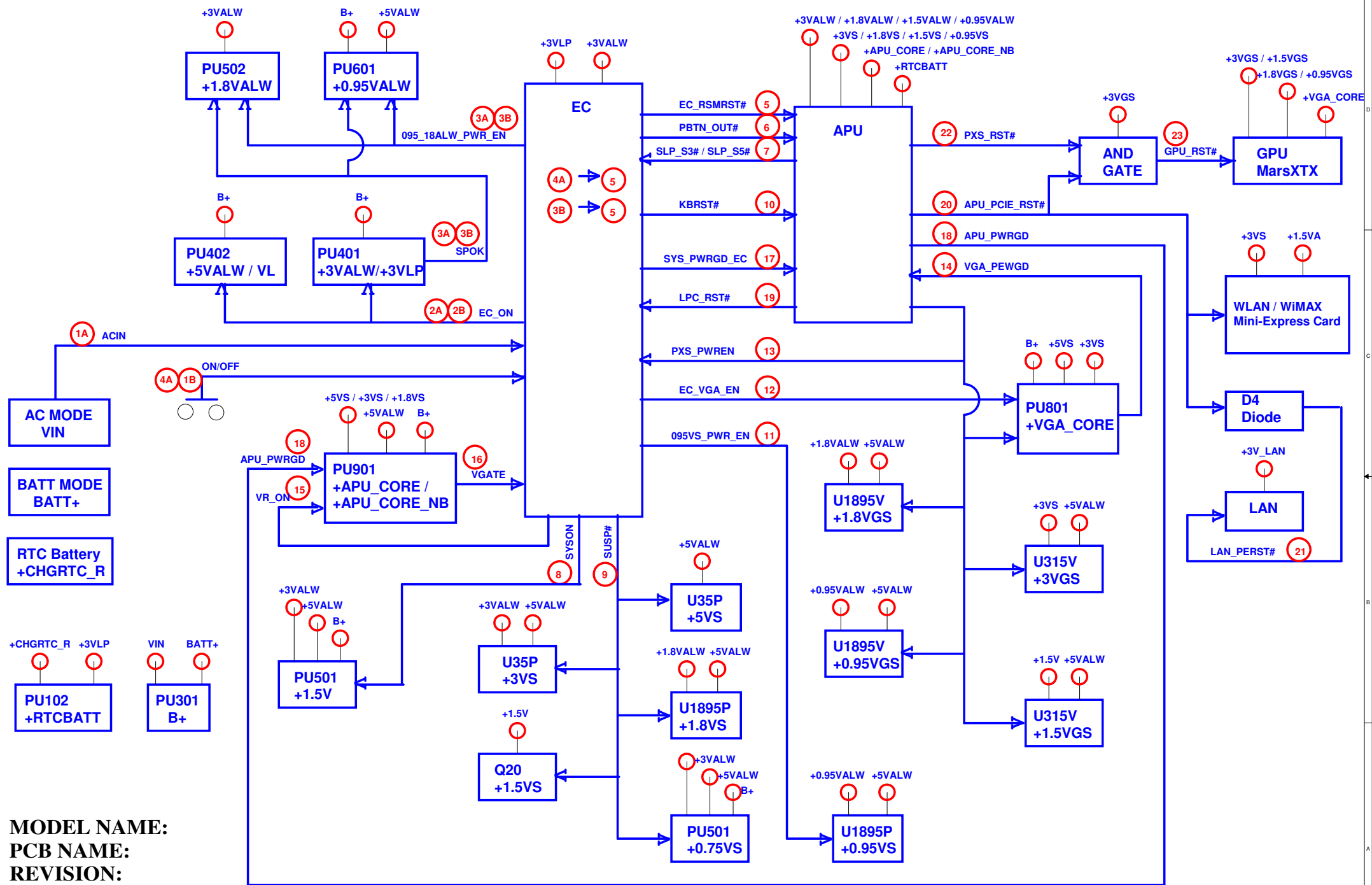
Straps Valid

Global ASIC Reset



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MODEL NAME:  
PCB NAME:  
REVISION:  
DATE: 2011/11/23

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