QCLA4 / QCLA5

Eureka 10FG

LA-8861P REV 0.2 Schematic

Intel Processor (Ivy Bridge) / PCH(Panther Point)
2012-02-09 Rev 0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/11	Deciphered Date	2012/12/31

Title	Cover Page		
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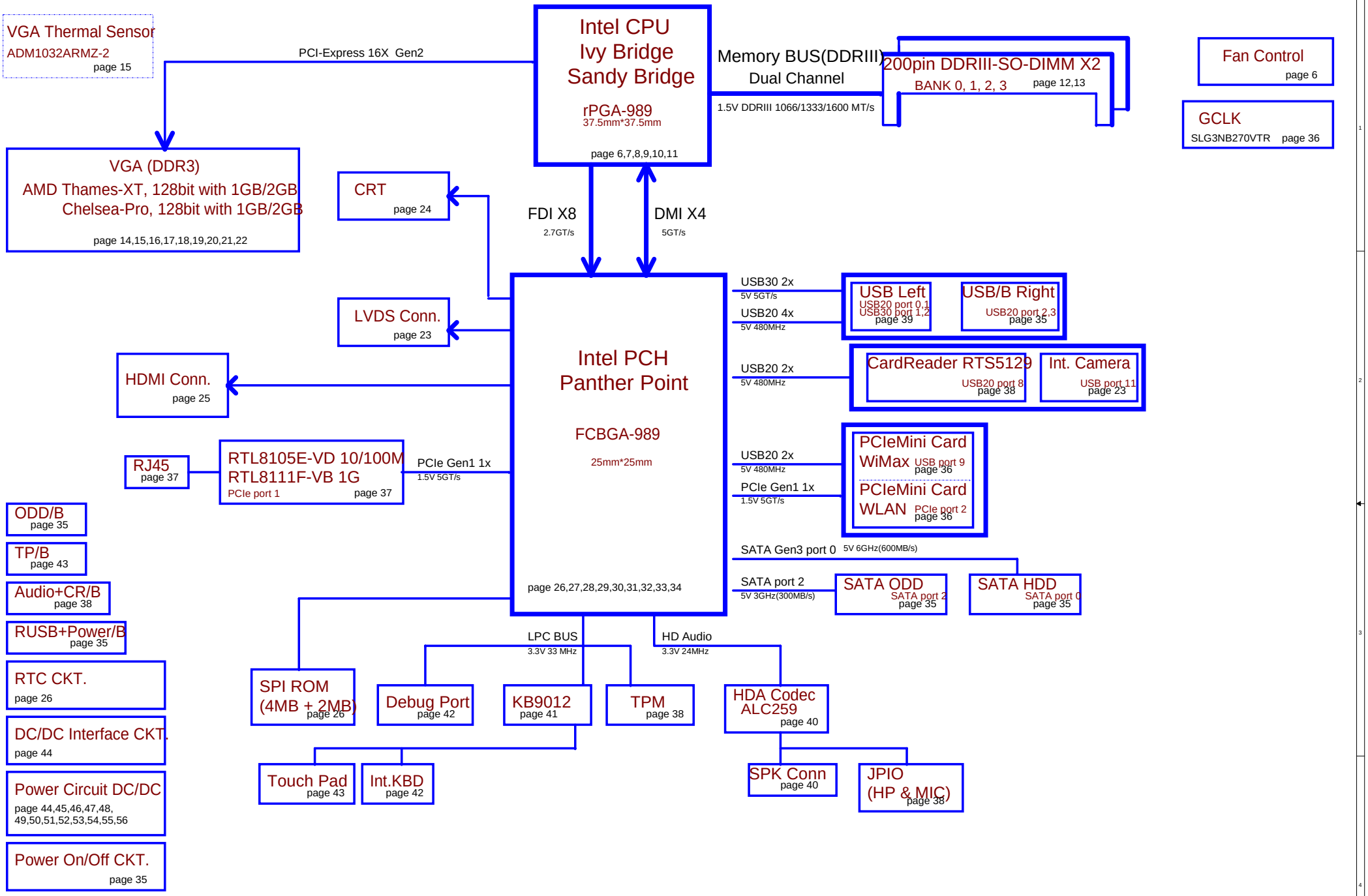

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/11	Deciphered Date 2012/12/31	Title: Block Diagram

Size: D	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
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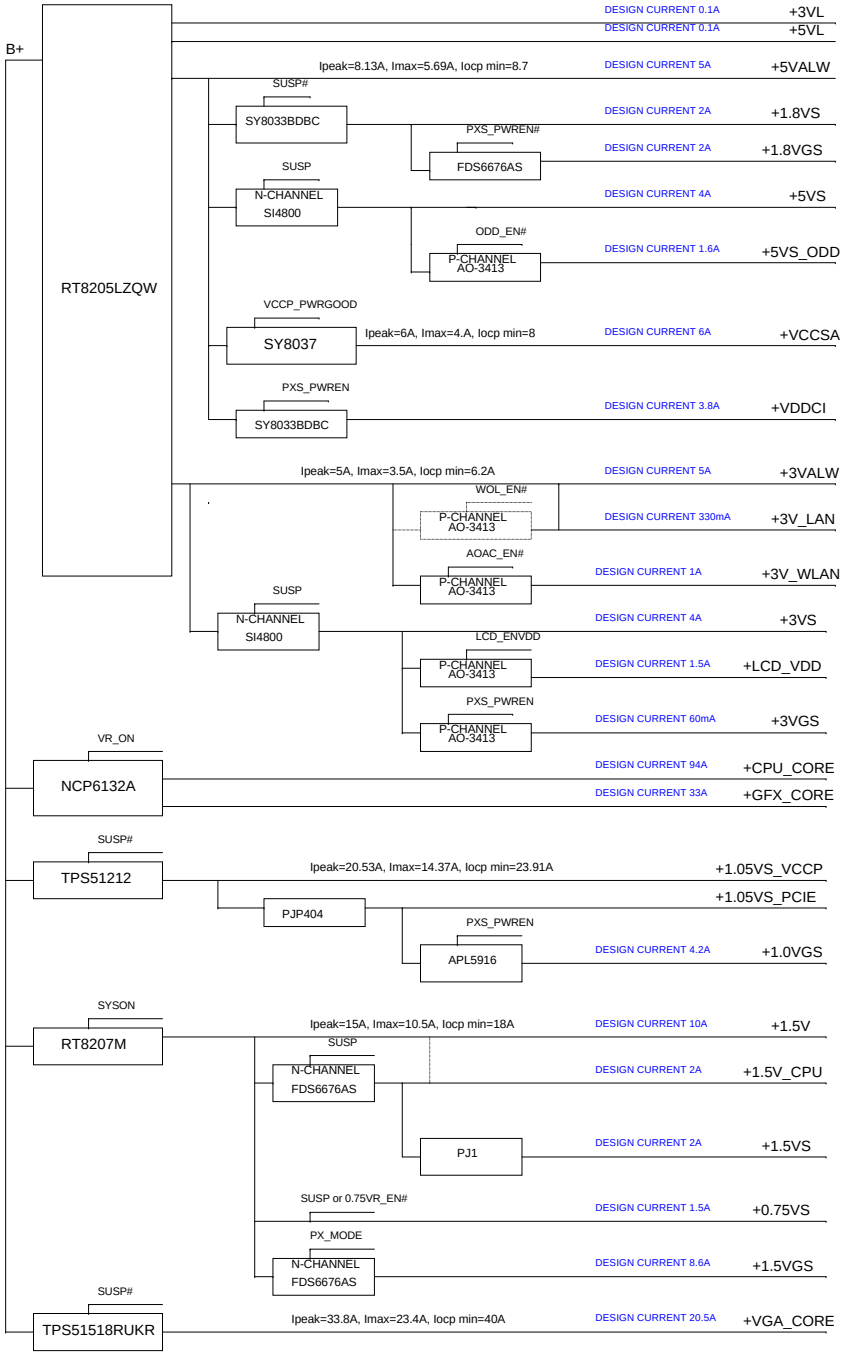

Security Classification	Compal Secret Data		
Issued Date	2011/11/11	Deciphered Date	2012/12/31

Compal Electronics, Inc.		
Title	Power Tree	
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	ATI GPU	82 H	1000 0010 b

Platform	SKU	CPU	PCH	VGA
Chief River		Clarksfield	HM76ES2/HM70C0 (PCHB0@/HM70C0@)	Themes/Chlsea (TH@/CH@)

BTO Option Table

Function	SKU	MIC		LAN		TPM			
description	SKU	MIC		LAN		TPM			
explain	PX4(reserve)	Dig Mic	Analog Mic	10/100M	Giga	9635	9655		
BTO	PX4@	CAM@	AMIC@	8105ELDO@	8111FVB@	TPM9635@	TPM9655@		

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

Function		
description		
explain		
BTO		

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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Power-Up/Down Sequence

All the ASIC supplies, except for VDDR3, must full
nominal voltages within 20 ms of the start of the r
shorter ramp-up duration is preferred. There is no
ramp up of VDDR3 relative to other power rails.

The external pull-up resistors on the DDC/AUX sign
ramp up before or after both VDDC and VDD_CT have r

VDDC and VDD_CT should not ramp up simultaneously.
should reach 90% before VDD_CT starts to ramp up (o

For power down, reversing the ramp-up sequence is

y reach their respective
amp-up sequence, though a
timing requirement on the

als (if applicable) should
amped up.

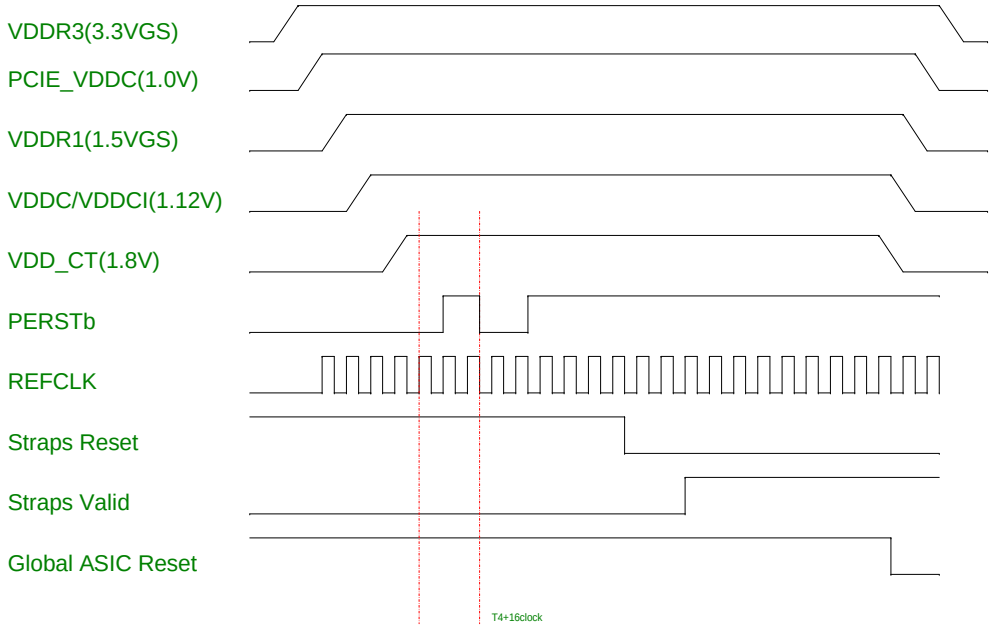
For example, VDDC
r vice versa).

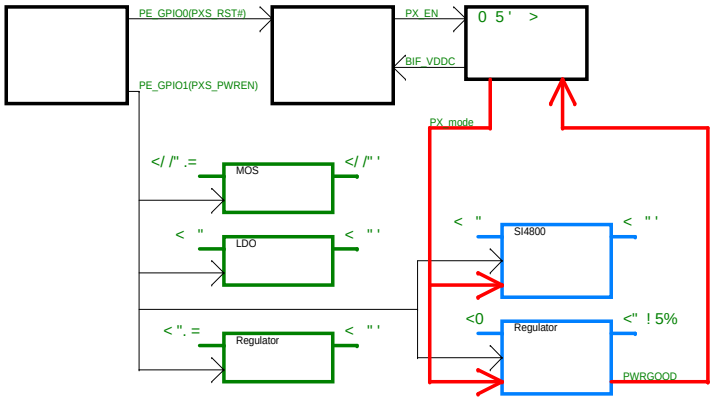
recommended.

! 5 + . ?@ % A B 9> ?@; 8 2
! 5 + . ?@ 5** A B 9> ?@ 5;

! 5 + B 9> ?@; 8 2 1 0 5 6
! 5 + . ?@ 5** A B 9> ?@ 5; 1 8 C B 9>6

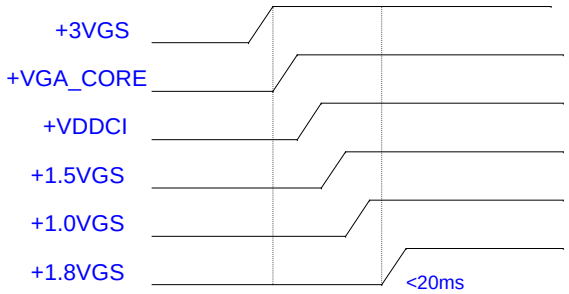
	" 8 9	: /	0 5	
! "##$!"##%$ &"##$ "##%($ "##! &$ # ! "##$ #)*+ ,!"## $ #)#+ ,! "##$ #)#+ ,!"## $ "##$ "## # $ "##-$ "## # $ # ..! "##$ " $ ' "	"	5**	5;	
#)*+ ,!"## $ #)#+ ,!"## $ # ..!"## $ ' "	"	5**	5;	
!"##	"	5**	5;	
"##%/	/ /"	5**	5;	
0 *!"## 1 2 3 4 "$ 0 5 6	' "##	5**	5; !"##	
"##%	"	5**	5**	
"## 7"##	&0#	5**	5**	





Note:
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGS,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Chelsea



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/03/11	Deciphered Date 2012/03/11	Title GPU Notes List
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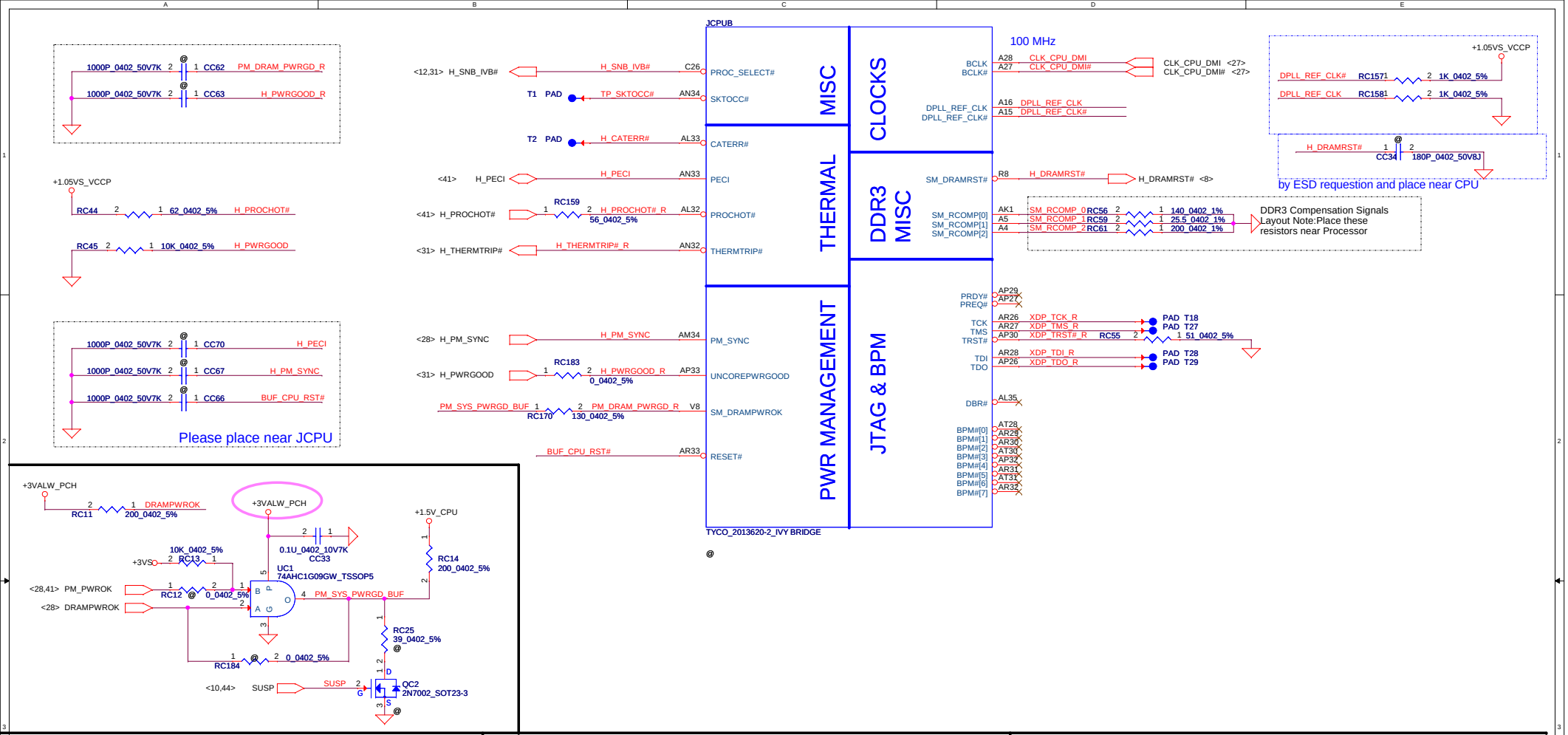
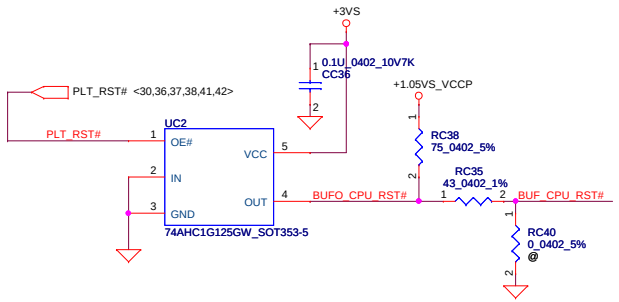
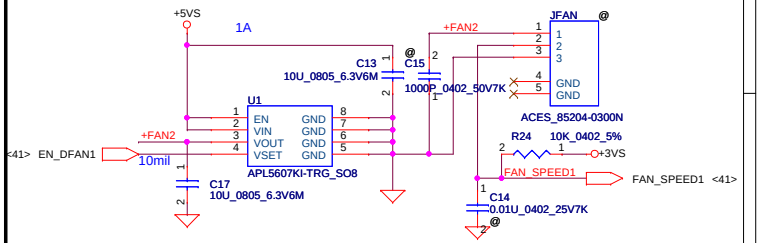


Buffered Rest to CPU



FAN Control Circuit (RPM)



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Issued Date	2011/11/11	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	Ivy Bridge_JTAG/XDP/FAN
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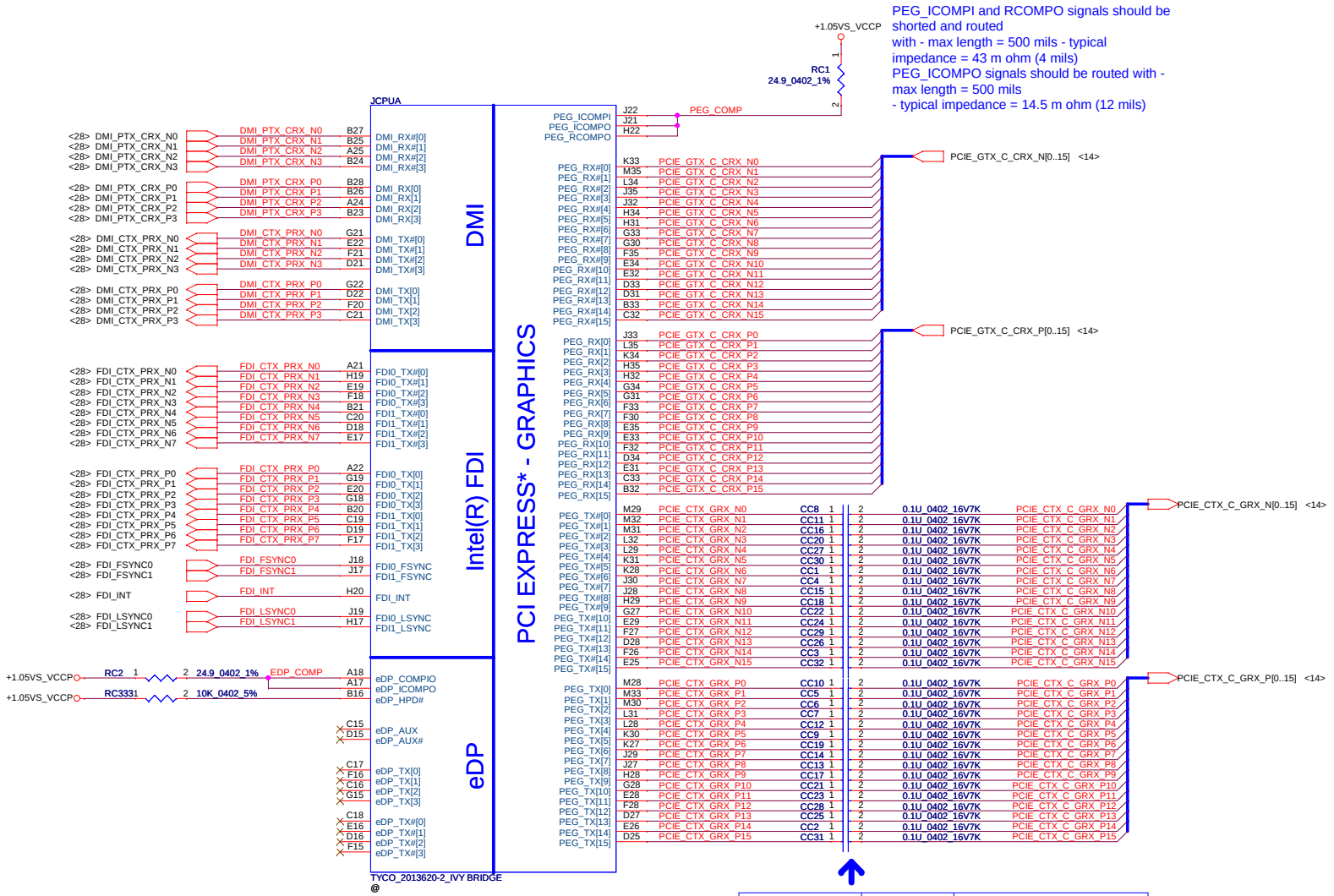

	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	100 nF~220 nF

AMD GPU (Themes & Chlsea) only support up to Gen2

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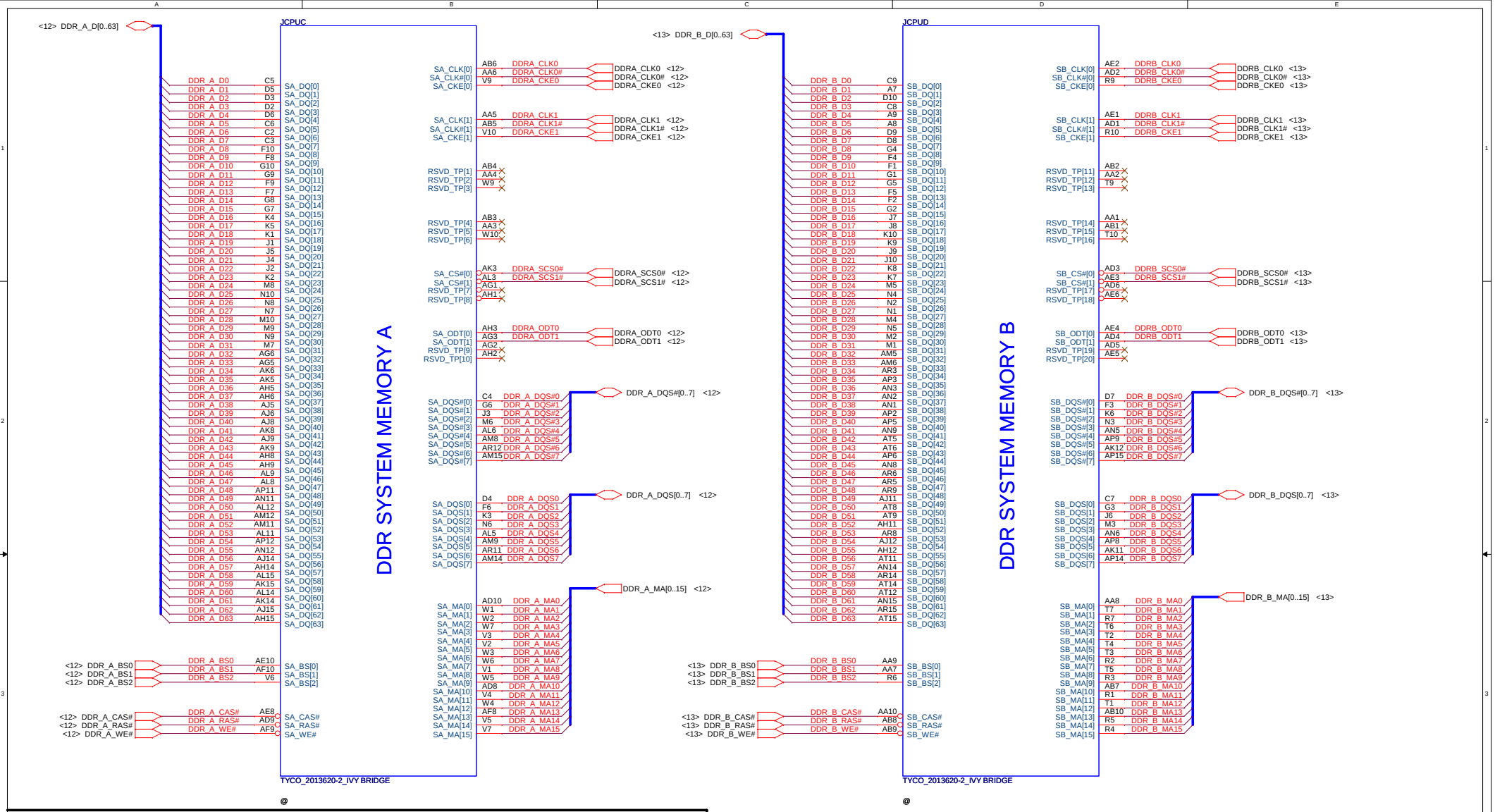

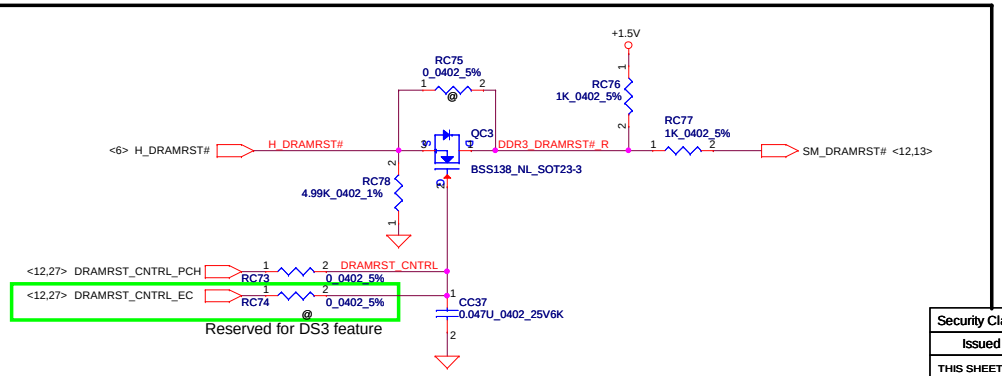

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Compal Electronics, Inc.			
Title	Ivy Bridge_DDR3		
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POWER

+CPU_CORE

+1.05VS_VCCP

JCPUF

97A

8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

AG35	VCC1	
AG34	VCC2	
AG33	VCC3	
AG32	VCC4	
AG31	VCC5	
AG30	VCC6	
AG29	VCC7	
AG28	VCC8	
AG27	VCC9	
AG26	VCC10	
AF35	VCC11	
AF34	VCC12	
AF33	VCC13	
AF32	VCC14	
AF31	VCC15	
AF30	VCC16	
AF29	VCC17	
AF28	VCC18	
AF27	VCC19	
AF26	VCC20	
AD35	VCC21	
AD34	VCC22	
AD33	VCC23	
AD32	VCC24	
AD31	VCC25	
AD30	VCC26	
AD29	VCC27	
AD28	VCC28	
AD27	VCC29	
AD26	VCC30	
AC35	VCC31	
AC34	VCC32	
AC33	VCC33	
AC32	VCC34	
AC31	VCC35	
AC30	VCC36	
AC29	VCC37	
AC28	VCC38	
AC27	VCC39	
AC26	VCC40	
AA35	VCC41	
AA34	VCC42	
AA33	VCC43	
AA32	VCC44	
AA31	VCC45	
AA30	VCC46	
AA29	VCC47	
AA28	VCC48	
AA27	VCC49	
AA26	VCC50	
Y35	VCC51	
Y34	VCC52	
Y33	VCC53	
Y32	VCC54	
Y31	VCC55	
Y30	VCC56	
Y29	VCC57	
Y28	VCC58	
Y27	VCC59	
Y26	VCC60	
V35	VCC61	
V34	VCC62	
V33	VCC63	
V32	VCC64	
V31	VCC65	
V30	VCC66	
V29	VCC67	
V28	VCC68	
V27	VCC69	
V26	VCC70	
U35	VCC71	
U34	VCC72	
U33	VCC73	
U32	VCC74	
U31	VCC75	
U30	VCC76	
U29	VCC77	
U28	VCC78	
U27	VCC79	
U26	VCC80	
R35	VCC81	
R34	VCC82	
R33	VCC83	
R32	VCC84	
R31	VCC85	
R30	VCC86	
R29	VCC87	
R28	VCC88	
R27	VCC89	
R26	VCC90	
P35	VCC91	
P34	VCC92	
P33	VCC93	
P32	VCC94	
P31	VCC95	
P30	VCC96	
P29	VCC97	
P28	VCC98	
P27	VCC99	
P26	VCC100	

AH13	VCCIO1	
AH10	VCCIO2	
AG10	VCCIO3	
AC10	VCCIO4	
Y10	VCCIO5	
U10	VCCIO6	
P10	VCCIO7	
L10	VCCIO8	
J14	VCCIO9	
J13	VCCIO10	
J12	VCCIO11	
J11	VCCIO12	
H14	VCCIO13	
H12	VCCIO14	
H11	VCCIO15	
G14	VCCIO16	
G13	VCCIO17	
G12	VCCIO18	
F14	VCCIO19	
F13	VCCIO20	
F12	VCCIO21	
F11	VCCIO22	
E14	VCCIO23	
E12	VCCIO24	
E11	VCCIO25	
D14	VCCIO26	
D13	VCCIO27	
D12	VCCIO28	
D11	VCCIO29	
C14	VCCIO30	
C13	VCCIO31	
C12	VCCIO32	
C11	VCCIO33	
B14	VCCIO34	
B12	VCCIO35	
A14	VCCIO36	
A13	VCCIO37	
A12	VCCIO38	
A11	VCCIO39	
J23	VCCIO40	

Reserve 0.1u to avoid noise

+1.05VS_VCCP

0.1U_0402_10V7K

CC50 @

RC91 130_0402_5%

+1.05VS_VCCP

0.1U_0402_10V7K

CC49 @

RC89 75_0402_5%

VIDALERT# AJ29 H_CPU_SVIDALRT#

VIDSCLK AJ30 H_CPU_SVIDCLK

VIDSOUT AJ28 H_CPU_SVIDDAT

RC90 43_0402_1%

RC88 0_0402_5%

RC92 0_0402_5%

VR_SVID_ALRT# <52>

VR_SVID_CLK <52>

VR_SVID_DAT <52>

Pull high resistor on VR side

+CPU_CORE

RC93 100_0402_1%

Close to CPU

VCC_SENSE AJ35 VCCSENSE_R

VSS_SENSE AJ34 VSSSENSE_R

RC94 0_0402_5%

RC95 0_0402_5%

VCCSENSE <52>

VSSSENSE <52>

VCCIO_SENSE B10 VCCIO_SENSE

VSS_SENSE_VCCIO A10

VCCIO_SENSE <49>

RC97 100_0402_1%

RC96 10_0402_1%

RC98 10_0402_1%

+1.05VS_VCCP

Close to CPU

TYCO_2013620-2_IVY BRIDGE

@

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Compal Electronics, Inc.

Title: Ivy Bridge_POWER-1

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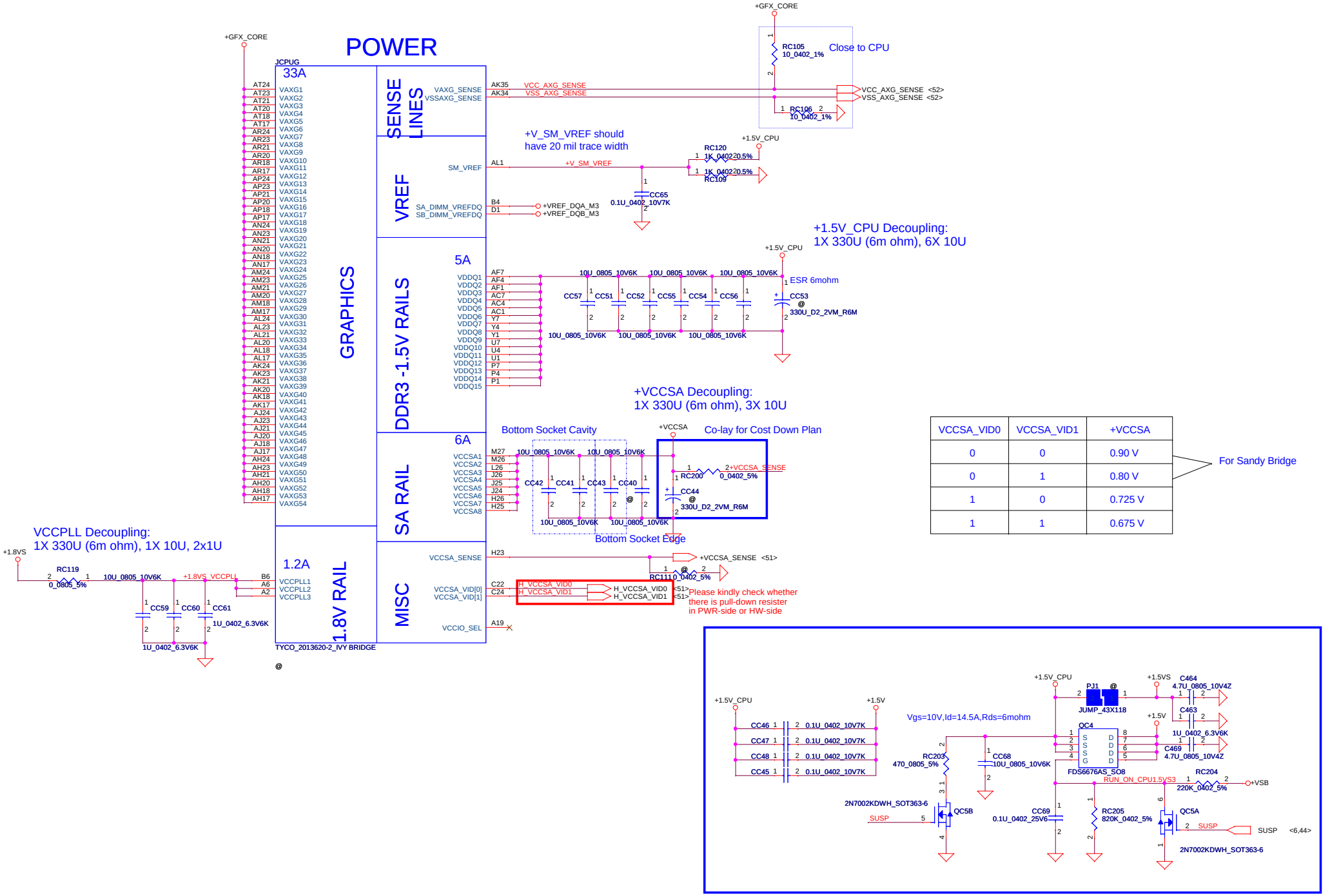
POWER



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	Ivy Bridge_POWER-2
Size: Custom	Document Number: QCLA4 LA-8861P M/B
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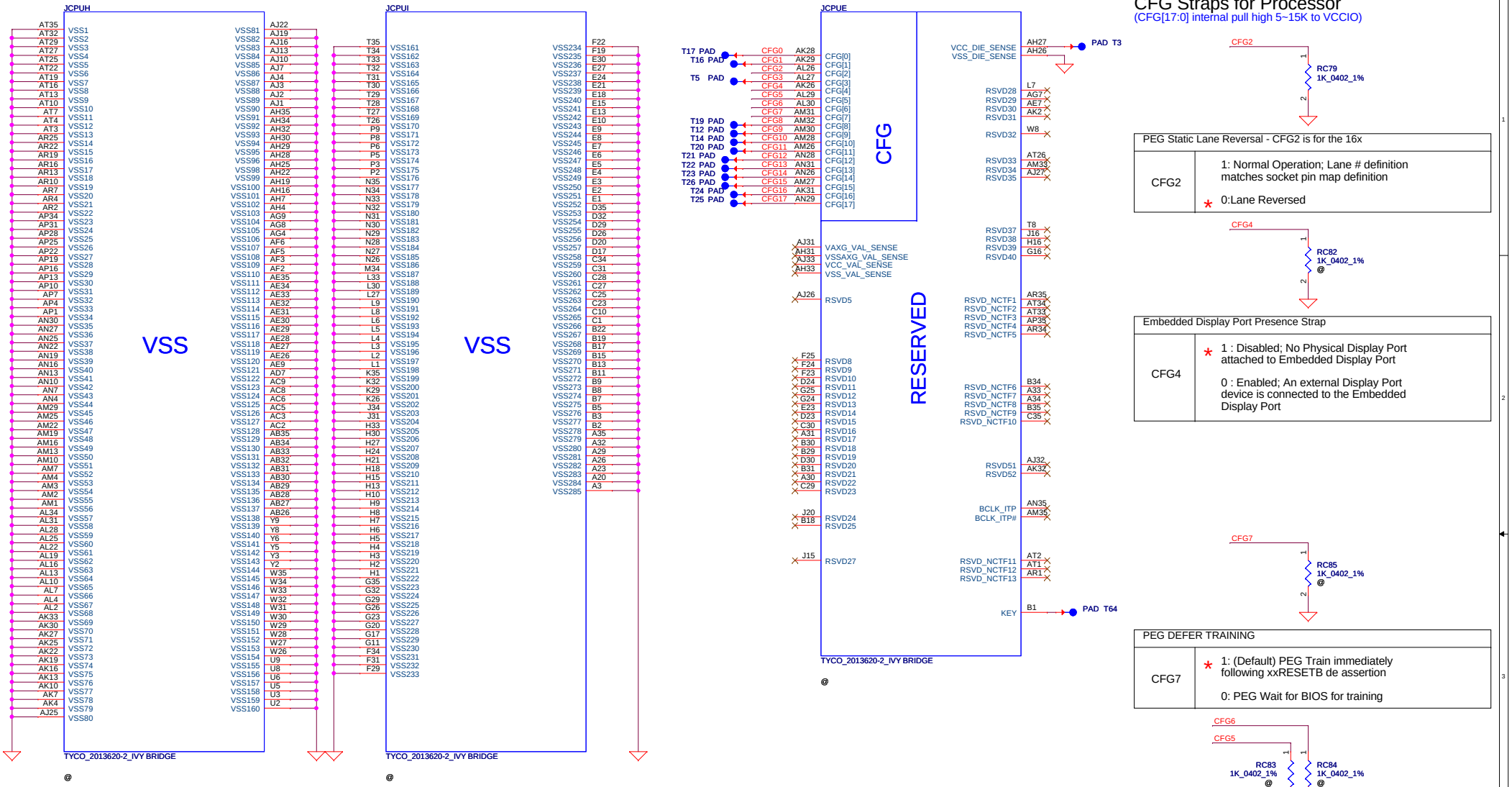

CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)

CFG2 — RC79 1K_0402_1%

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG4 — RC82 1K_0402_1% @

Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 — RC85 1K_0402_1% @

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG6 — RC83 1K_0402_1% @

CFG5 — RC84 1K_0402_1% @

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Compal Electronics, Inc.

Title: Ivy Bridge_GND/RSVD/CFG

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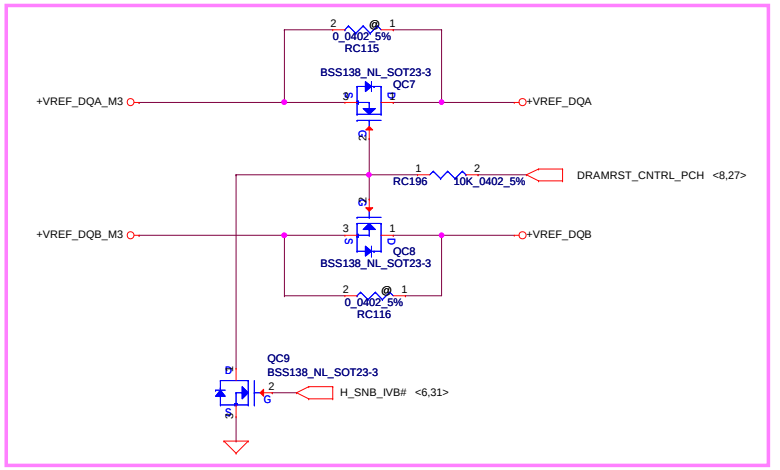
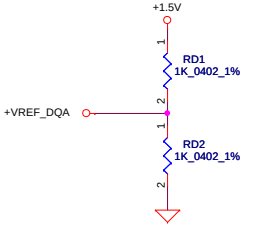
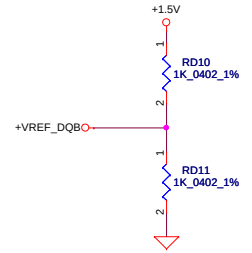
DDR3 SO-DIMM A
Reverse Type

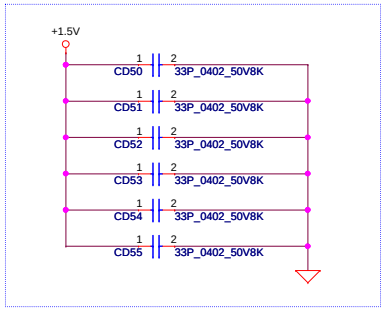
DDR_A_DQS[0..7] <8>
DDR_A_DQS#[0..7] <8>
DDR_A_D[0..63] <8>
DDR_A_MA[0..15] <8>

Intel DDR Vref M3

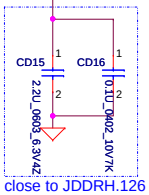




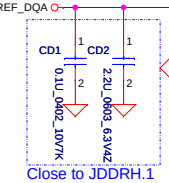




please place these caps near the reference power plane of CMD/AD



close to JDDRH.126

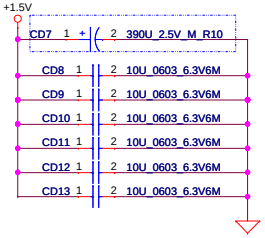


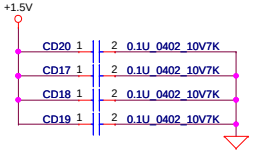
Close to JDDRH.1

Swap DIMMA to DDR3H
(for layout concern)

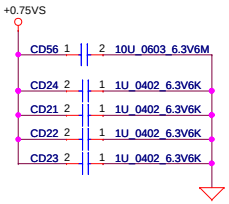
Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA





Layout Note:
Place near JDDRH.203 and 204



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Compal Electronics, Inc.

Title: DDRIII-SODIMM0

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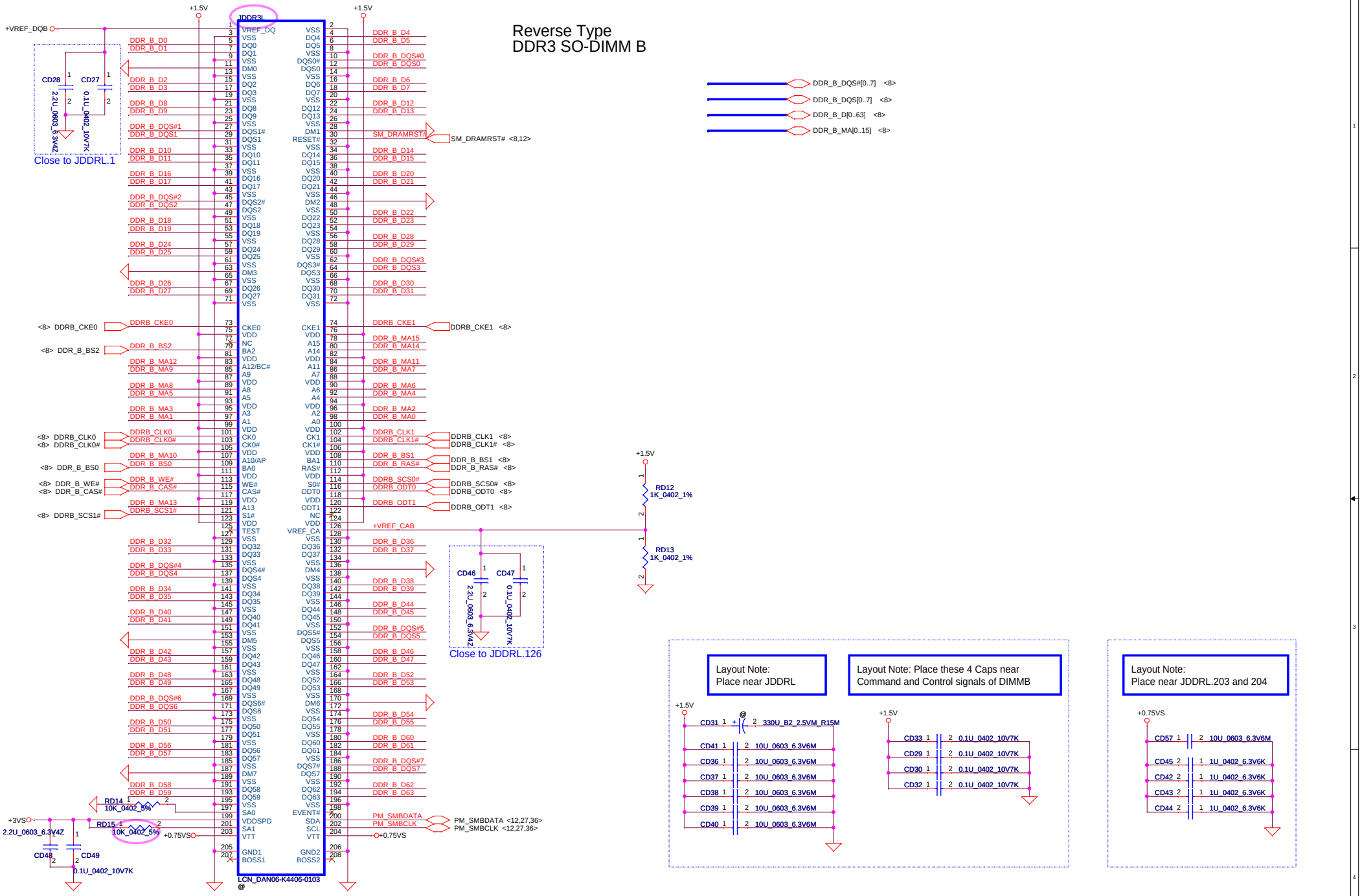

Swap DIMMB to DDR3L
(for layout concern)

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Compal Electronics, Inc.

Title: DDRIII-SODIMM1

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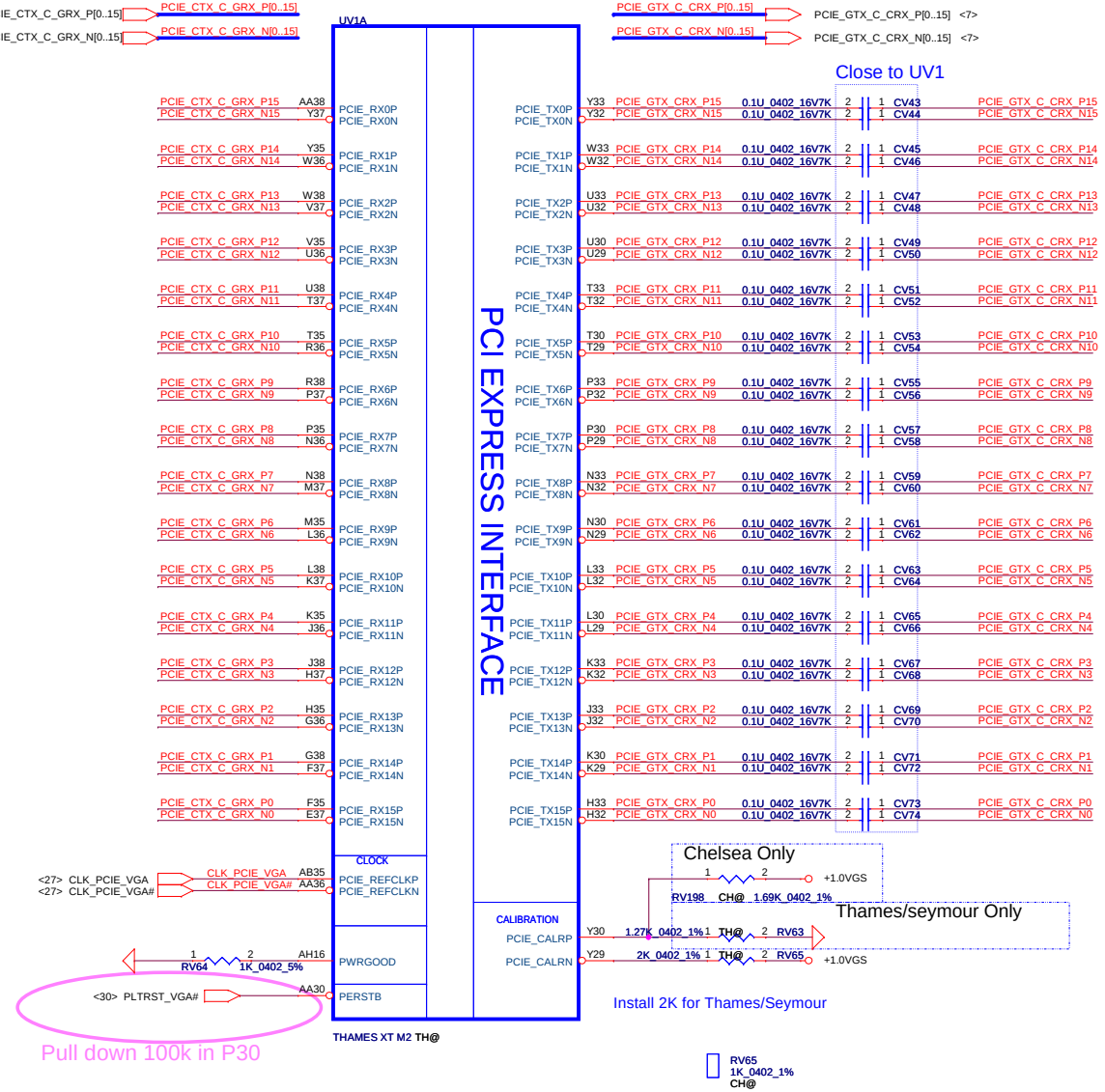
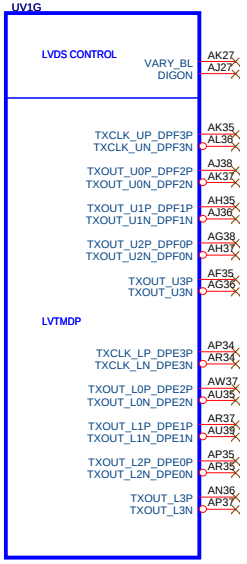
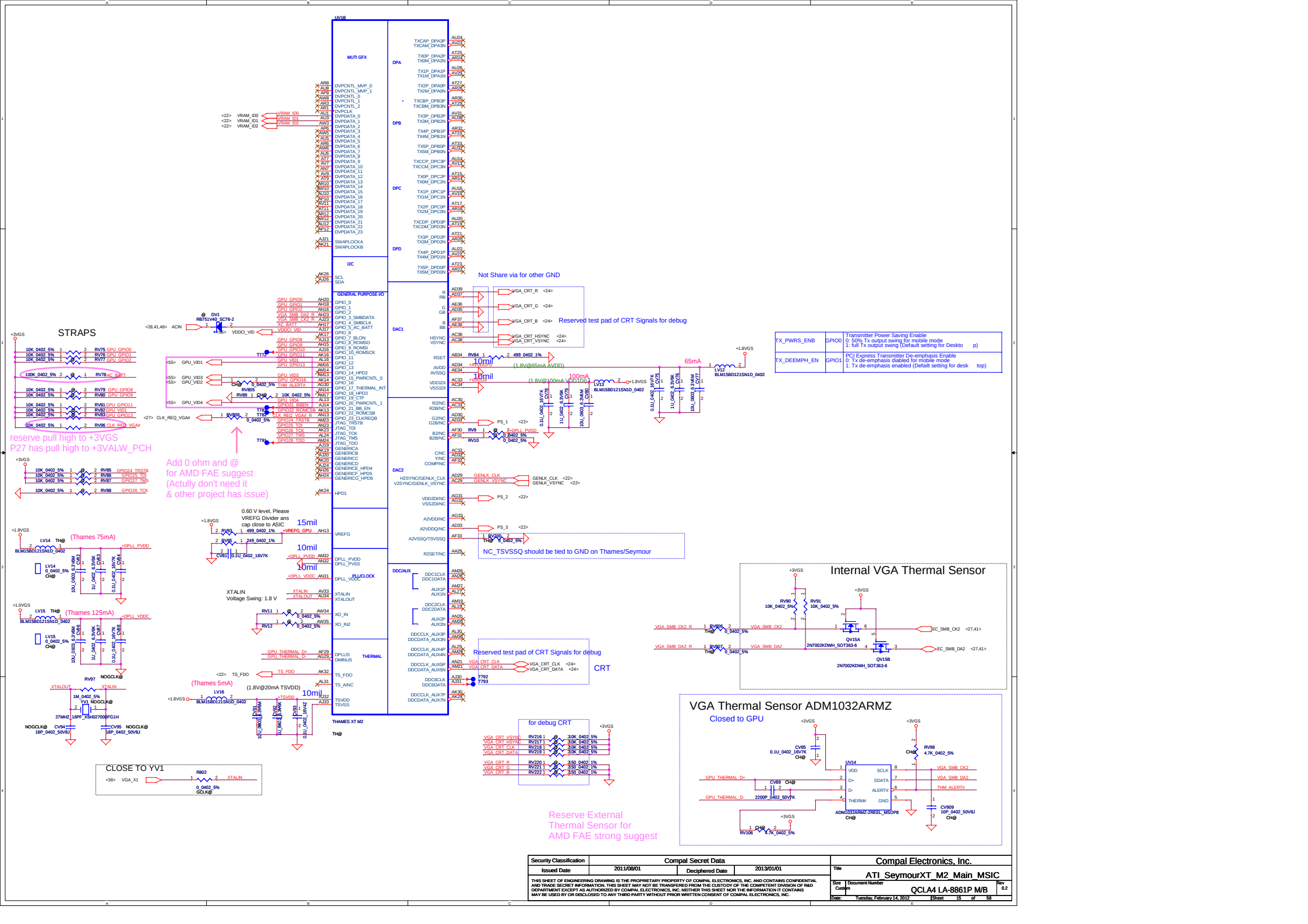
GFX PCIE LANE REVERSAL



LVDS Interface



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/01	Deciphered Date	2013/01/01
Title	ATI_SeymourXT_M2_PCIE/LVDS		
Size: Custom	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 14 of 58		



TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Deskto p)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desk top)

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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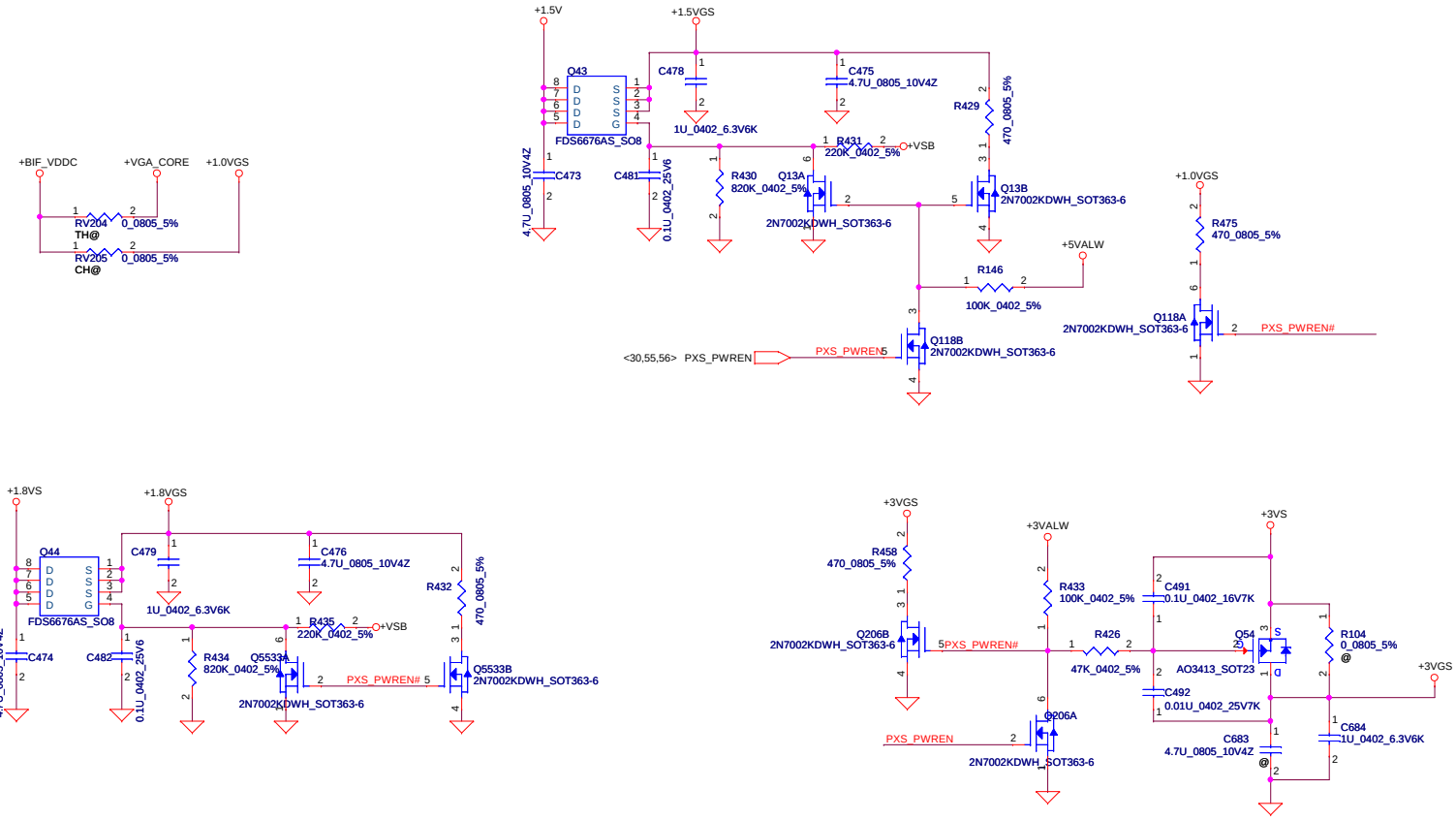
Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

Size: Custom | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 15 of 58



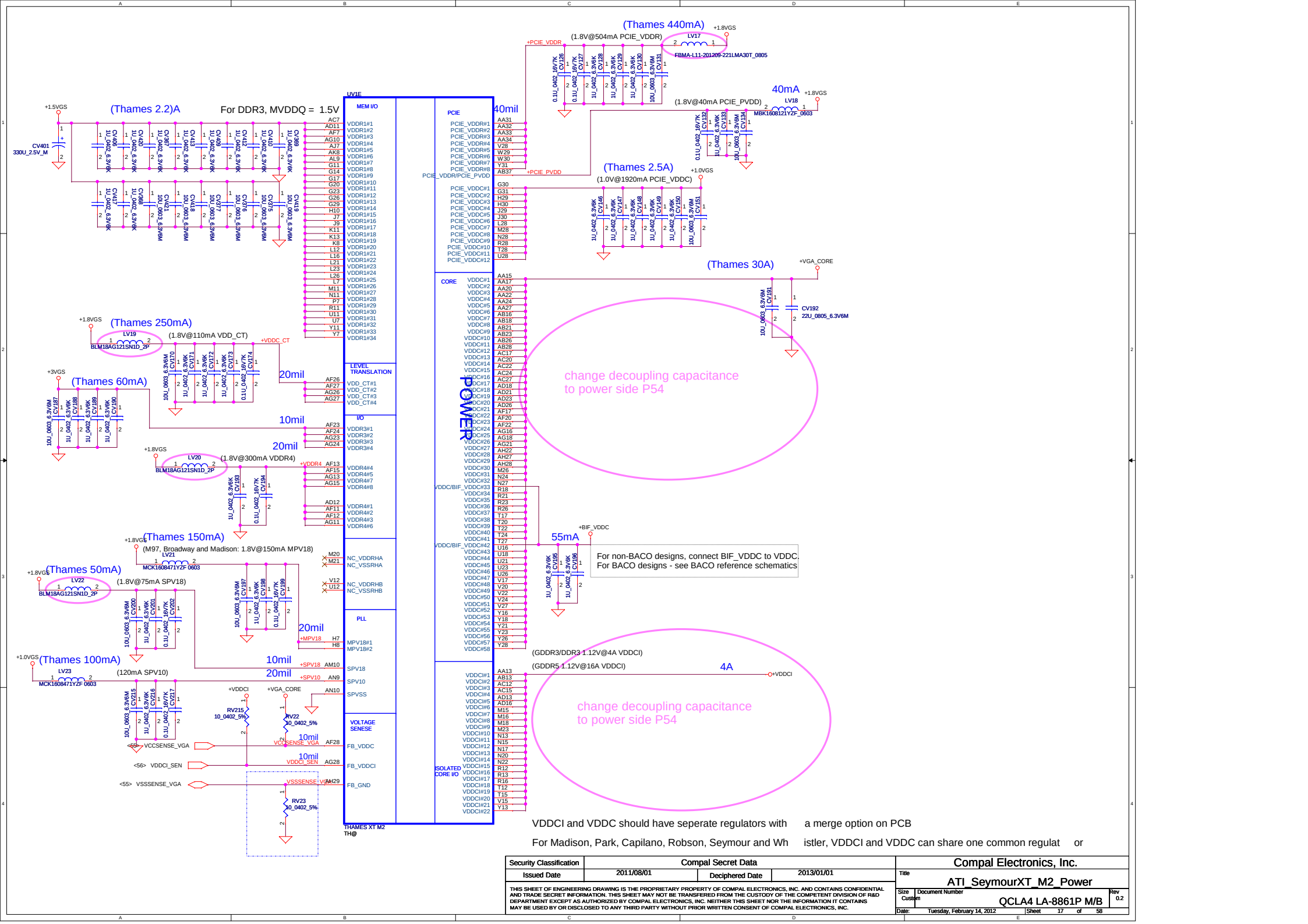
Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_BACO POWER

Size	Document Number	Rev
Custom	QCLA4 LA-8861P M/B	0.2

Date: Tuesday, February 14, 2012 Sheet 16 of 58



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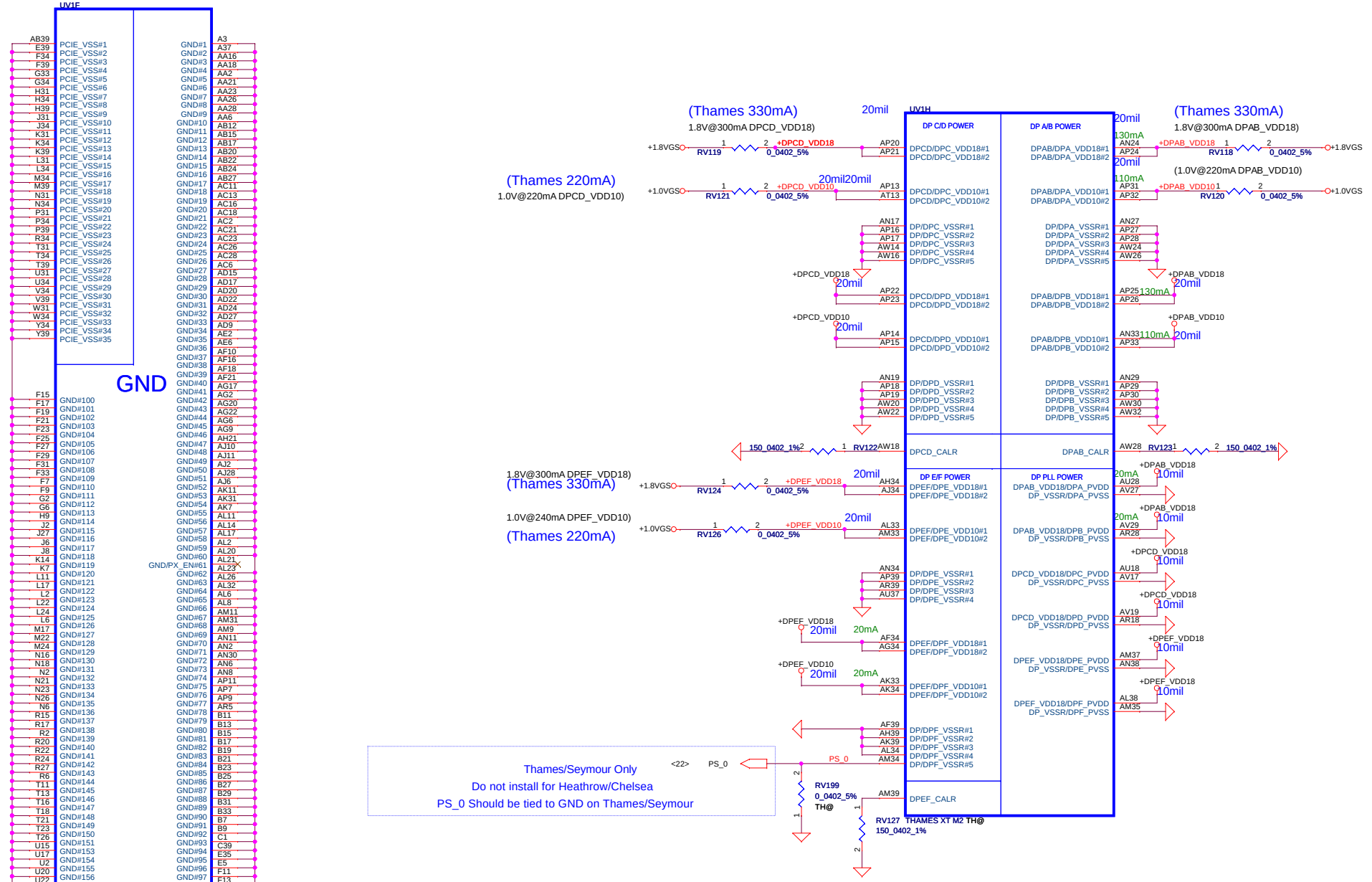
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
Custom	QCLA4 LA-8861P M/B	0.2

Date: Tuesday, February 14, 2012 Sheet 17 of 58



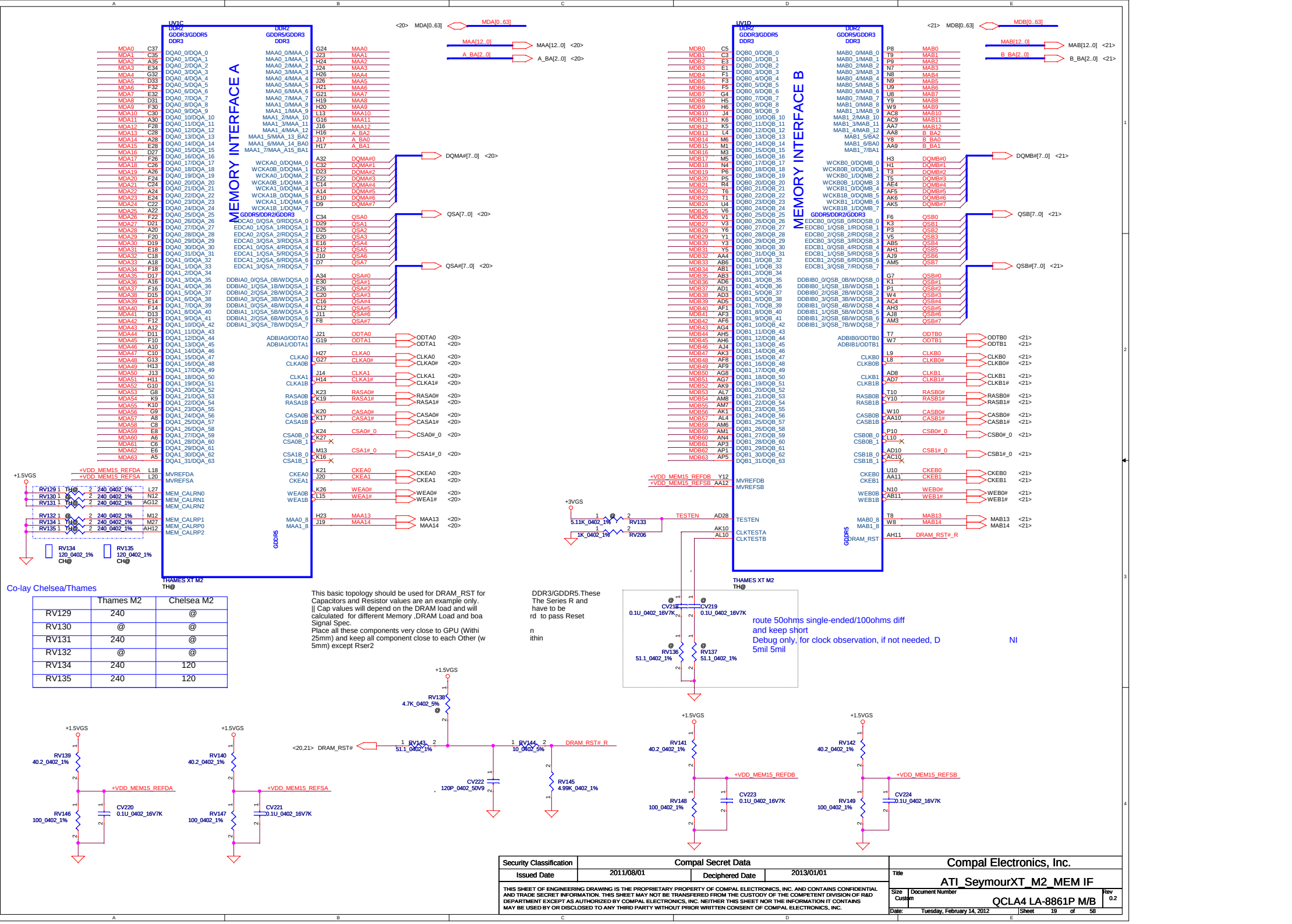
Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size: Custom | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 18 of 58



Co-lay Chelsea/Thames

	Thames M2	Chelsea M2
RV129	240	@
RV130	@	@
RV131	240	@
RV132	@	@
RV134	240	120
RV135	240	120

This basic topology should be used for DRAM_RST for Capacitors and Resistor values are an example only. || Cap values will depend on the DRAM load and will calculated for different Memory ,DRAM Load and boa Signal Spec.
Place all these components very close to GPU (Withi 25mm) and keep all component close to each Other (w 5mm) except Rser2

DDR3/GDDR5.These
The Series R and
have to be
rd to pass Reset

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
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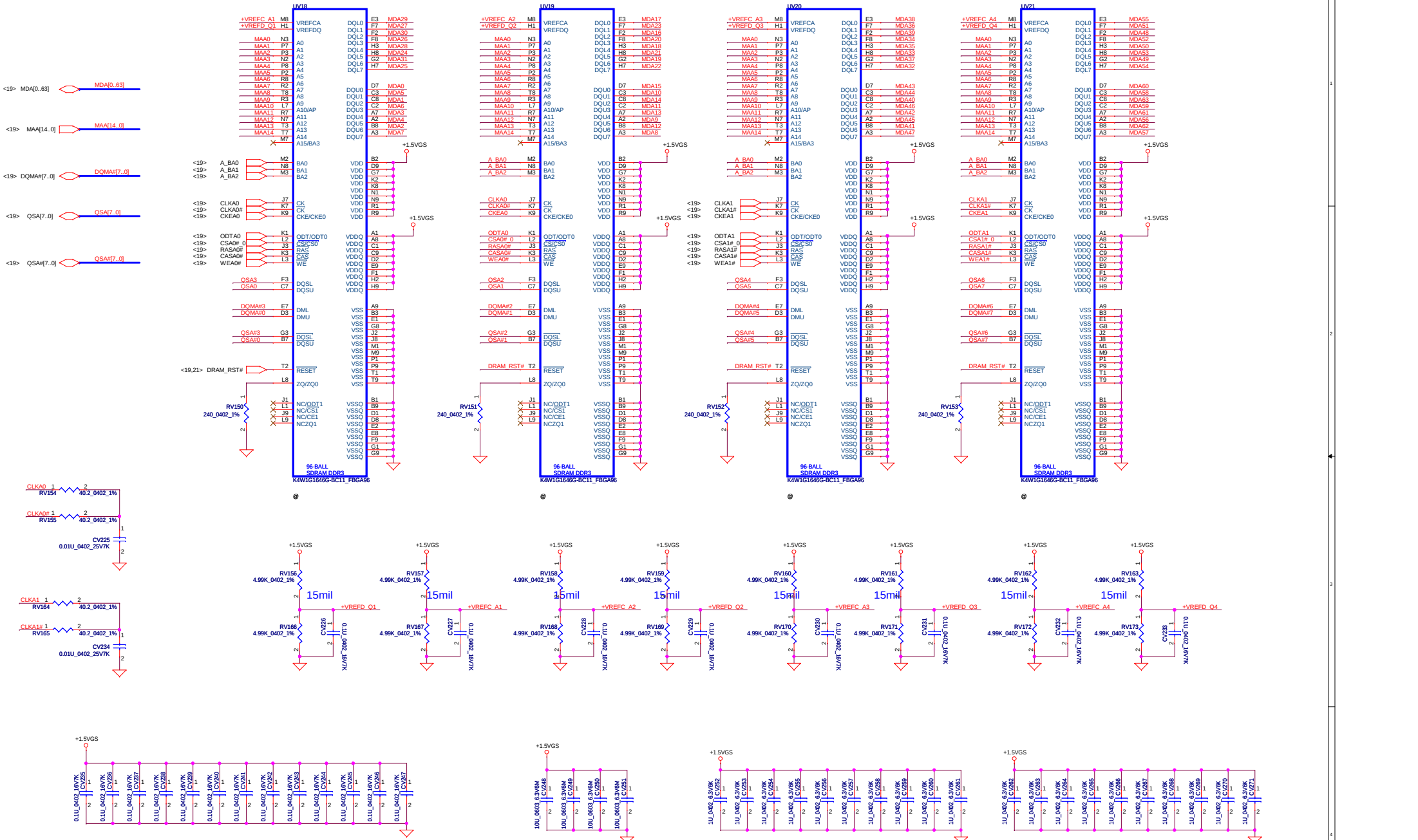
CHANNEL A: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
C	QCLA4 LA-8861P M/B	0.2

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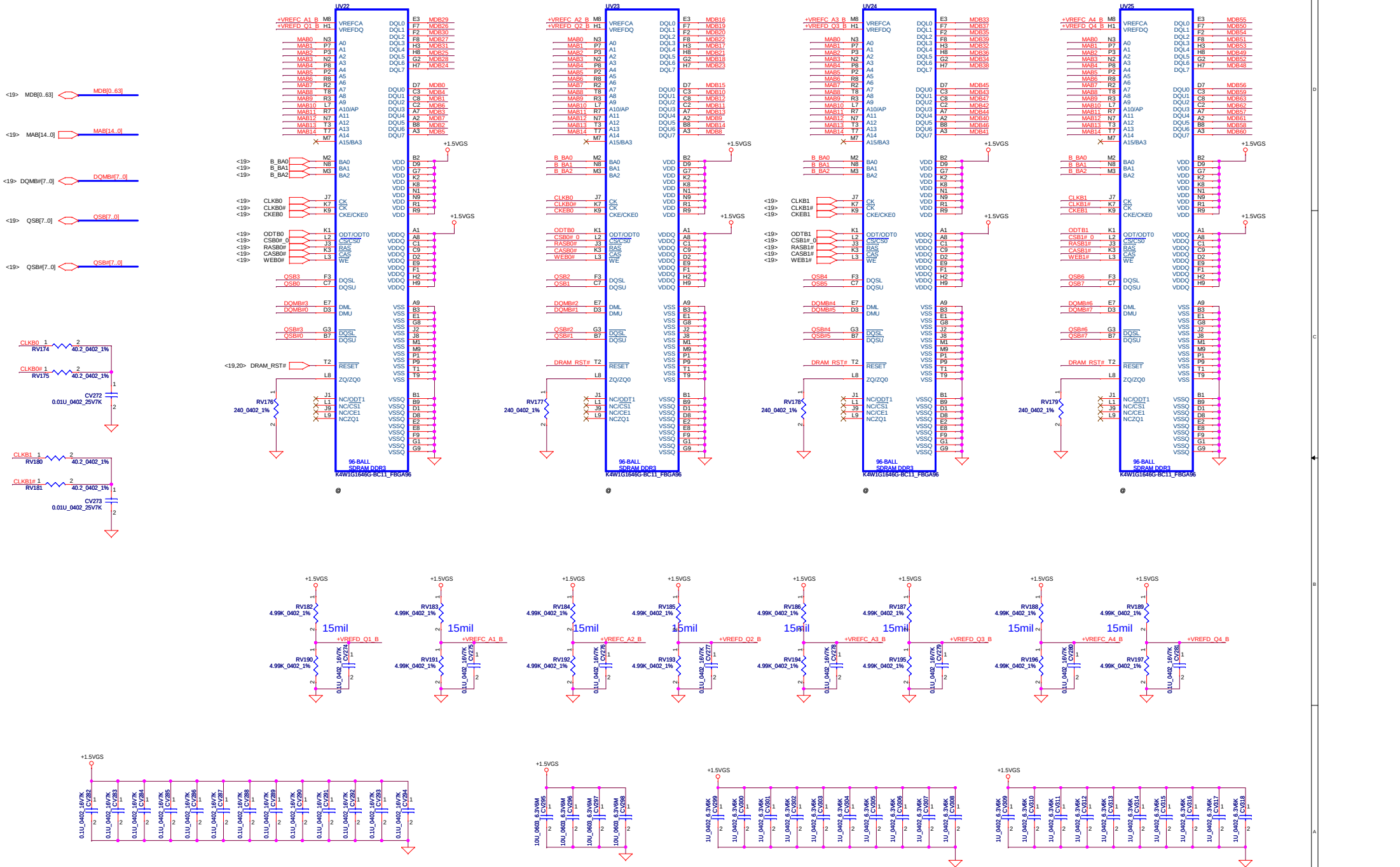
CHANNEL B: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

Size	Document Number	Rev
C	QCLA4 LA-8861P M/B	0.2

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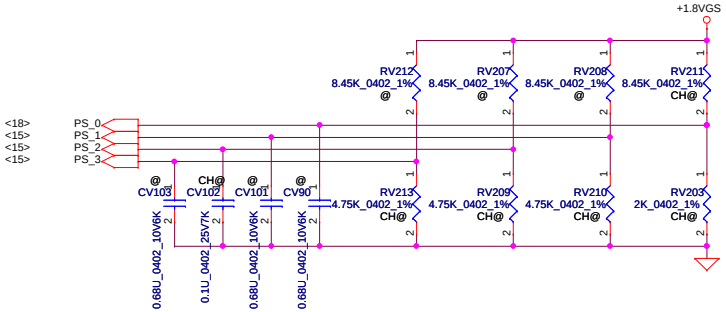
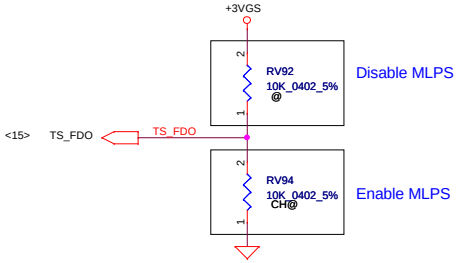


	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45k	2k
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75k
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75k
PS_3[5:1]	1 1	0 0 0	NC	NC	4.75k



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select 256MB: 0 0 1	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsea PRO)	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO2	PCIE Gen3 capability 0: 2.5GT/s 1: 5GT/s	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO8	PCIE clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsea PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIE full TX output swing 0: Half swing 1: Full swing	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIE transmitter de-emphsis enable 0: Disable 1: Enable	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM 0: Disable 1: Enable	0
PS_2[4]	VGA DIS	GPIO9	VGA disable 0: Enable 1: Disable	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
AUD[1] AUD[0]	HSYNC VSYNC		AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0

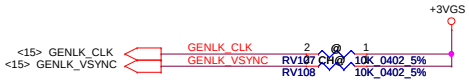
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT I NSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP " LOW" AND NOT CONFLICT DURING RESET

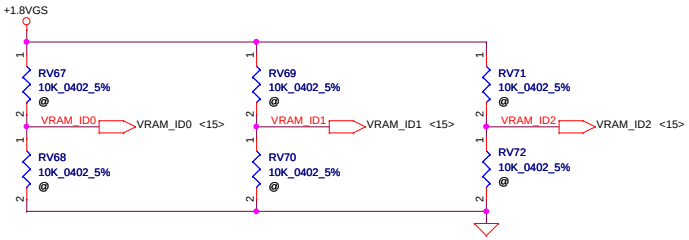
GPIO21 H2SYNC GENERICC GPIO2 GPIO8

VRAM Straps

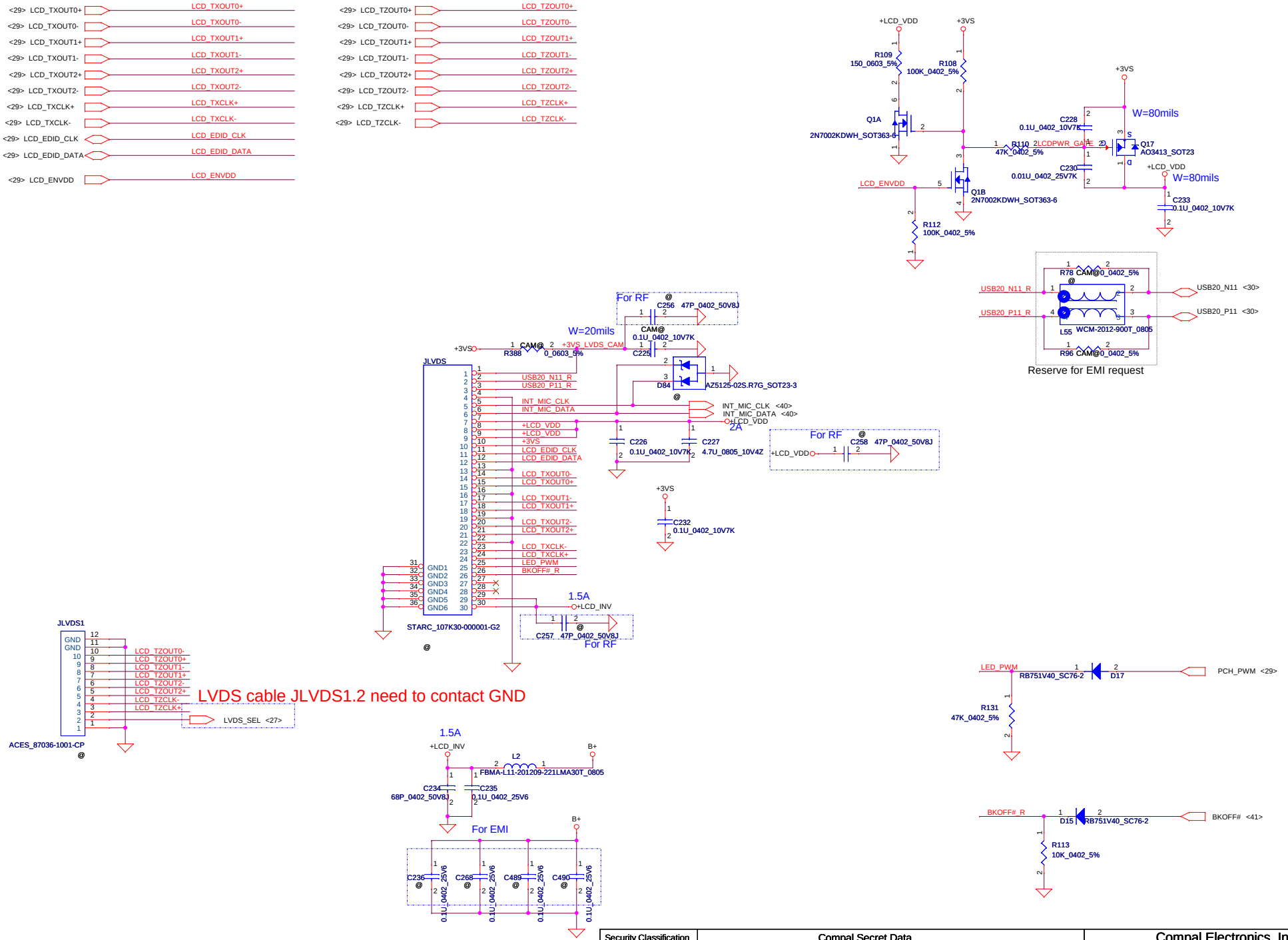
	!	"#$%	"#$%	"#$%	
64MX16 (1G)	H5TQ1G63DFR-11C	0	0	1	
64MX16 (1G)	K4W1G1646G-BC11	1	0	1	
* 128M16 (2G)	H5TQ2G63BFR-11C	0	1	1	
* 128M16 (2G)	K4W2G1646C-HC11	1	1	1	



Modify VRAM Straps different from AMD platform (Because BIOS team want to Common VBIOS, Seperate VRAM Straps could be easily control VRAM if AMD & Intel have different VRAM turning setting)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/11	Deciphered Date 2012/12/31	Title ATI_STRAP PINS
			Size Custom / Document Number / Rev
			Date: Tuesday, February 14, 2012 Sheet 22 of 58



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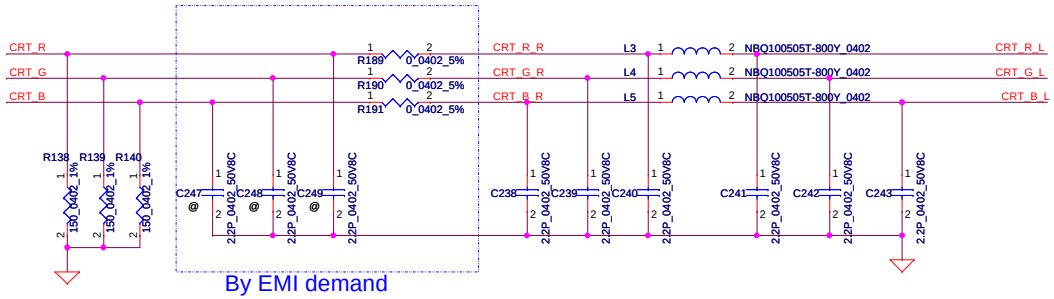
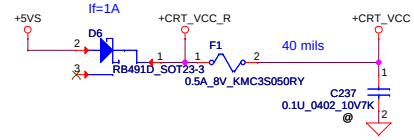
Issued Date	2011/11/11	Deciphered Date 2012/12/31	Title: LVDS

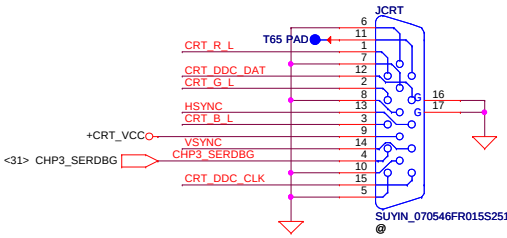
Size: B/26 Custom	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 23 of 58		

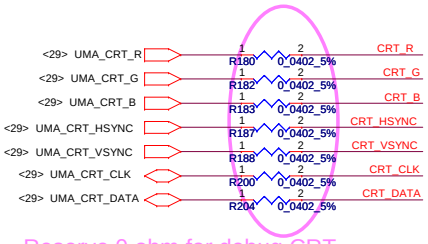
CRT CONNECTOR



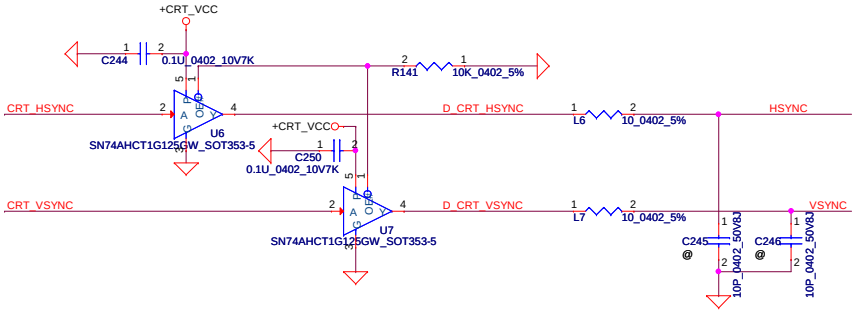
By EMI demand

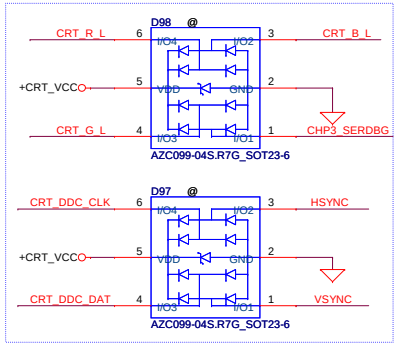






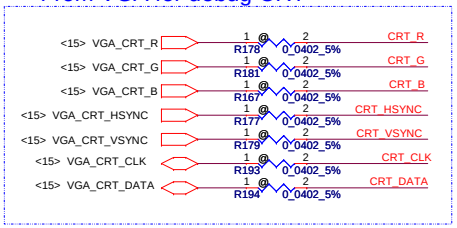
Reserve 0 ohm for debug CRT

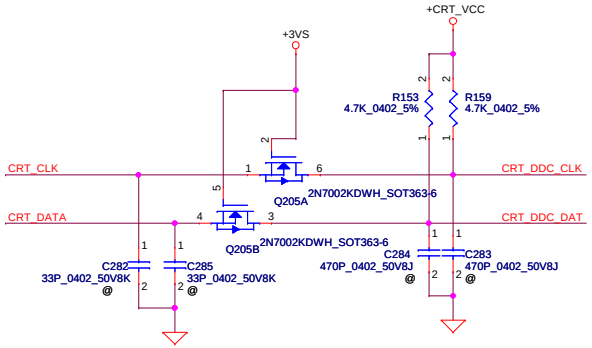




2/9: Add for ESD request

From VGA for debug CRT





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Issued Date	2011/11/11	Deciphered Date 2012/12/31	Title: CRT

Size: D26	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
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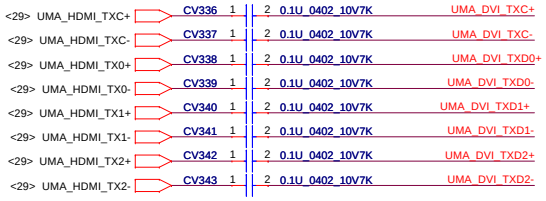
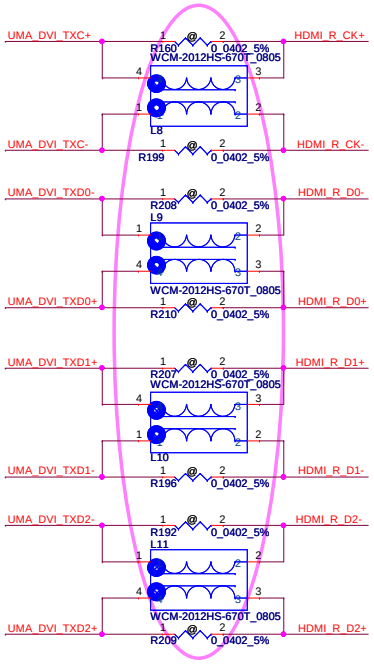
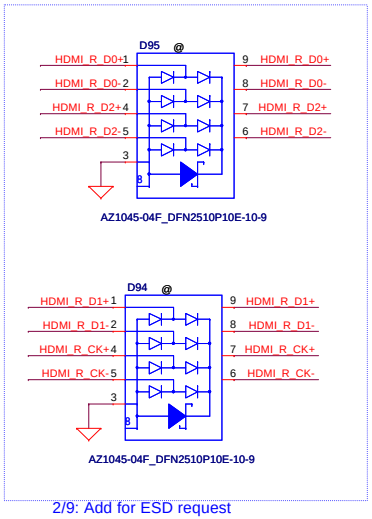
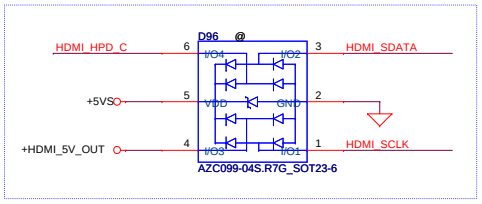




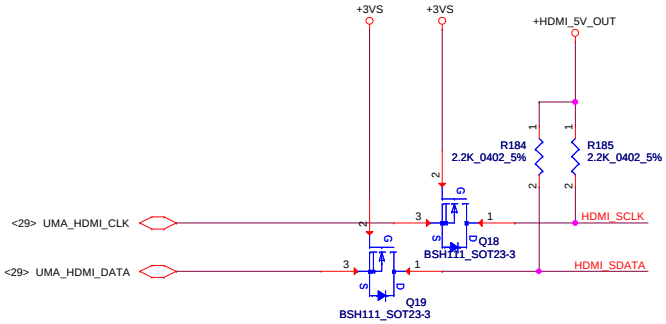
change to 67ohm

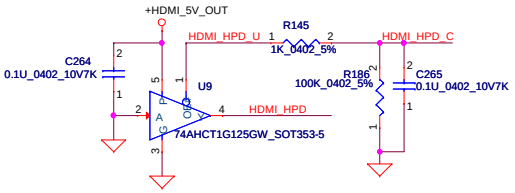


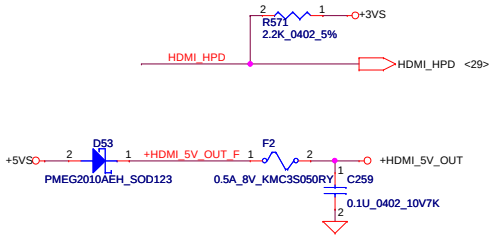
2/9: Add for ESD request

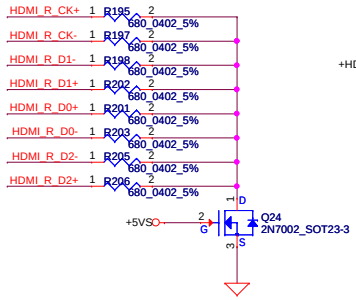


2/9: Add for ESD request

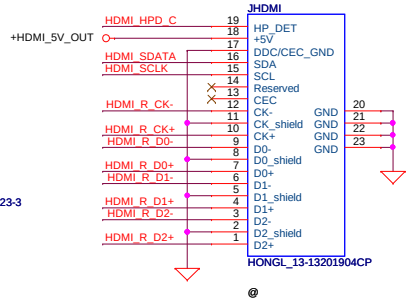








HDMI Connector



@

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CMOS Setting, near DDR Door

iME Setting.

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

PCH_SPKR
High = Enabled "No Reboot Mode"
Low = Disabled (Default)

ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Chief River Mobile platform

Change Net name due to this function is high active

Placement near to YH1

SPI ROM for BIOS & ME (4MByte)

4MB ROM P/N:
SA000041P00
SA00003K800
SA00004LI00

SPI ROM for Win8 (2MByte)

2MB ROM P/N:
SA000041N00
SA00003FO10

Socket: SP07000F500/SP07000H900
Please place U13 & U4 close to U2 PCH,
please place RH66, RH67, RH68 near UH3
Please place RH267 near RH66, Please place RH271 ne ar RH67,
Please place RH269 near RH68.

BOOT BIOS Strap Bit 0
If use GCLK, please delete DH1

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Issued Date	2011/11/11	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: PCH_HDA/JTAG/SATA/SPI/LPC

Size	Document Number	Rev
Custom	QCLA4 LA-8861P M/B	0.2

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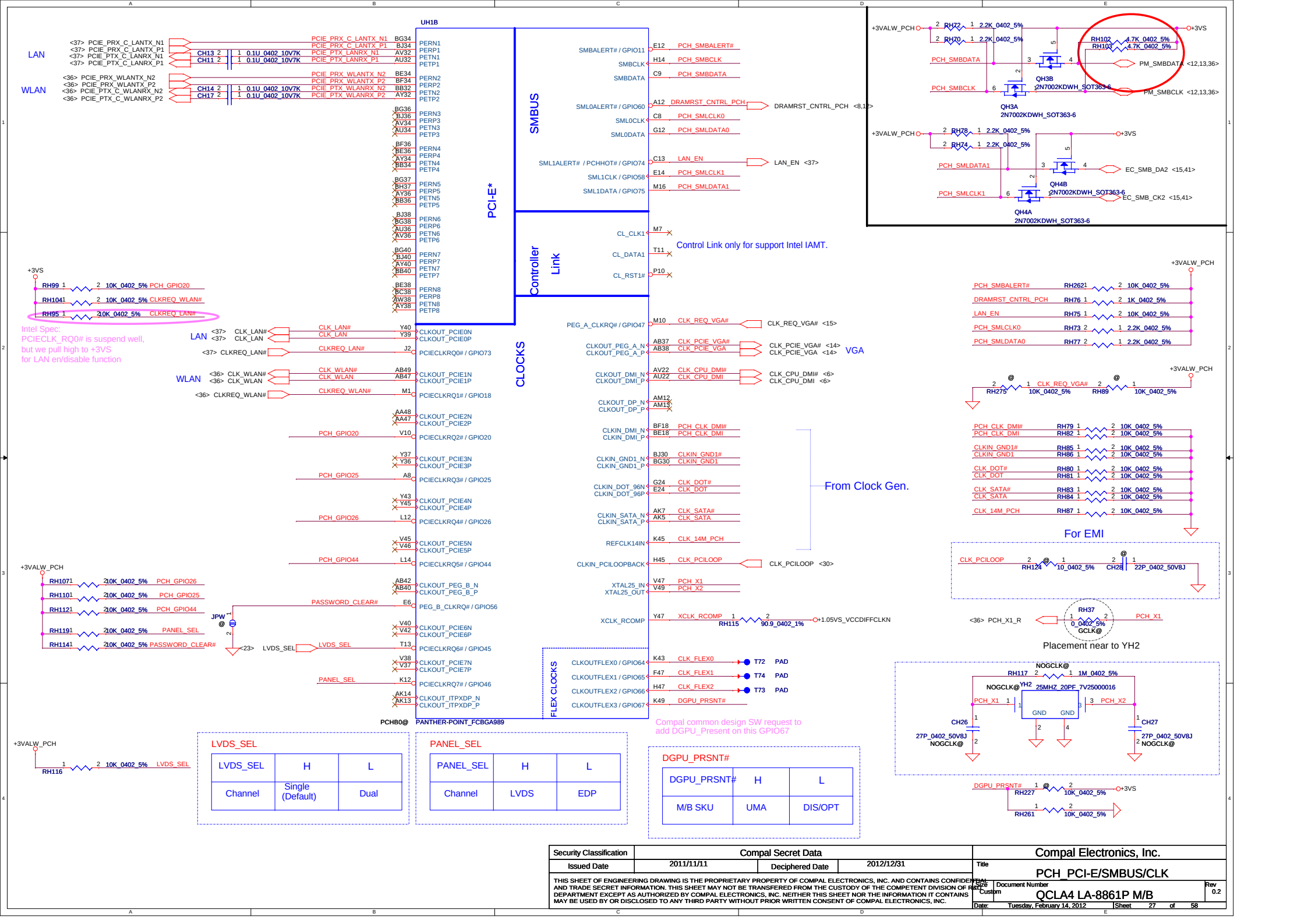

Security Classification	Compal Secret Data		
Issued Date	2011/11/11	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PCH_PCI-E/SMBUS/CLK		
Size	Custom	Document Number	QCLA4 LA-8861P M/B
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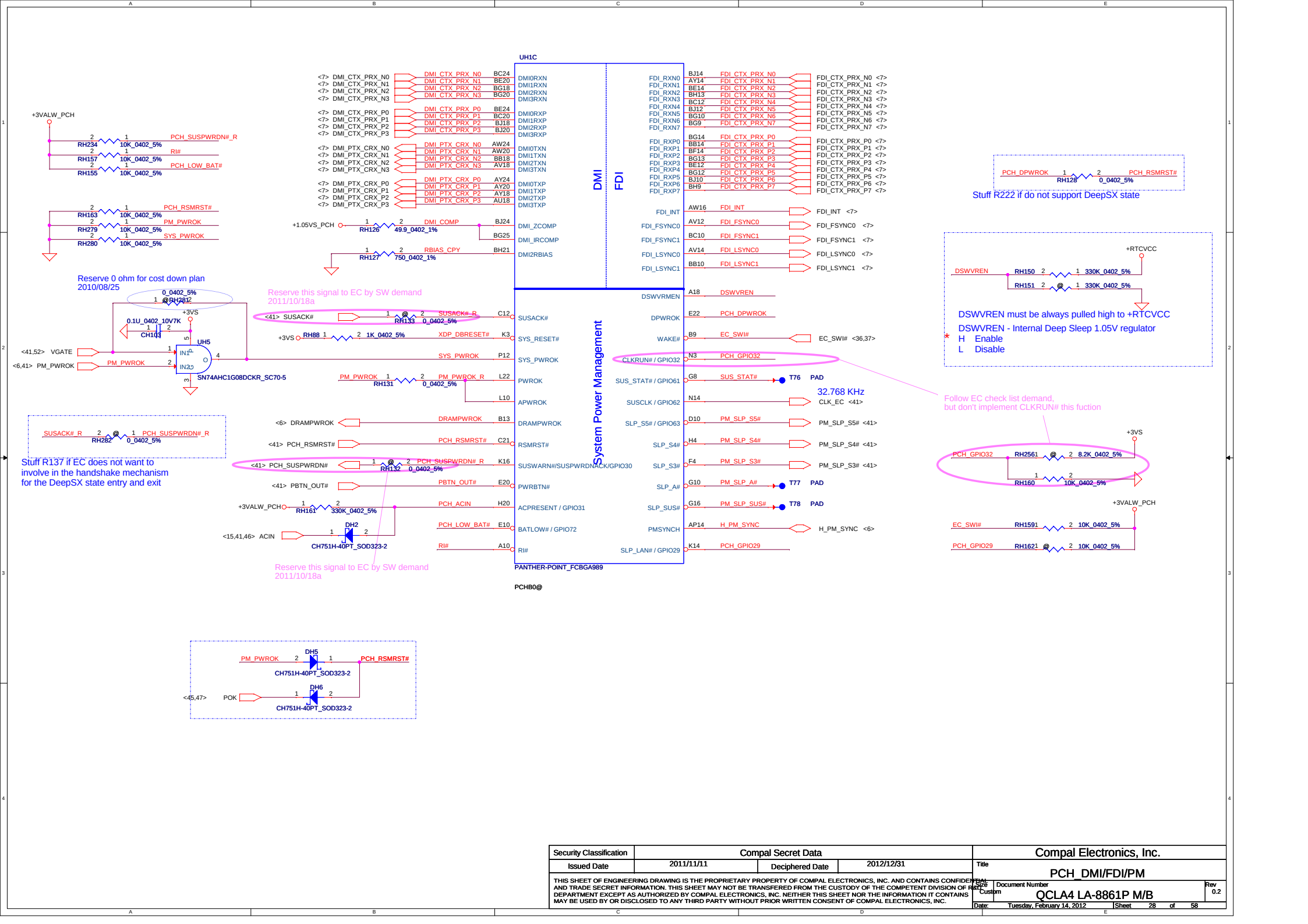
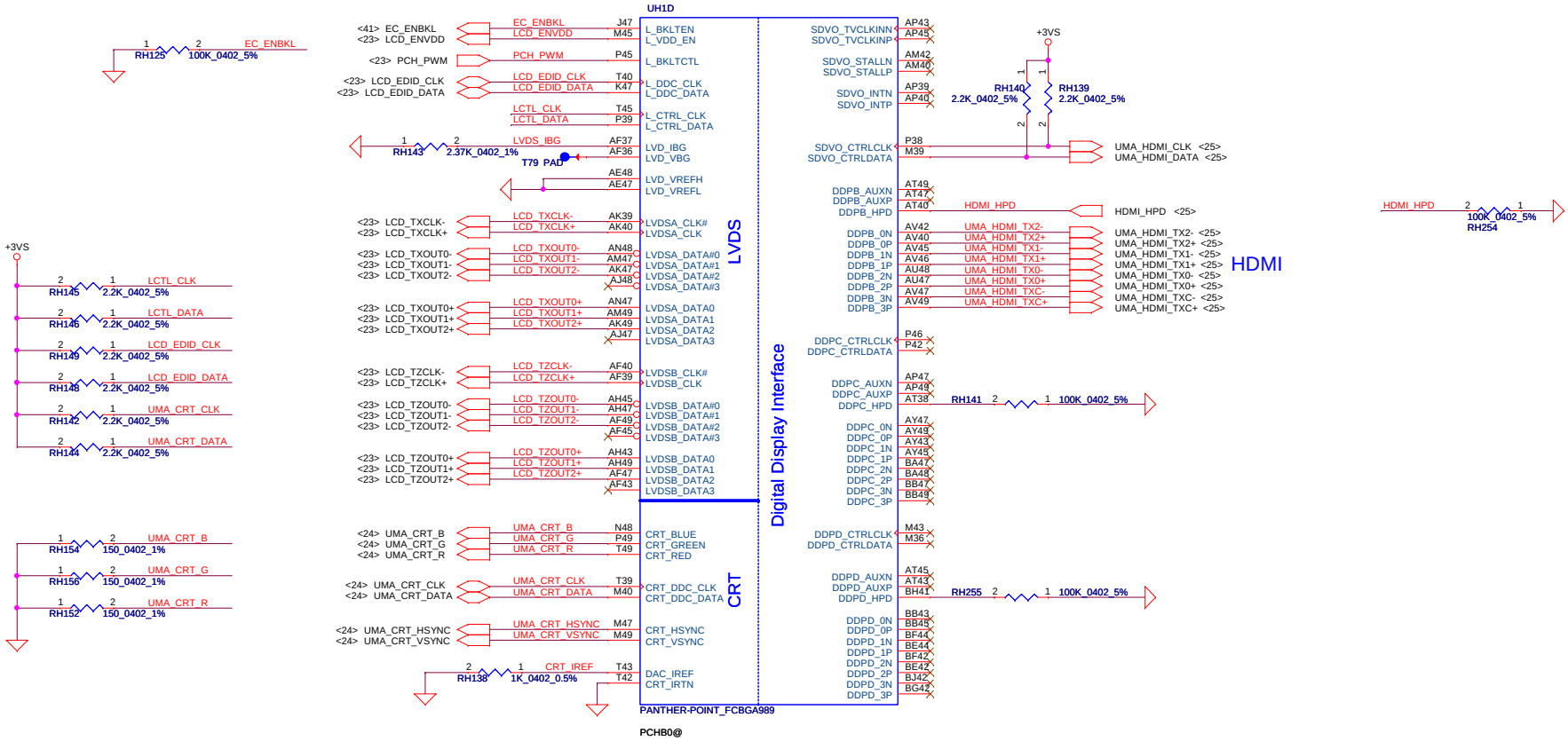
Date:	Tuesday, February 14, 2012	Sheet	27 of 58



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/11	Deciphered Date 2012/12/31	Title: PCH_DMI/FDI/PM
Size: D26 Custom	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 28 of 58		



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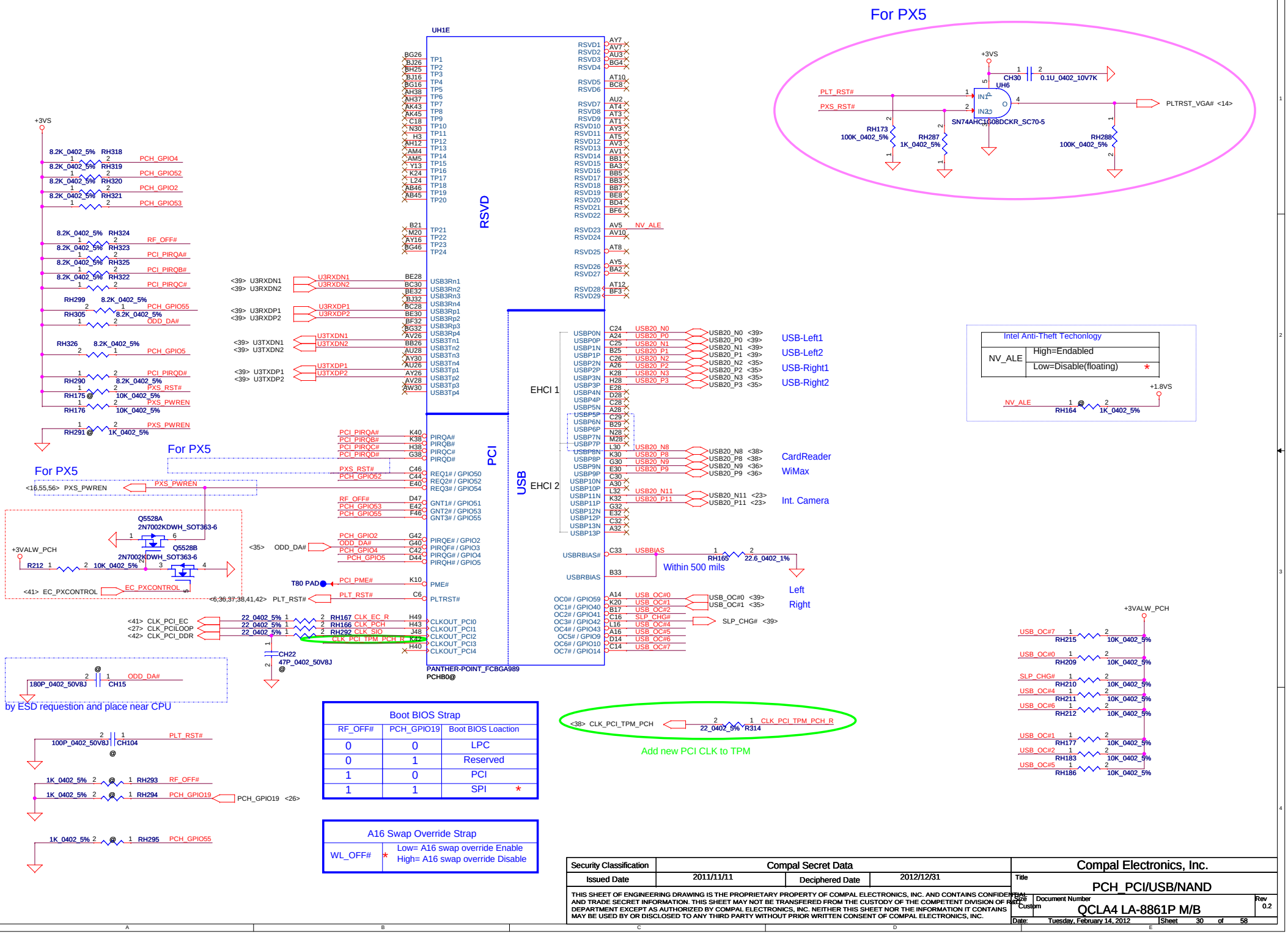
Size: Custom	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 29 of 58		



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Title: PCH_PCI/USB/NAND

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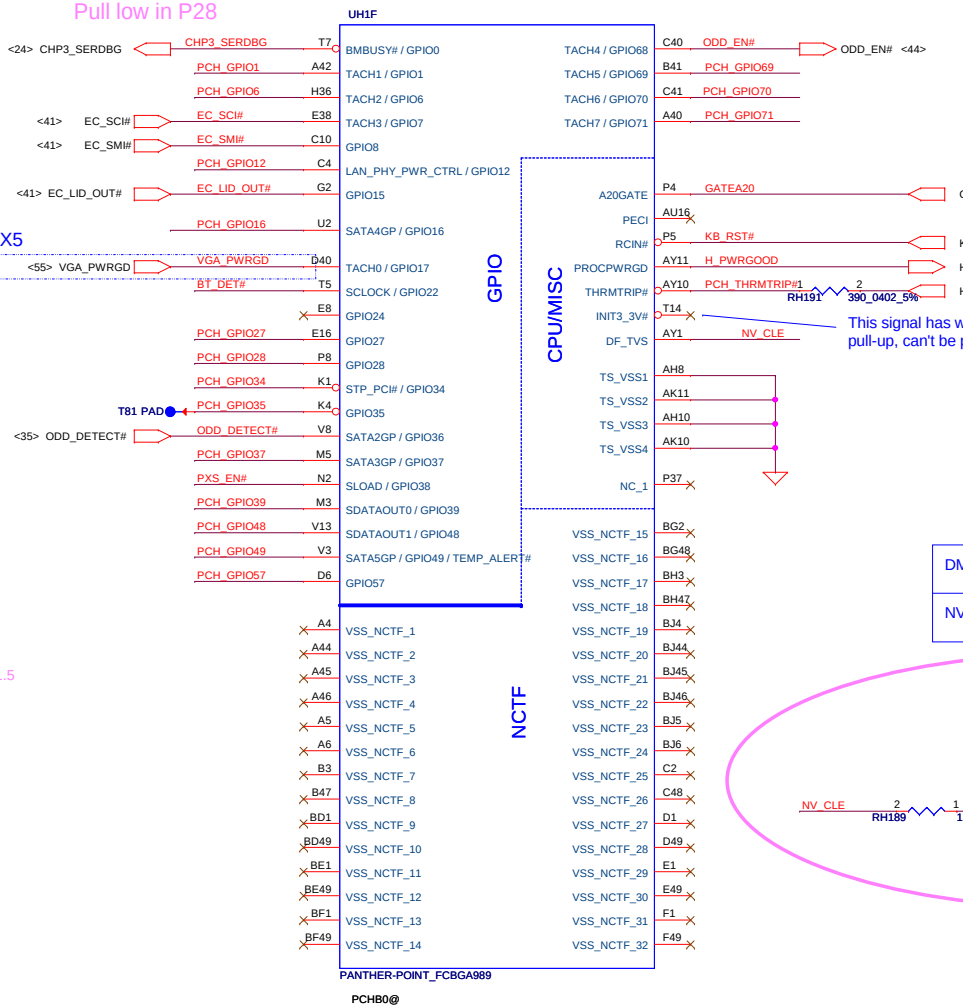
Pull low in P28

UH1F



PCHB0@

<24> CHP3_SERDBG — CHP3_SERDBG — T7
PCH_GPIO1 — A42
PCH_GPIO6 — H36
<41> EC_SCI# — EC_SCI# — E38
<41> EC_SMI# — EC_SMI# — C10
PCH_GPIO12 — C4
<41> EC_LID_OUT# — EC_LID_OUT# — G2
PCH_GPIO16 — U2

For PX5

<55> VGA_PWRGD — VGA_PWRGD — D40
BT_DET# — T5
E8
PCH_GPIO27 — E16
PCH_GPIO28 — P8
PCH_GPIO34 — K1
T81 PAD — PCH_GPIO35 — K4
<35> ODD_DETECT# — ODD_DETECT# — V8
PCH_GPIO37 — M5
PXS_EN# — N2
PCH_GPIO39 — M3
PCH_GPIO48 — V13
PCH_GPIO49 — V3
PCH_GPIO57 — D6

C40 — ODD_EN# — ODD_EN# <44>
B41 — PCH_GPIO69
C41 — PCH_GPIO70
A40 — PCH_GPIO71

P4 — GATEA20 — GATEA20 <41>
AU16
P5 — KB_RST# — KB_RST# <41>
AY11 — H_PWRGOOD — H_PWRGOOD <6>
AY10 — PCH_THRMTRIP# — RH191 2 390_0402_5% 1 — H_THERMTRIP# <6>
T14
AY1 — NV_CLE

This signal has weak internal pull-up, can't be pulled low

AH8
AK11
AH10
AK10
P37

A4 — VSS_NCTF_1
A44 — VSS_NCTF_2
A45 — VSS_NCTF_3
A46 — VSS_NCTF_4
A5 — VSS_NCTF_5
A6 — VSS_NCTF_6
B3 — VSS_NCTF_7
B47 — VSS_NCTF_8
BD1 — VSS_NCTF_9
BD49 — VSS_NCTF_10
BE1 — VSS_NCTF_11
BE49 — VSS_NCTF_12
BF1 — VSS_NCTF_13
BF49 — VSS_NCTF_14

BG2 — VSS_NCTF_15
BG48 — VSS_NCTF_16
BH3 — VSS_NCTF_17
BH47 — VSS_NCTF_18
BJ4 — VSS_NCTF_19
BJ44 — VSS_NCTF_20
BJ45 — VSS_NCTF_21
BJ46 — VSS_NCTF_22
BJ5 — VSS_NCTF_23
BJ6 — VSS_NCTF_24
C2 — VSS_NCTF_25
C48 — VSS_NCTF_26
D1 — VSS_NCTF_27
D49 — VSS_NCTF_28
E1 — VSS_NCTF_29
E49 — VSS_NCTF_30
F1 — VSS_NCTF_31
F49 — VSS_NCTF_32

+3VALW_PCH

RH204 2 1K_0402_5% 1 EC_LID_OUT#
RH205 2 10K_0402_5% 1 EC_SMI#
RH298 2 10K_0402_5% 1 PCH_GPIO12
RH202 2 10K_0402_5% 1 PCH_GPIO28
RH207 2 10K_0402_5% 1 PCH_GPIO57

+3VS

RH180 2 10K_0402_5% 1 PCH_GPIO34
RH190 2 10K_0402_5% 1 PCH_GPIO1
RH185 2 10K_0402_5% 1 BT_DET#
RH178 2 200K_0402_5% 1 ODD_DETECT#
RH197 2 10K_0402_5% 1 PCH_GPIO6
RH179 2 10K_0402_5% 1 PCH_GPIO16
RH303 2 10K_0402_5% 1 EC_SCI#
RH194 2 10K_0402_5% 1 PCH_GPIO39
RH304 2 10K_0402_5% 1 PCH_GPIO48
RH195 2 10K_0402_5% 1 PCH_GPIO49
RH216 2 1K_0402_5% 1 CHP3_SERDBG

RH198 2 10K_0402_5% 1 PCH_GPIO37
RH199 2 @ 10K_0402_5% 1 PCH_GPIO27
RH201 2 10K_0402_5% 1 PXS_EN#

Follow Compal ORB
and Intel Check list 460603 V1.5

+3VS

RH300 PCH_GPIO69
RH297 ODD_EN#
RH182 GATEA20
RH184 KB_RST#
RH315 PCH_GPIO70
10K_0402_5%

+3VS

RH203 PCH_GPIO71 10K_0402_5%

DMI & FDI Termination Voltage

NV_CLE	
	Set to VCC when HIGH
	Set to VSS when LOW

+1.8VS

RH187 2.2K_0402_5%
RH188 2.2K_0402_5%
NV_CLE — RH189 2 1K_0402_5% 1 — DH54 PMEG2010AEH_SOD123 — H_SNB_IVB# <6,12>

GPIO28

* On-Die PLL Voltage Regulator
H: Enable
L: Disable

RH206 1 @ 2 1K_0402_5% PCH_GPIO28

GPIO8

Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable

RH308 1 @ 2 1K_0402_5% EC_SMI#

Integrated clock enable functionality
is achieved by soft-strap
The current default is clock enable

PXS_EN#

PXS_EN#	H	L
SKU	NonPXS	PXS

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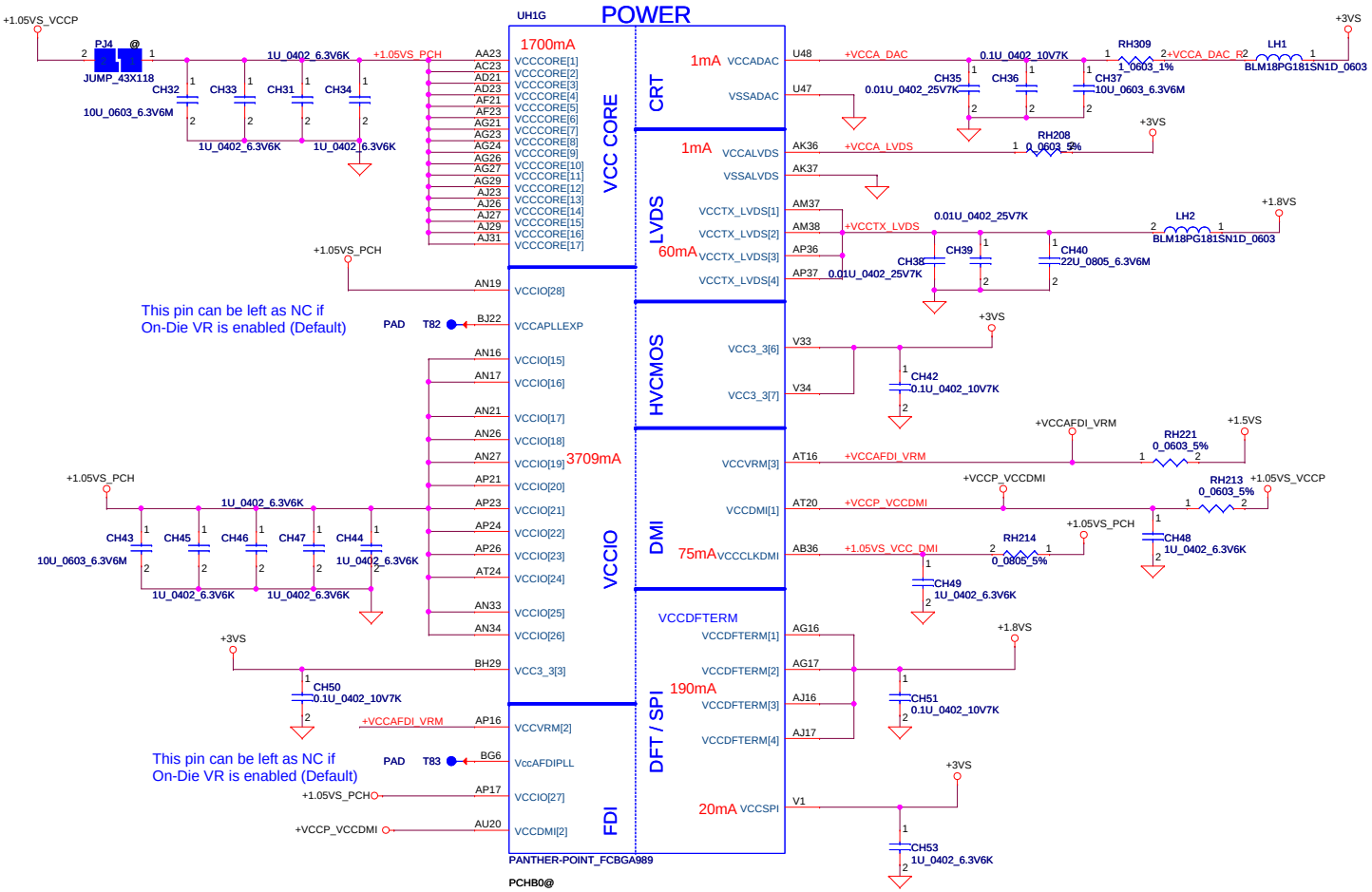
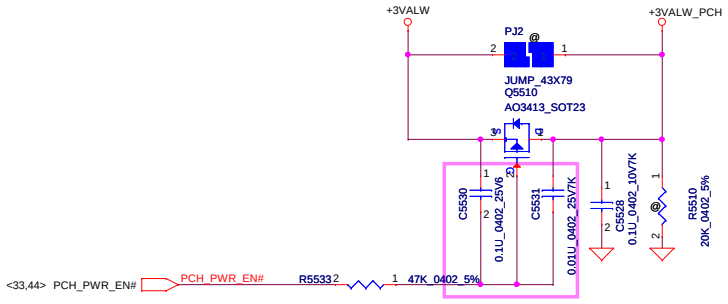
Date: Tuesday, February 14, 2012	Sheet 31 of 58		



PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3V_PCH



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Compal Electronics, Inc.

Title: PCH_POWER-1

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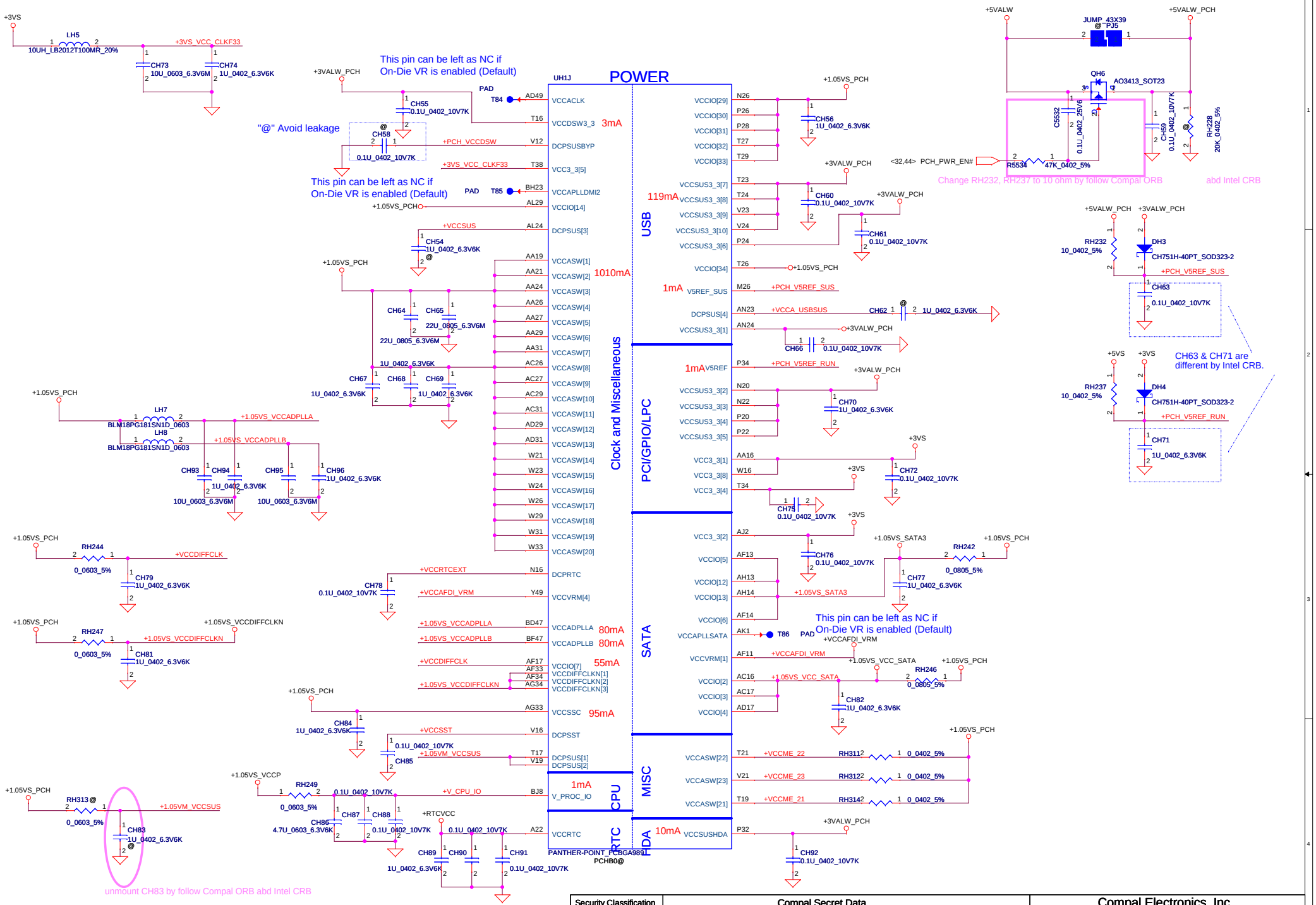

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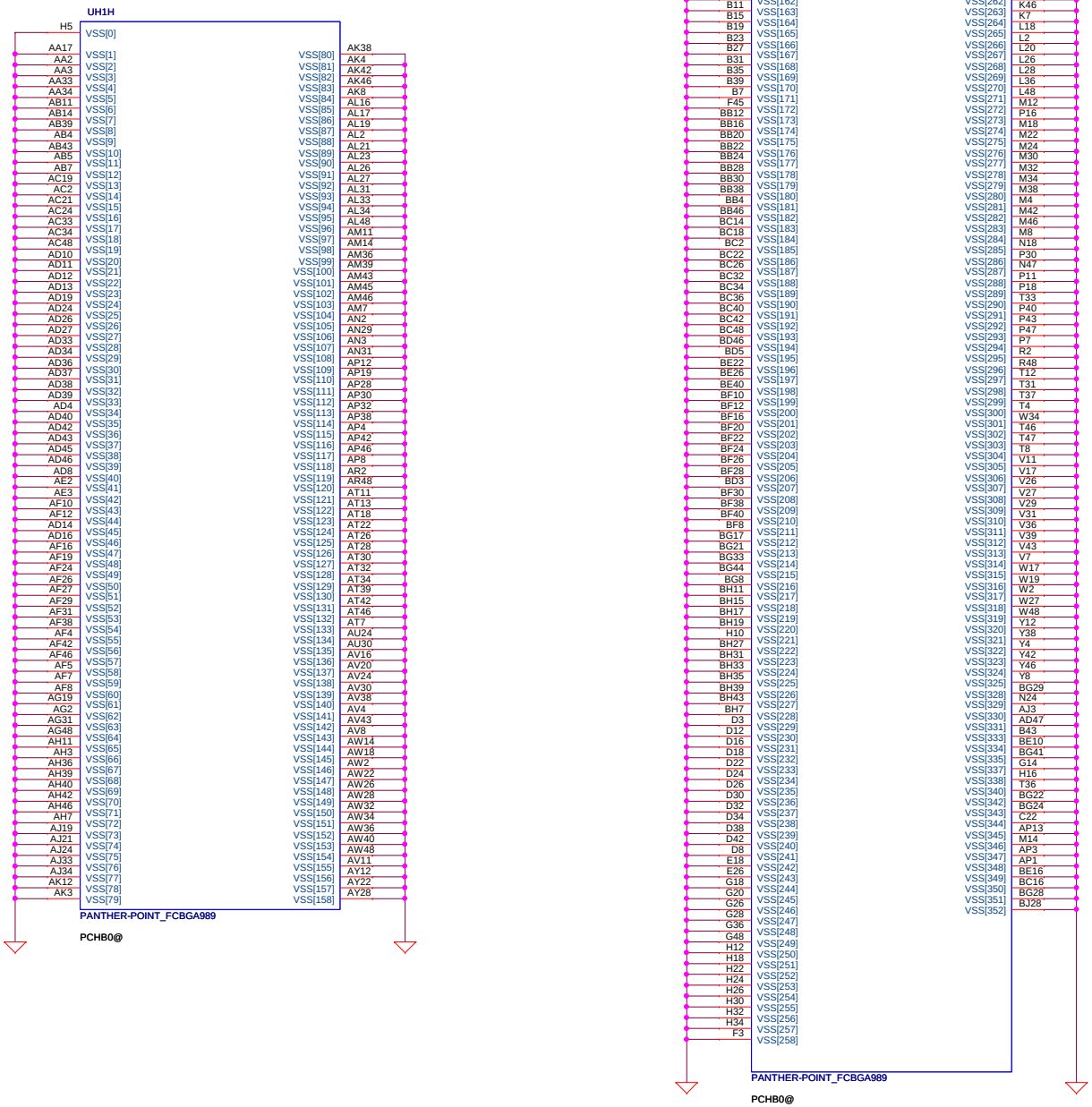
Compal Electronics, Inc.			
Title: PCH_POWER-2			
Size: Custom	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 33 of 58		



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Size Custom	Document Number QCLA4 LA-8861P M/B	Rev 0.2
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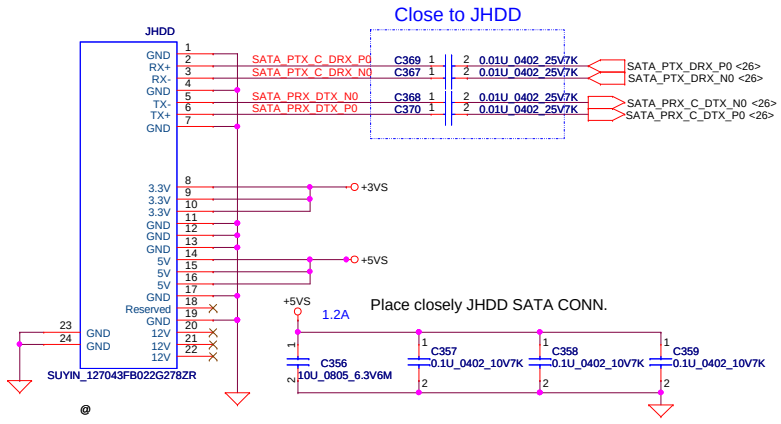
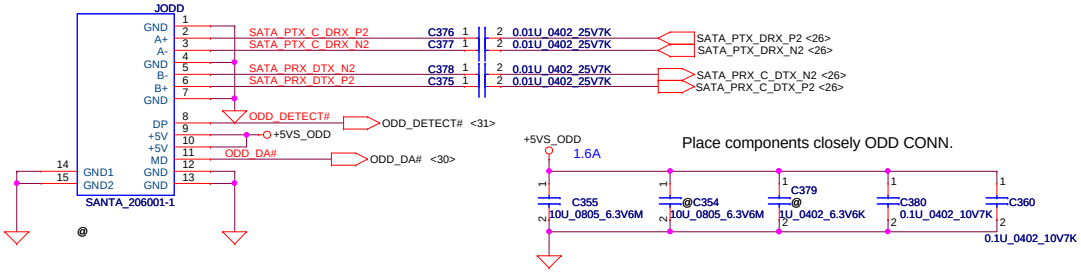
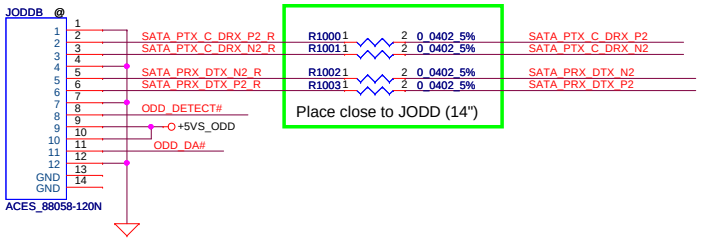
SATA HDD Conn.



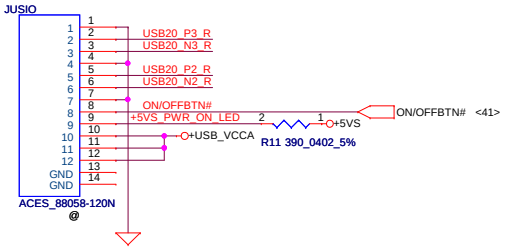
SATA ODD Conn

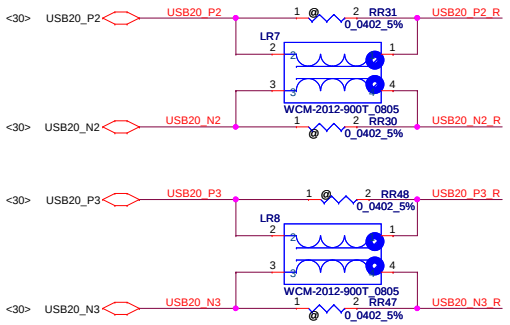


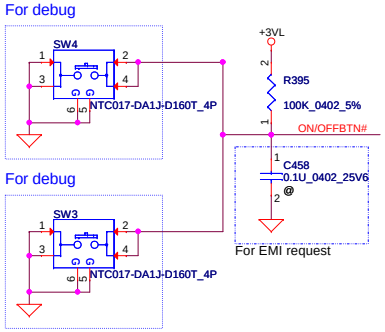
SATA ODD Conn (for 15')

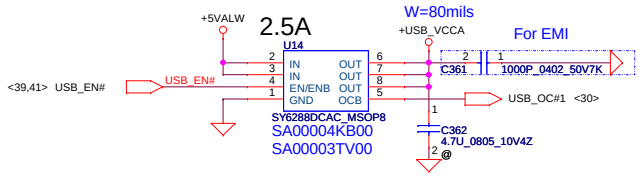


Power Button & RUSB connector









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Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB

Size | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

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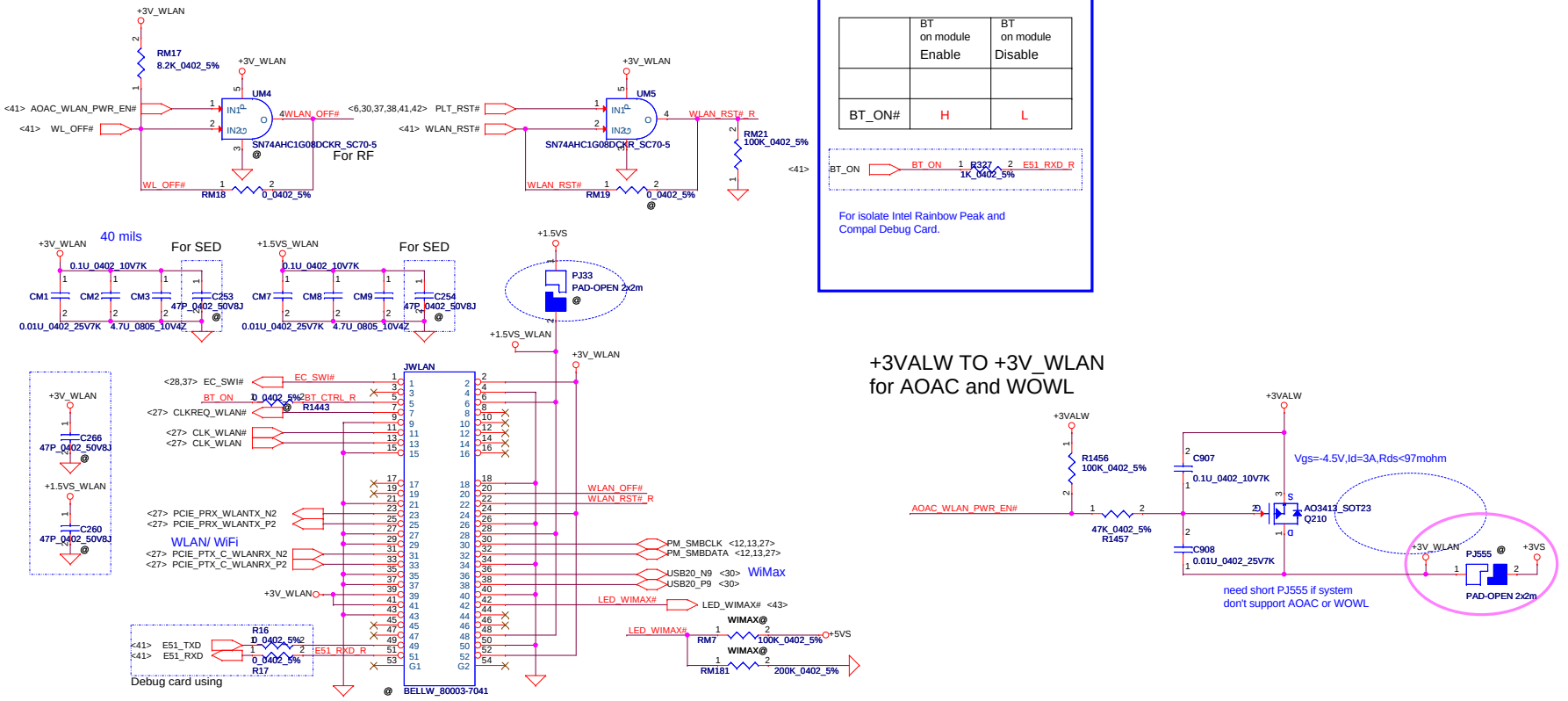
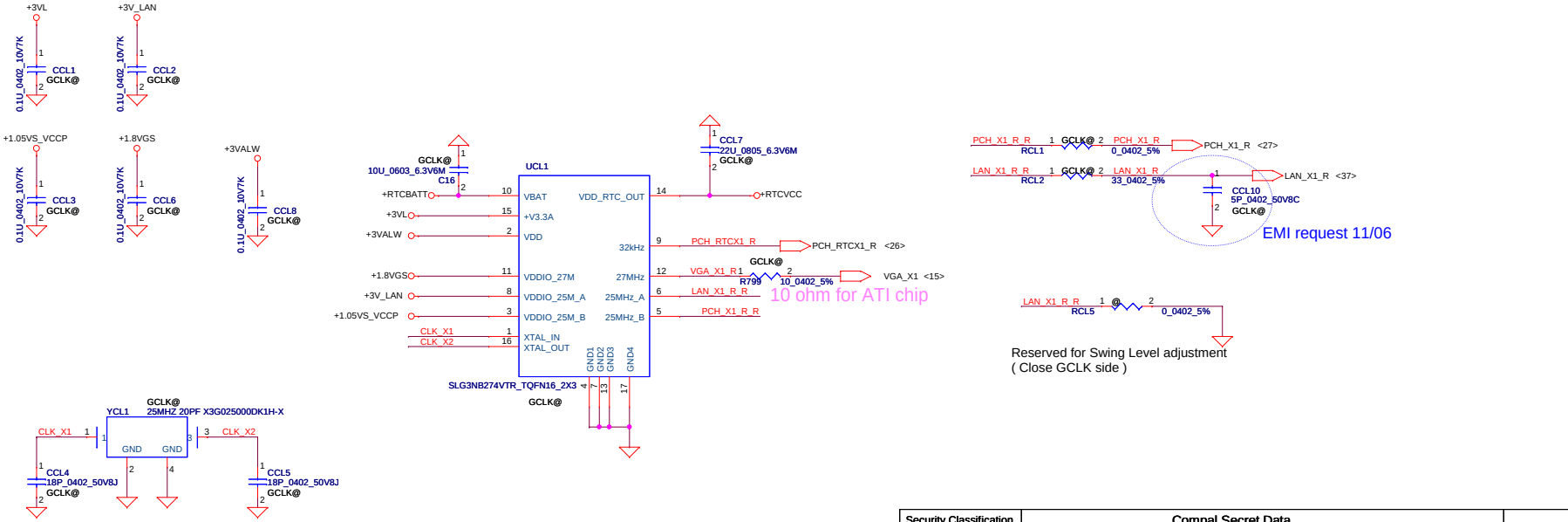
Slot 1 Half PCIe Mini Card-WLAN/ WiMax





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Compal Electronics, Inc.

Title: PCIe-WLAN/GCLK

Size	Document Number	Rev
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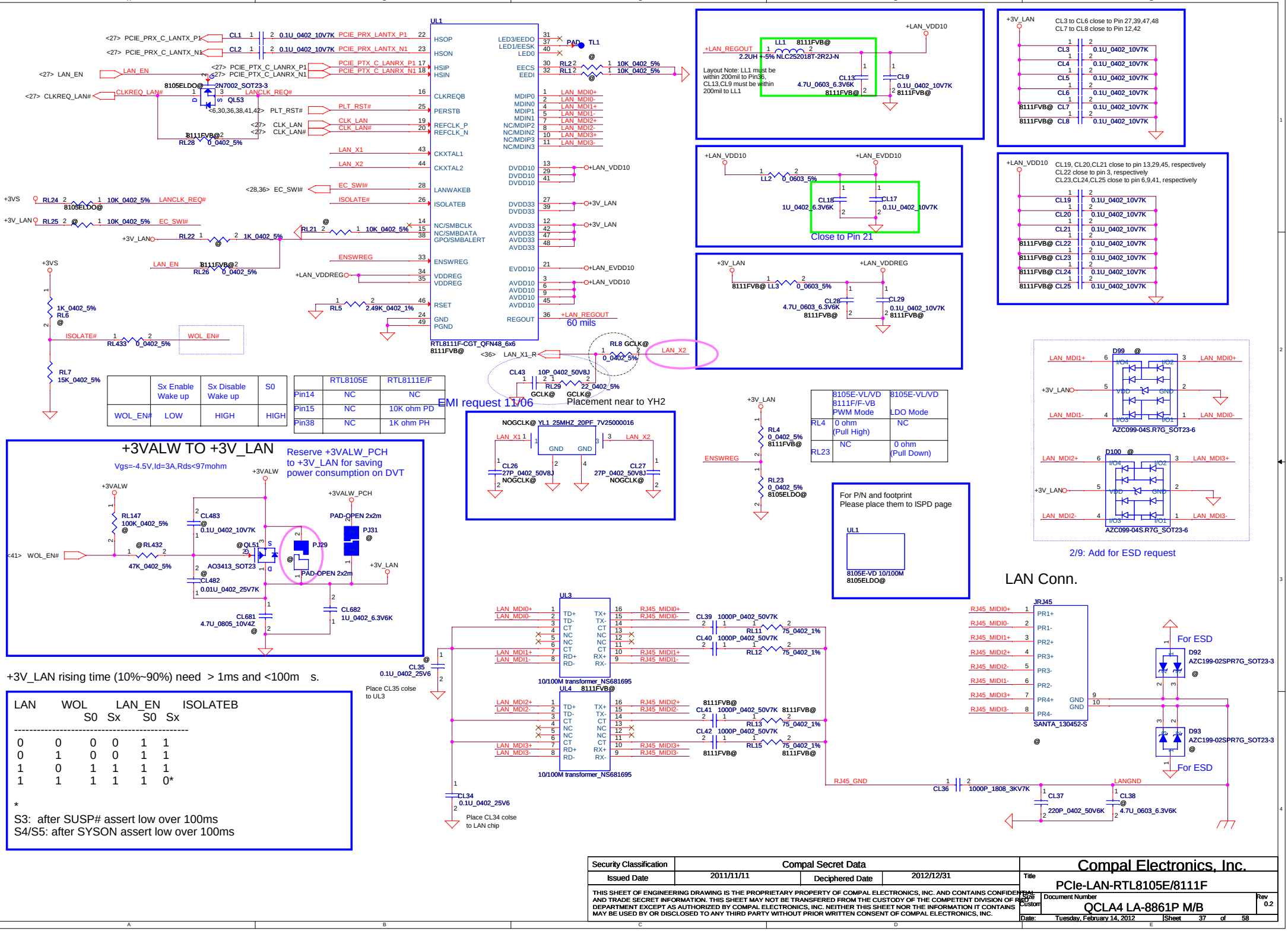

	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

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Title	PCIe-LAN-RTL8105E/8111F
Size: Custom	Document Number: QCLA4 LA-8861P M/B
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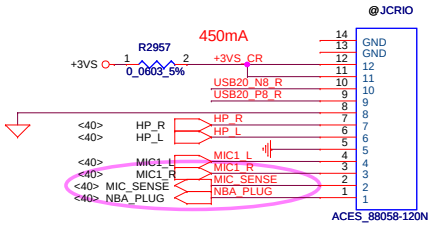
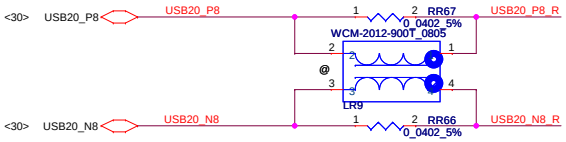
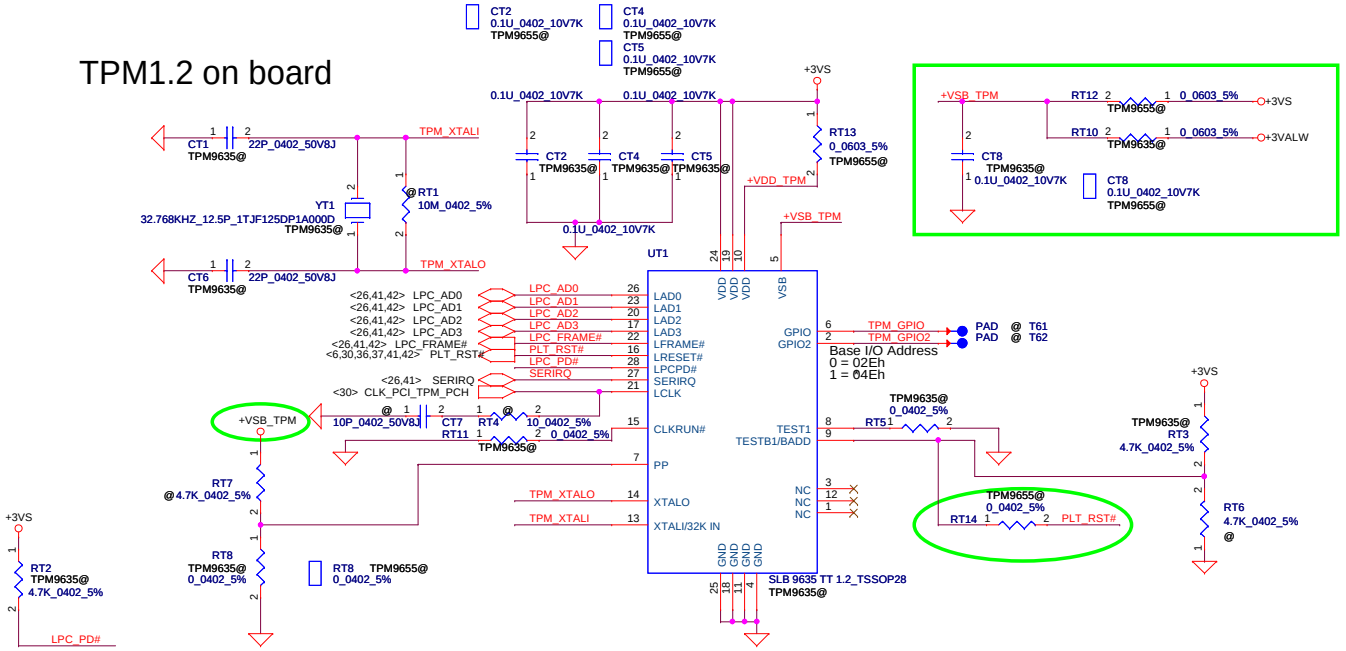
CardReader Conn.





TPM1.2 on board



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Compal Electronics, Inc.

Title: USB-CardReader RTS5129/TPM

Size: Custom | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

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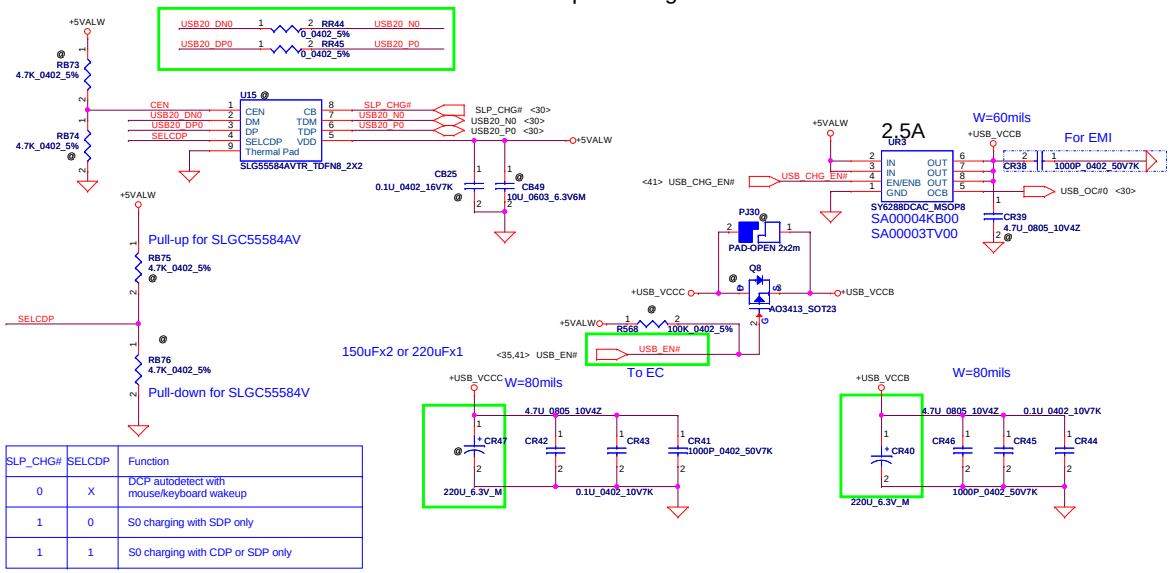
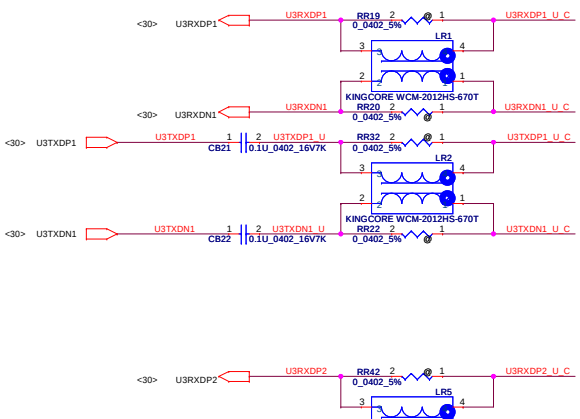
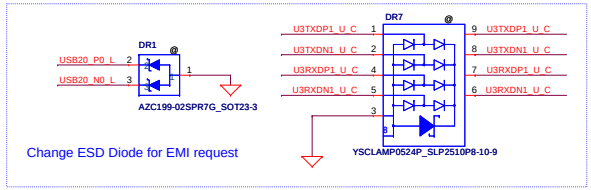
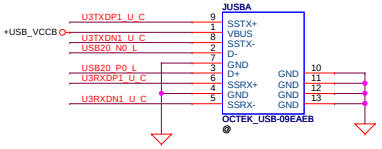
Sleep & Charge Function

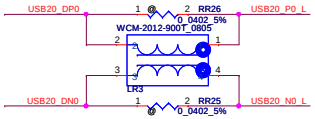


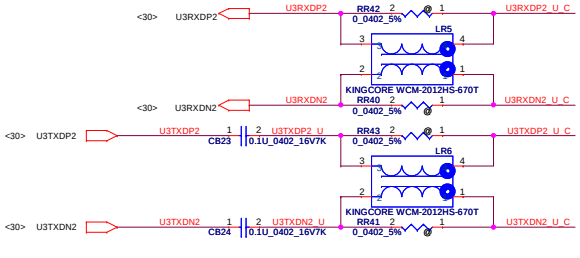
SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only

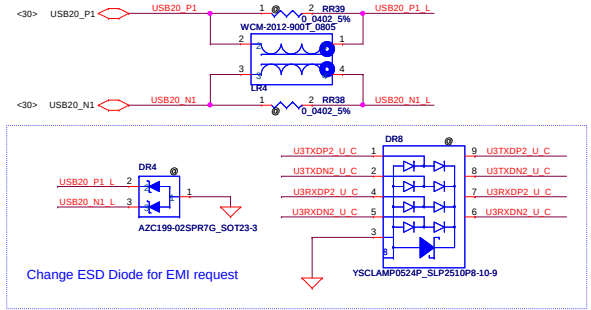


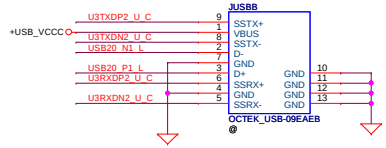












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Issued Date	2011/11/11	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCIe-USB3.0 connector

Size: Custom | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

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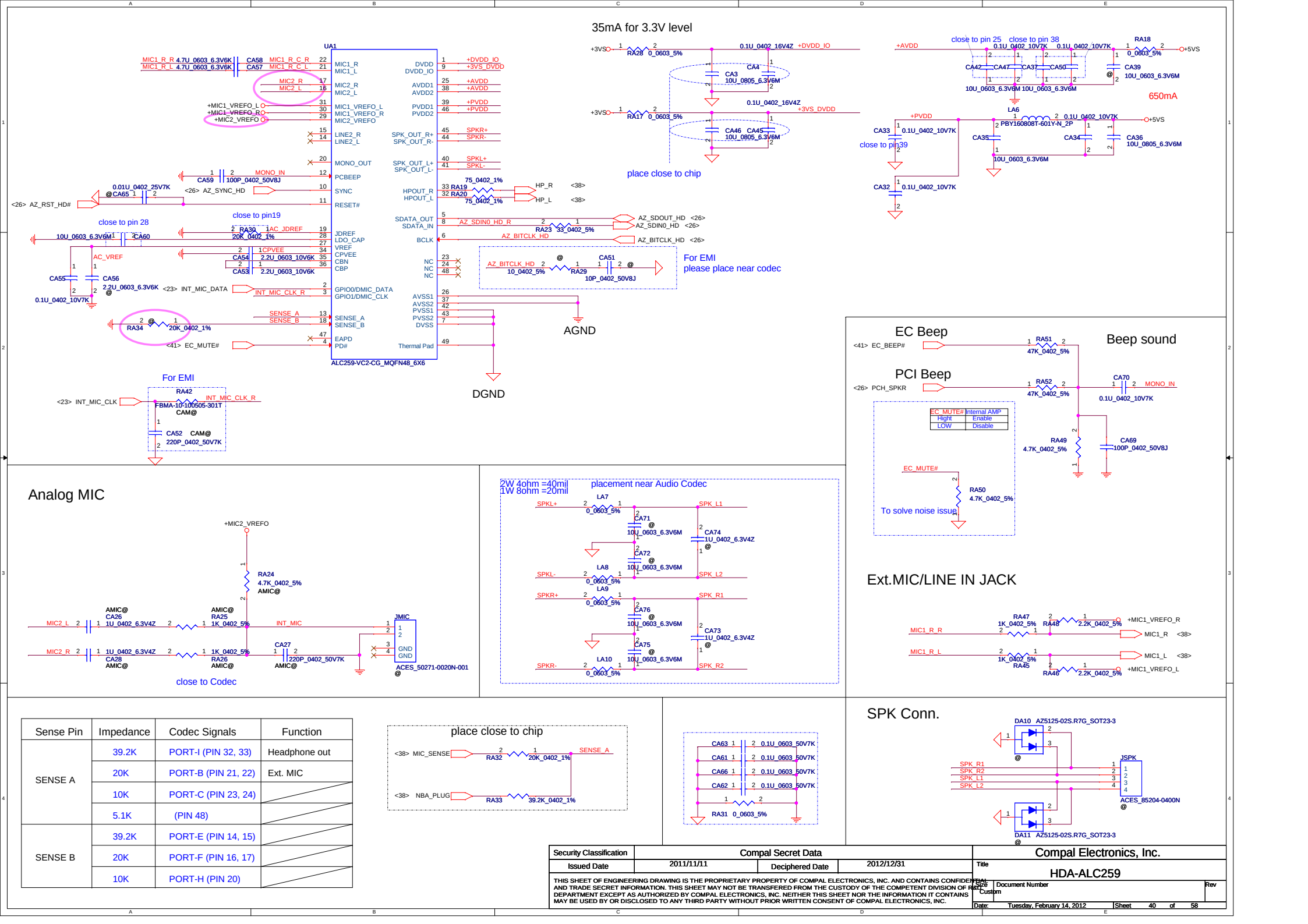

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

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Compal Electronics, Inc.

Title: HDA-ALC259

Size: Custom | Document Number | Rev

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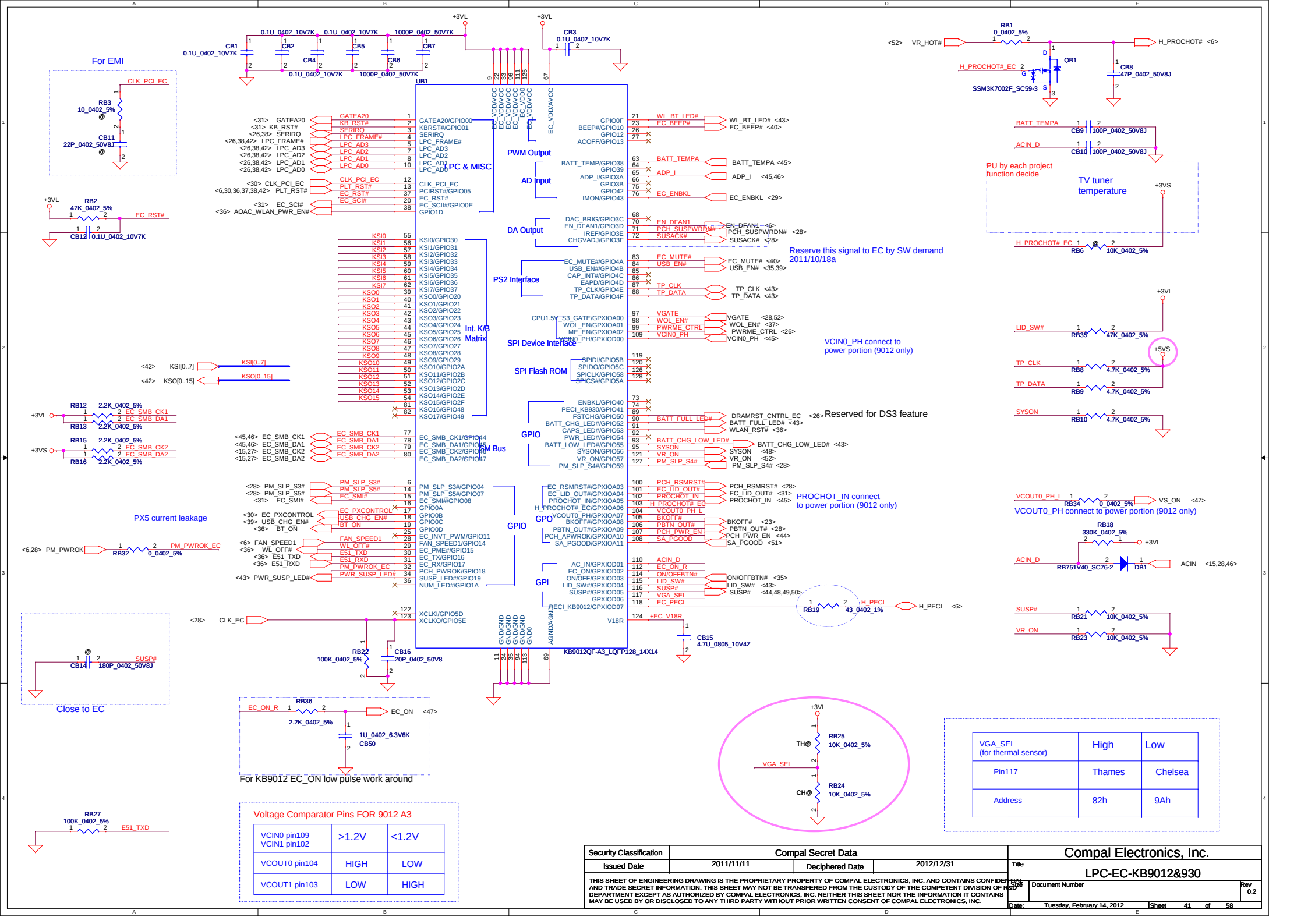

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Compal Electronics, Inc.

Title: LPC-EC-KB9012&930

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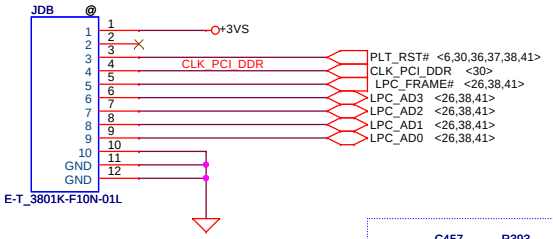
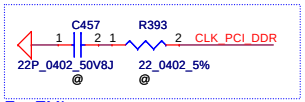
LPC Debug Port

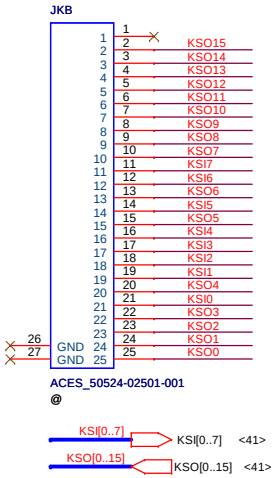
Place the PAD under DDR DIMM.

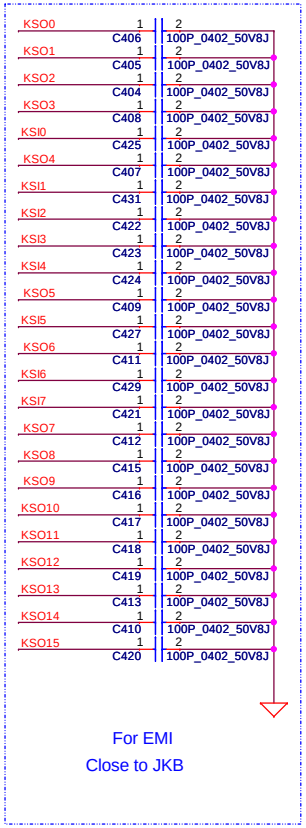




For EMI

KEYBOARD CONN.





For EMI

Close to JKB

Security Classification	Compal Secret Data		
Issued Date	2011/11/11	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Debug/KB

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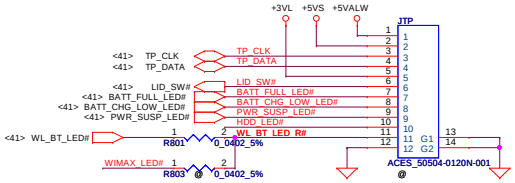
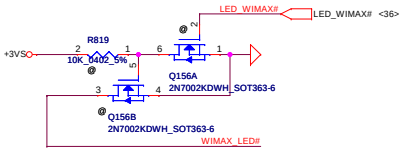
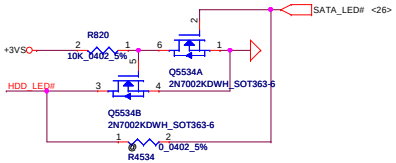
Touchpad Connector



WiMAX LED



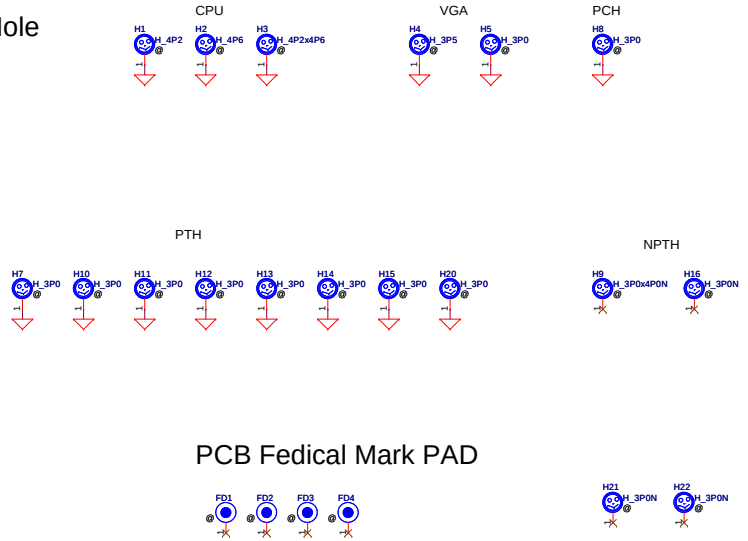
SATA LED



ESD solution

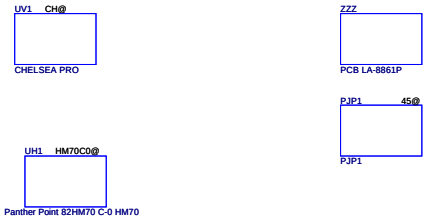
EMI solution

Screw Hole



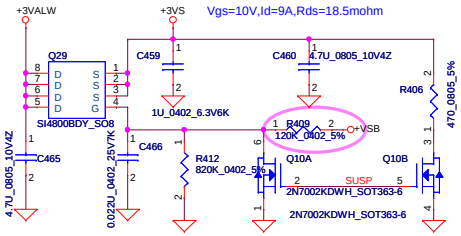
PCB Fedical Mark PAD

ISPD



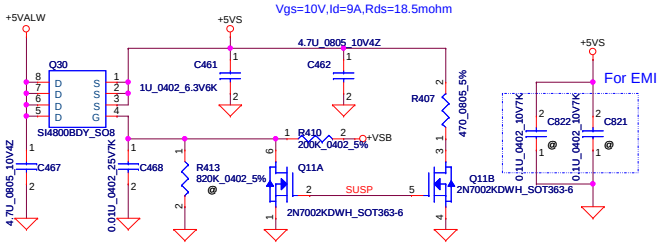
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/11	Deciphered Date 2012/12/31	Title: PWR/TP/LED/LP/LS/Screw
Size	Document Number: QCLA4 LA-8861P M/B		Rev: 0.2
Date: Tuesday, February 14, 2012	Sheet 43 of 58		

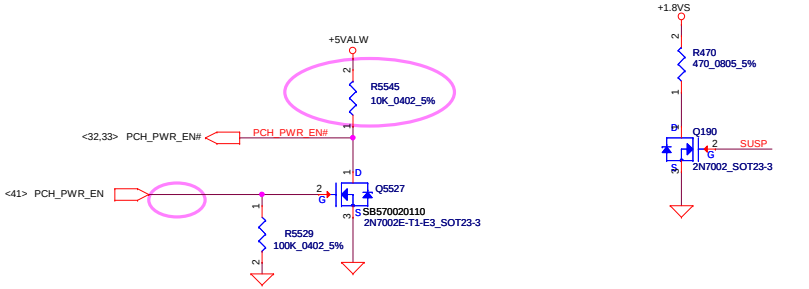
+3VALW TO +3VS



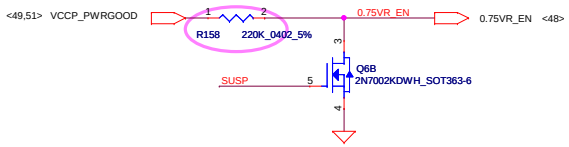
change R409 to 120k 5%

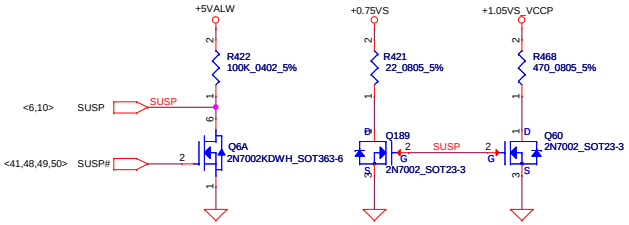
+5VALW TO +5VS



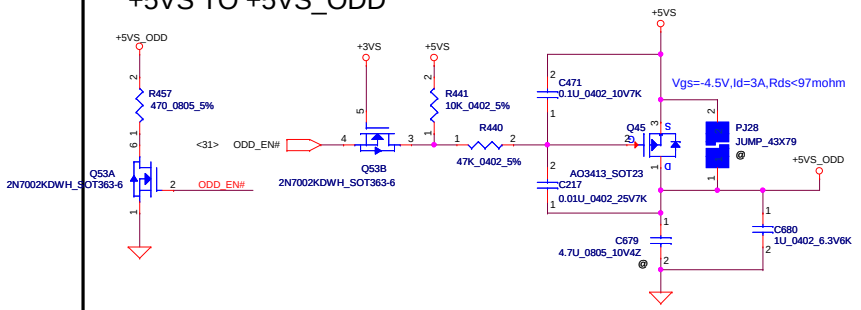


For S3 CPU Power Saving





+5VS TO +5VS_ODD



Security Classification	Compal Secret Data		
Issued Date	2011/11/11	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

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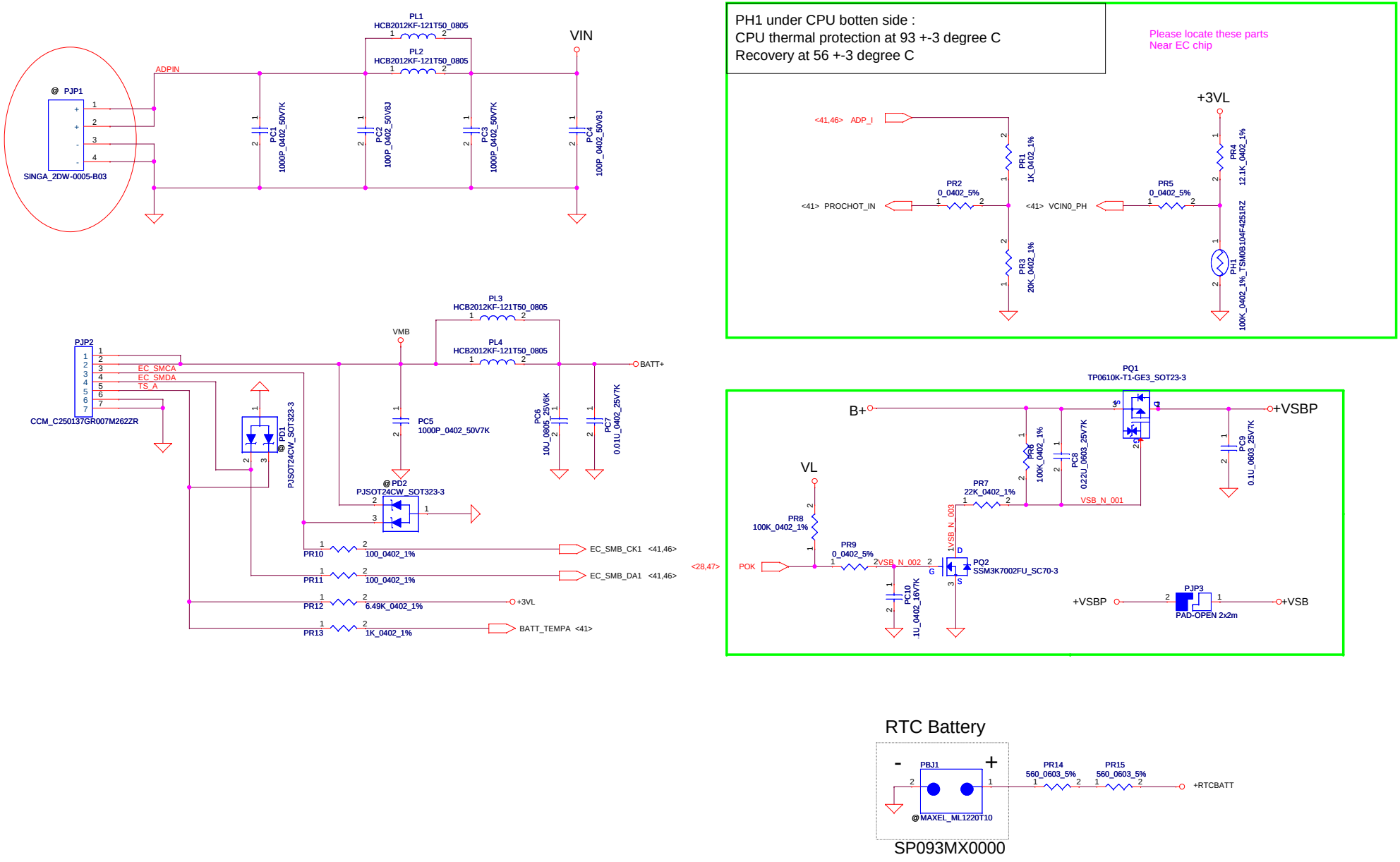


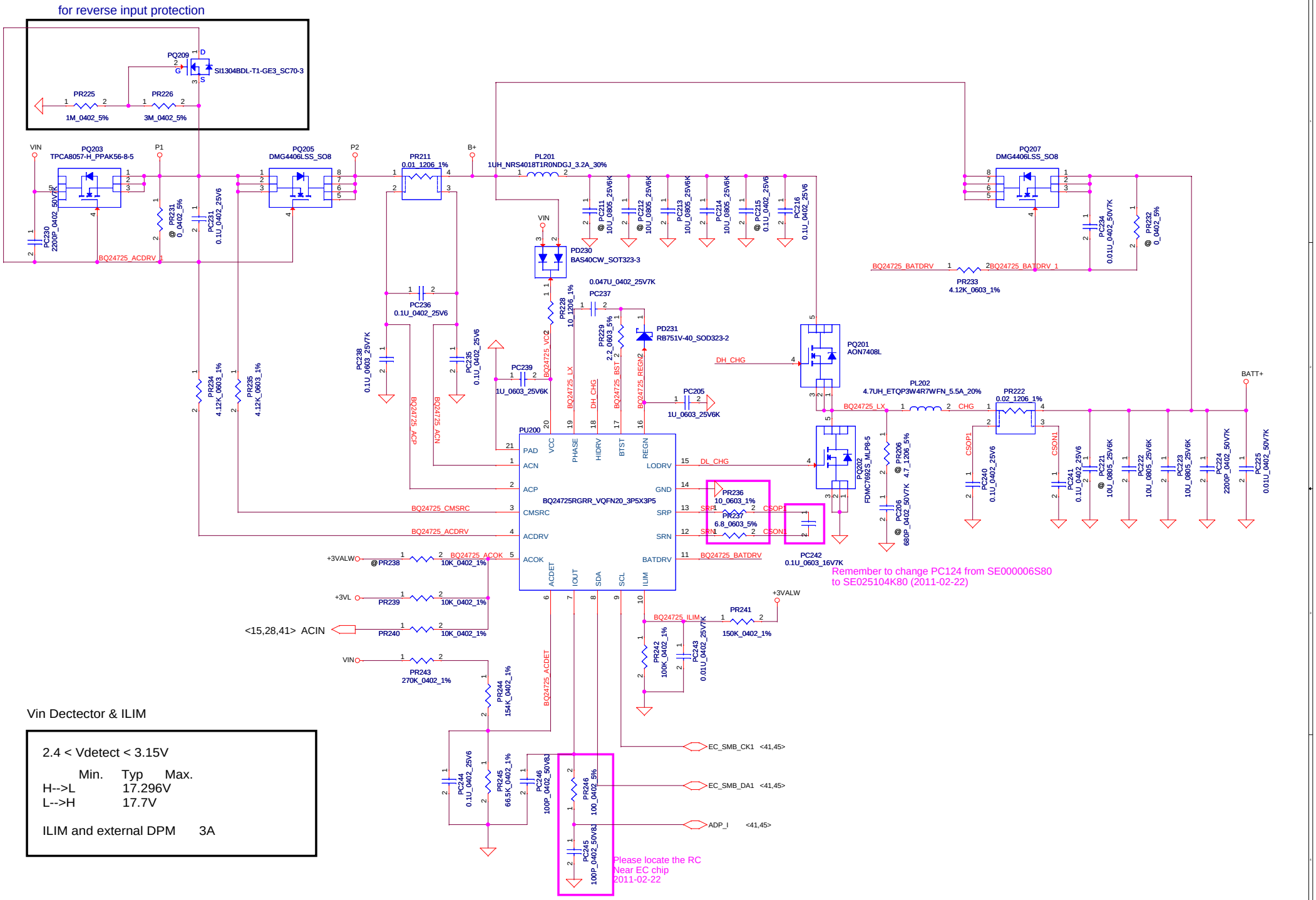
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size | Document Number: SAMSUNG | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 45 of 58



Vin Dectector & ILIM

2.4 < Vdetect < 3.15V

	Min.	Typ	Max.
H-->L		17.296V	
L-->H		17.7V	

ILIM and external DPM 3A

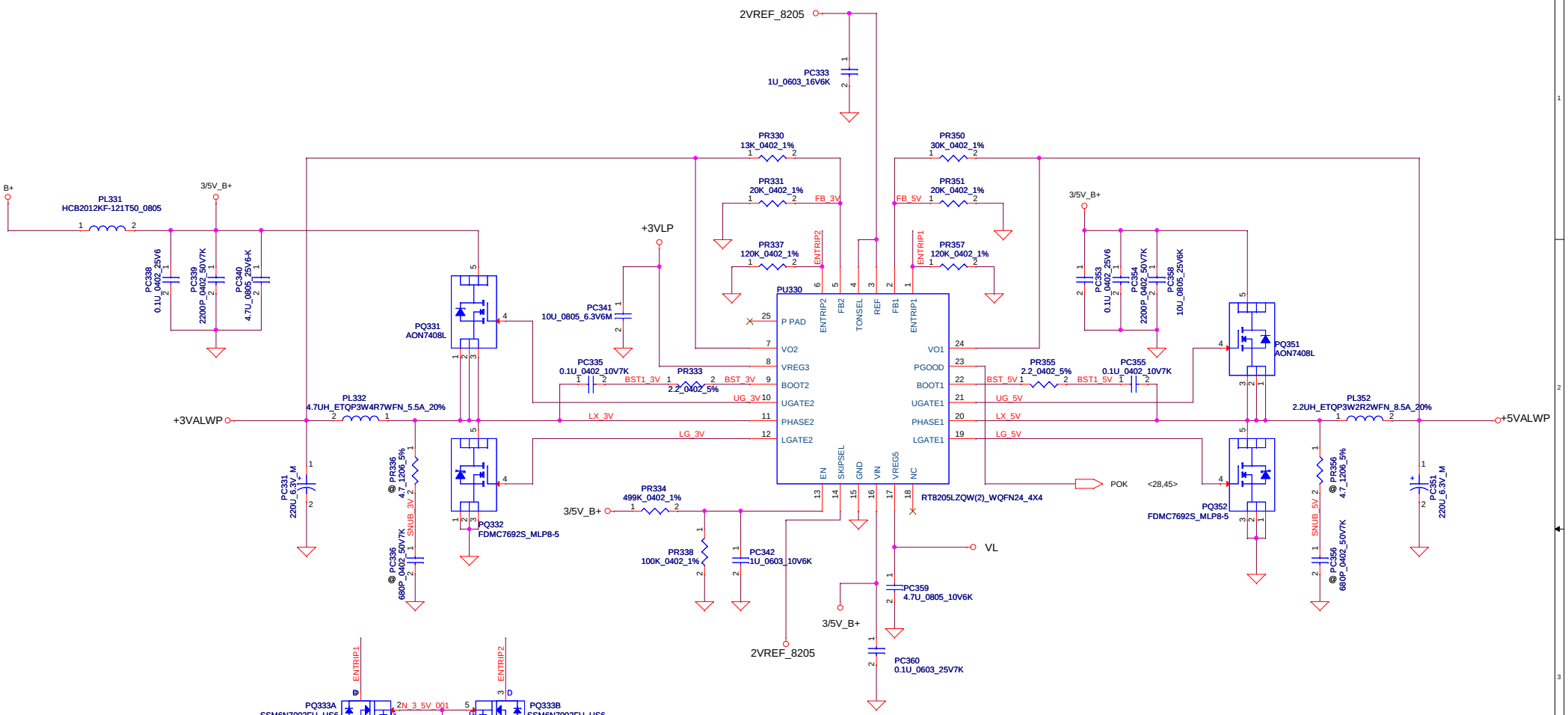
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR-CHARGER

Size | Document Number: SAMSUNG | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 46 of 58



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: Custom	Document Number: QCLA4 LA-8861P M/B	Rev: 0.2
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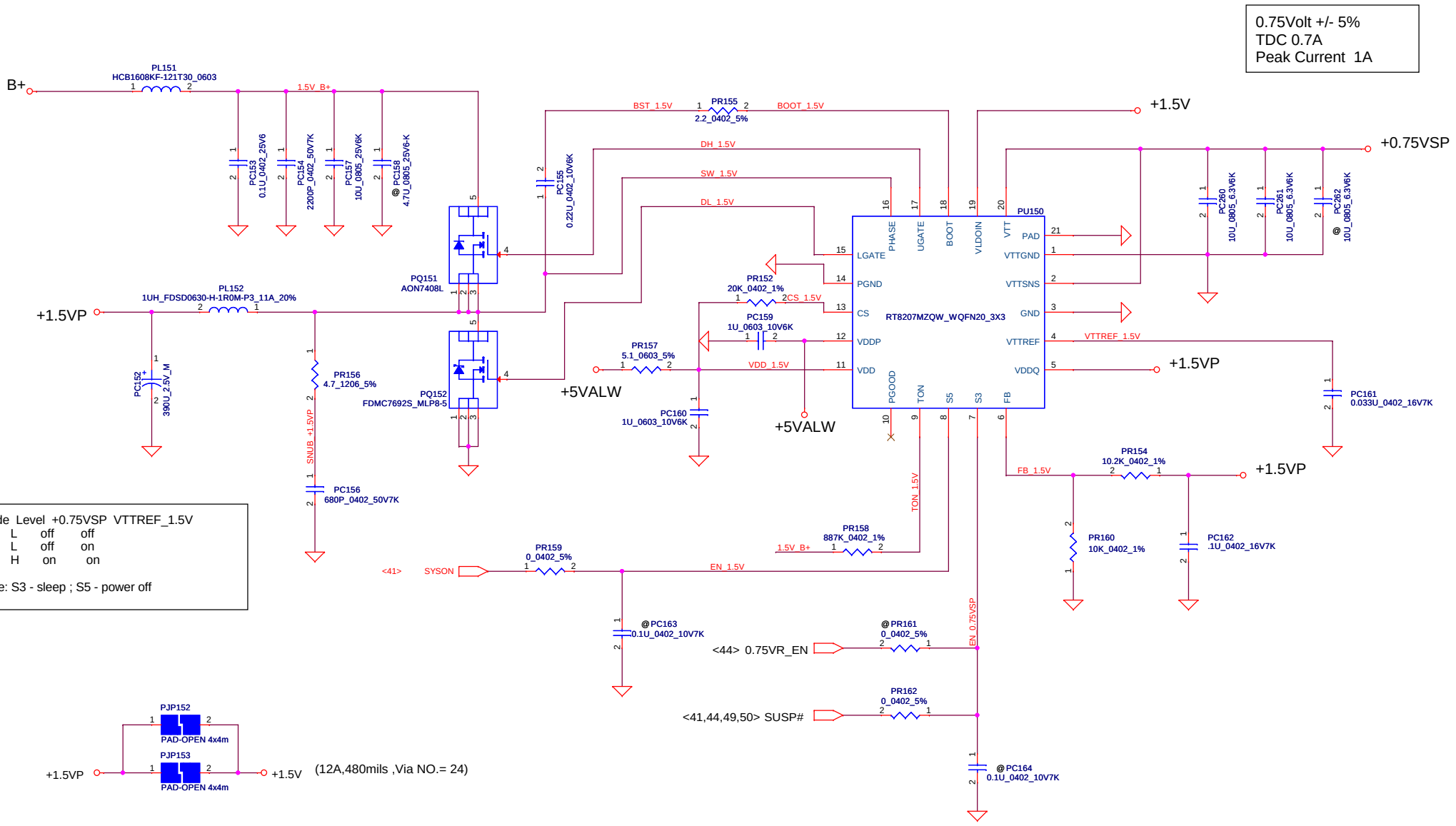


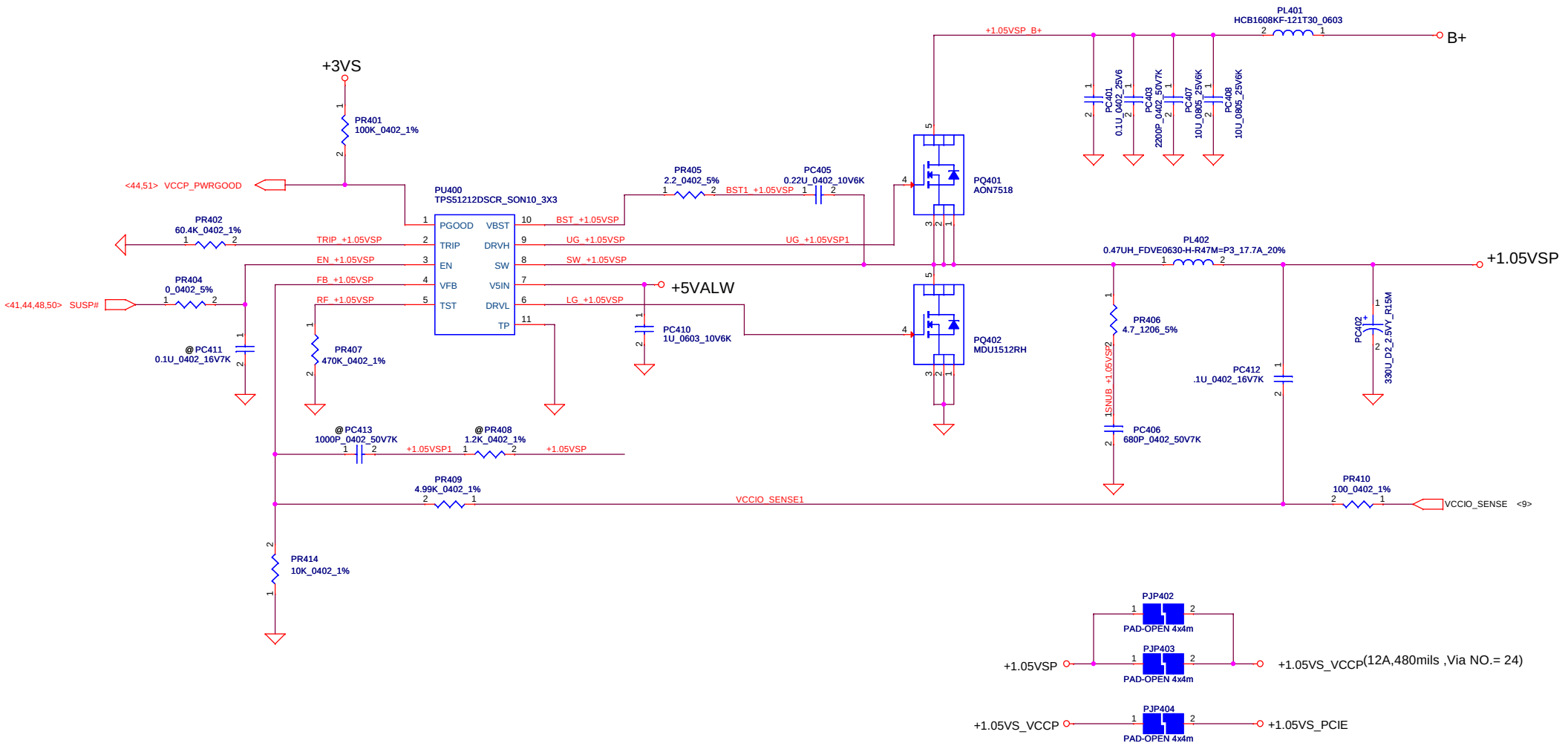
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

Size: Custom | Document Number: SAMSUNG | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 48 of 58

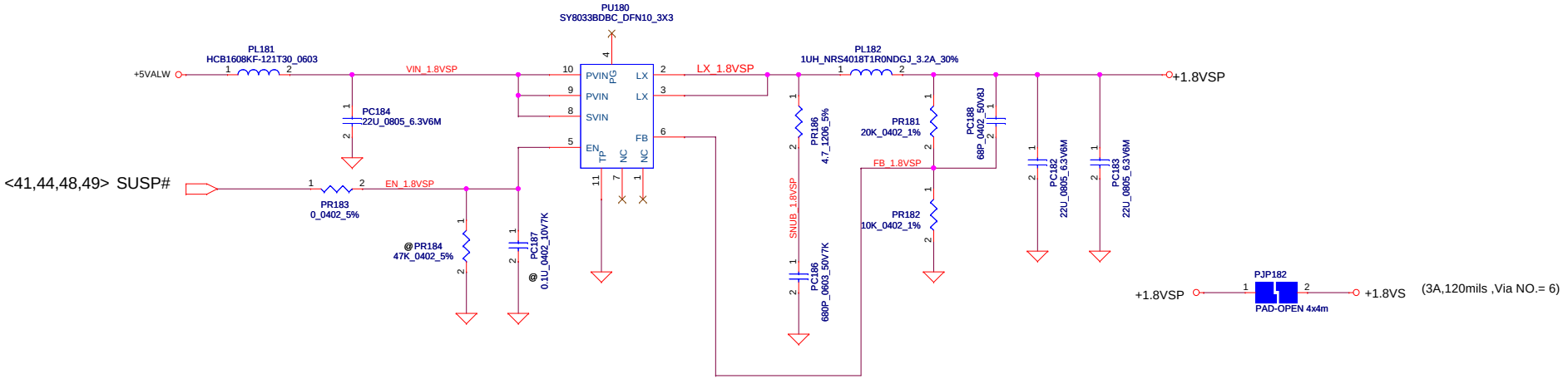


Compal Electronics, Inc.

Title: PWR-V1.05SP

Size: Custom | Document Number: SAMSUNG | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 49 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-1.8VSP

Size | Document Number: SAMSUNG | Rev: 0.2

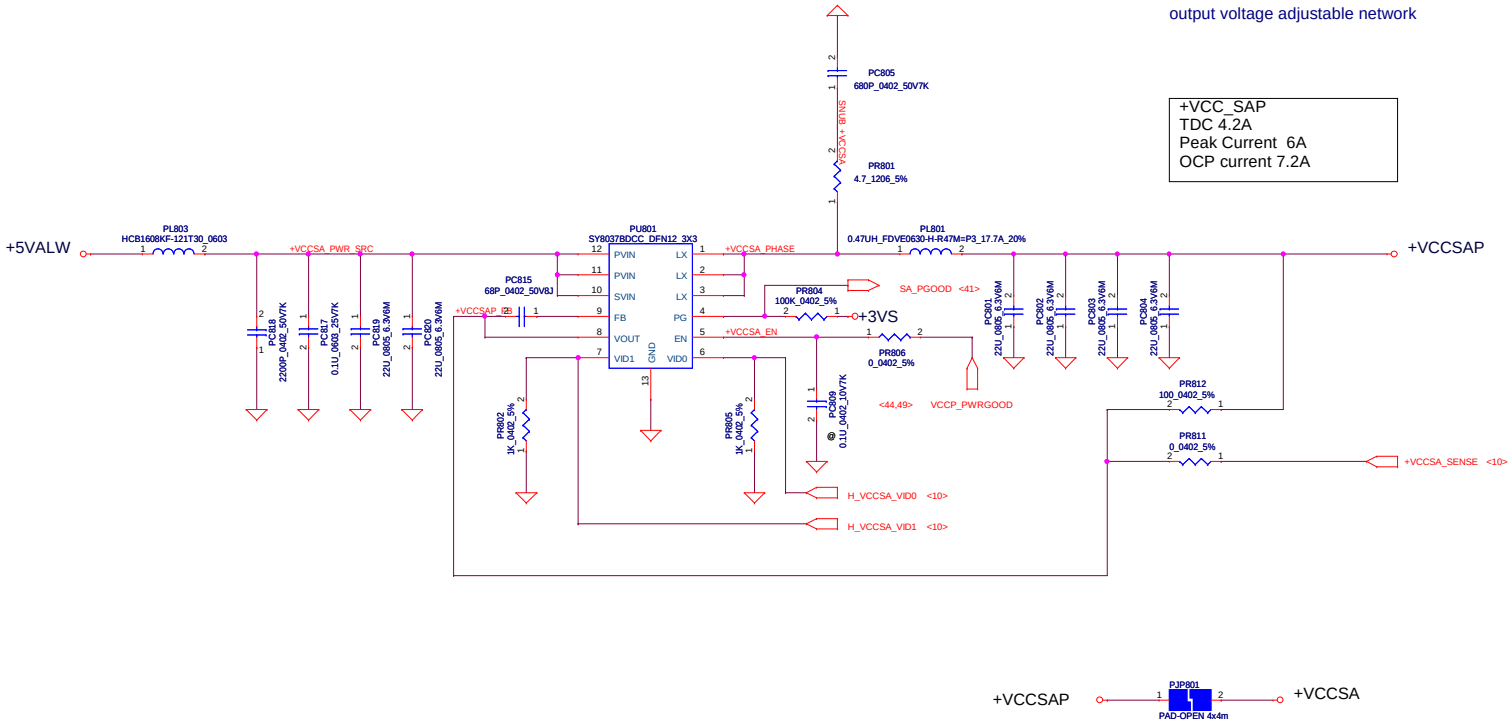
Date: Tuesday, February 14, 2012 | Sheet 50 of 58

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



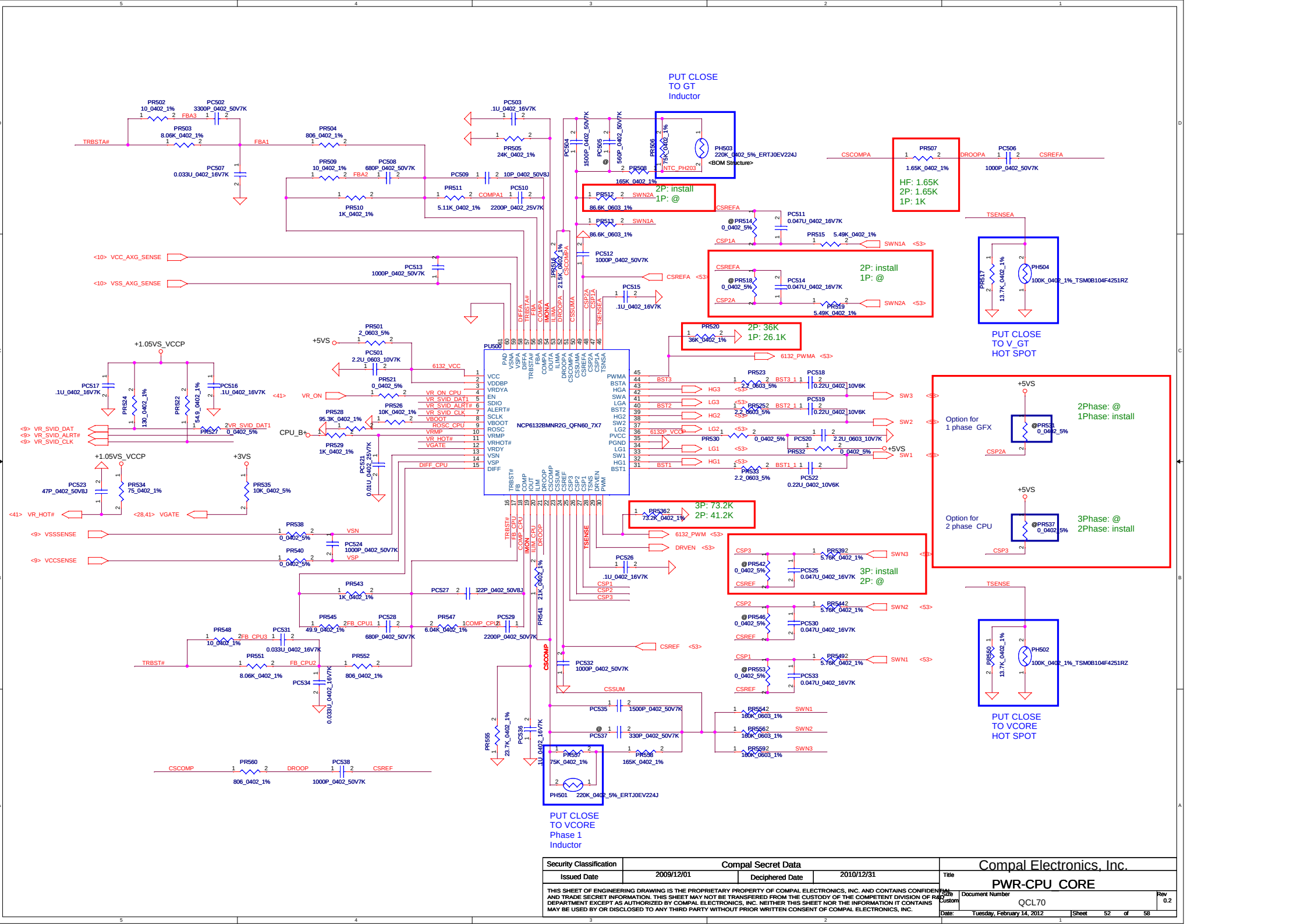
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size	Document Number	Rev
C	SAMSUNG	0.2

Date: Tuesday, February 14, 2012 Sheet 51 of 58


PUT CLOSE TO GT Inductor
PUT CLOSE TO V_GT HOT SPOT
PUT CLOSE TO VCORE HOT SPOT
PUT CLOSE TO VCORE Phase 1 Inductor
HF: 1.65K
2P: 1.65K
1P: 1K
2P: install
1P: @
2P: 36K
1P: 26.1K
3P: 73.2K
2P: 41.2K
3P: install
2P: @
Option for 1 phase GFX
2Phase: @
1Phase: install
Option for 2 phase CPU
3Phase: @
2Phase: install
NCP6132BMNR2G_QFN60_7X7
PU500
PH503 220K_0402_5%_ERTJ0EV224J
PH504 100K_0402_1%_TSM0B104F4251RZ
PH502 100K_0402_1%_TSM0B104F4251RZ
PH501 220K_0402_5%_ERTJ0EV224J
+1.05VS_VCCP
+5VS
+3VS
CPU_B+
Security Classification
Compal Secret Data
Issued Date
2009/12/01
Deciphered Date
2010/12/31
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Title
PWR-CPU_CORE
Size
Custom
Document Number
QCL70
Rev
0.2
Date:
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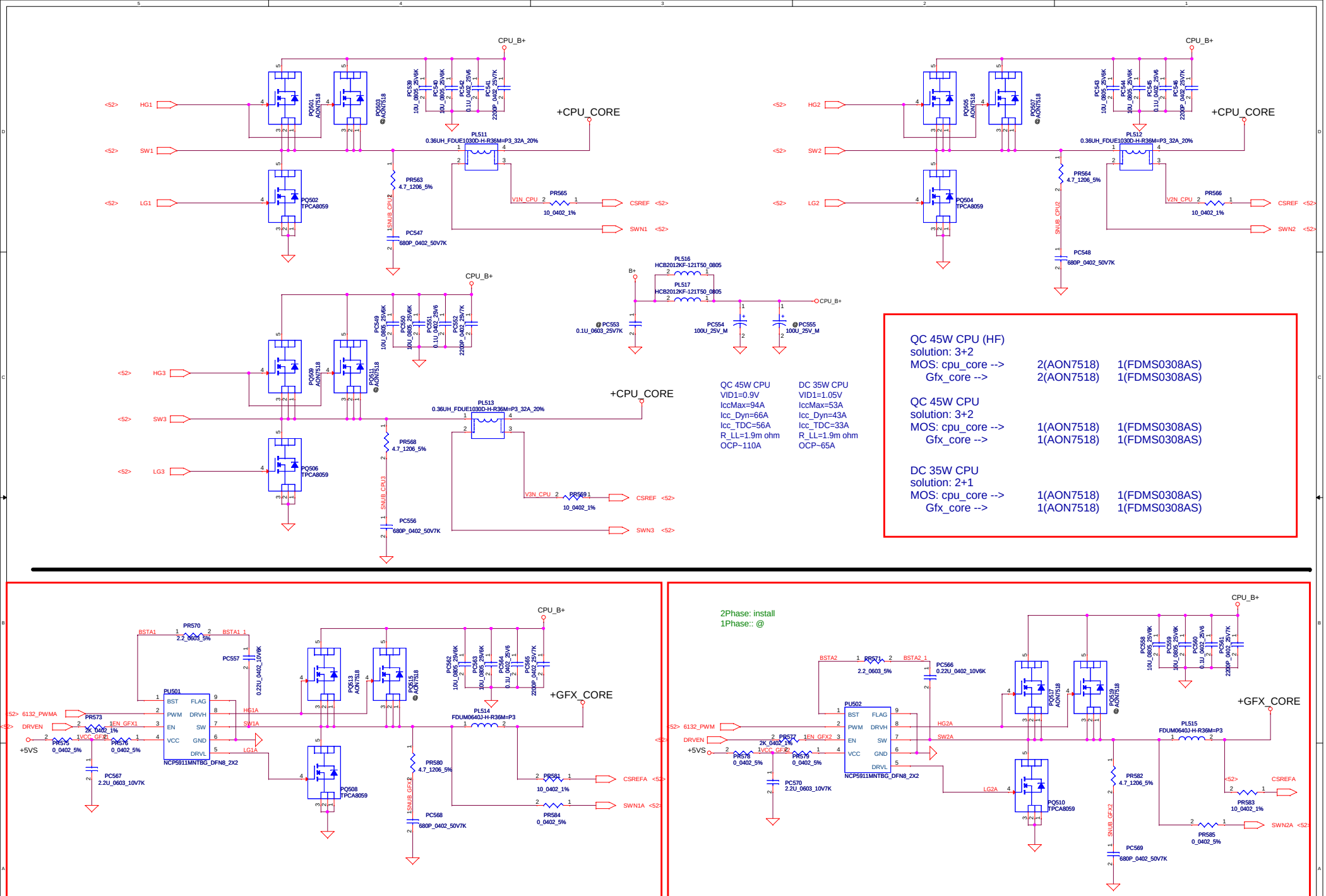

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
C	QCL70	0.2

Date: Tuesday, February 14, 2012 Sheet 53 of 58

+CPU_CORE

+CPU_CORE

PC1101 10U_0805_6.3V6M
PC1102 10U_0805_6.3V6M
PC1103 10U_0805_6.3V6M
PC1104 10U_0805_6.3V6M
PC1105 10U_0805_6.3V6M
PC1106 10U_0805_6.3V6M
PC1107 10U_0805_6.3V6M
PC1108 10U_0805_6.3V6M
PC1109 10U_0805_6.3V6M
PC1110 10U_0805_6.3V6M

+CPU_CORE

PC1111 22U_0805_6.3V6M
PC1112 22U_0805_6.3V6M
PC1113 22U_0805_6.3V6M
PC1114 22U_0805_6.3V6M
PC1115 22U_0805_6.3V6M
PC1116 22U_0805_6.3V6M
PC1117 22U_0805_6.3V6M
PC1118 22U_0805_6.3V6M
PC1119 22U_0805_6.3V6M
PC1120 22U_0805_6.3V6M
PC1121 22U_0805_6.3V6M
PC1122 22U_0805_6.3V6M
PC1123 22U_0805_6.3V6M
PC1124 22U_0805_6.3V6M
PC1125 22U_0805_6.3V6M
PC1126 22U_0805_6.3V6M

+GFX_CORE

+GFX_CORE

PC1151 22U_0805_6.3V6M
PC1152 22U_0805_6.3V6M
PC1153 22U_0805_6.3V6M
PC1154 22U_0805_6.3V6M
PC1155 22U_0805_6.3V6M
PC1156 22U_0805_6.3V6M
PC1157 22U_0805_6.3V6M
PC1158 22U_0805_6.3V6M
PC1159 22U_0805_6.3V6M
PC1160 22U_0805_6.3V6M
PC1161 22U_0805_6.3V6M
PC1162 22U_0805_6.3V6M
PC1164 330U_D2_2V_Y
PC1165 330U_D2_2V_Y
PC1166 330U_D2_2V_Y

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 F (0805) 2 x (0805) no-stuff sites

+1.05VS_VCCP

PC751 22U_0805_6.3V6M
PC752 22U_0805_6.3V6M
PC753 22U_0805_6.3V6M
PC754 22U_0805_6.3V6M
PC755 22U_0805_6.3V6M
PC756 22U_0805_6.3V6M
PC757 22U_0805_6.3V6M
PC758 22U_0805_6.3V6M
PC759 22U_0805_6.3V6M
PC760 22U_0805_6.3V6M
PC761 22U_0805_6.3V6M
PC762 22U_0805_6.3V6M
PC763 330U_D2_2V_Y
PC764 330U_D2_2V_Y
PC765 330U_D2_2V_Y

+CPU_CORE

PC1127 330U_D2_2V_Y
PC1128 330U_D2_2V_Y
PC1129 330U_D2_2V_Y
PC1130 330U_D2_2V_Y
PC1131 330U_D2_2V_Y

+VGA_CORE

+VGA_CORE

PC932 10U_0603_6.3V6M
PC931 10U_0603_6.3V6M
PC923 10U_0603_6.3V6M
PC924 10U_0603_6.3V6M
PC925 10U_0603_6.3V6M
PC926 10U_0603_6.3V6M
PC928 10U_0603_6.3V6M
PC927 10U_0603_6.3V6M
PC929 10U_0603_6.3V6M
PC933 10U_0603_6.3V6M

PC965 1U_0402_6.3V6K
PC966 1U_0402_6.3V6K
PC964 1U_0402_6.3V6K
PC937 1U_0402_6.3V6K
PC938 1U_0402_6.3V6K
PC969 1U_0402_6.3V6K
PC940 1U_0402_6.3V6K
PC941 1U_0402_6.3V6K
PC942 1U_0402_6.3V6K
PC943 1U_0402_6.3V6K

PC944 1U_0402_6.3V6K
PC945 1U_0402_6.3V6K
PC946 1U_0402_6.3V6K
PC947 1U_0402_6.3V6K
PC948 1U_0402_6.3V6K
PC949 1U_0402_6.3V6K
PC950 1U_0402_6.3V6K
PC951 1U_0402_6.3V6K
PC952 1U_0402_6.3V6K
PC953 1U_0402_6.3V6K

PC970 1U_0402_6.3V6K
PC955 1U_0402_6.3V6K
PC971 1U_0402_6.3V6K
PC957 1U_0402_6.3V6K
PC958 1U_0402_6.3V6K
PC959 1U_0402_6.3V6K
PC960 1U_0402_6.3V6K
PC961 1U_0402_6.3V6K
PC962 1U_0402_6.3V6K
PC963 1U_0402_6.3V6K

+VDDCI

PC934 1U_0402_6.3V6K
PC939 1U_0402_6.3V6K
PC935 1U_0402_6.3V6K
PC954 1U_0402_6.3V6K
PC968 1U_0402_6.3V6K
PC956 1U_0402_6.3V6K
PC636 1U_0402_6.3V6K
PC967 1U_0402_6.3V6K
PC972 1U_0402_6.3V6K
PC973 1U_0402_6.3V6K

PC921 10U_0603_6.3V6M
PC922 10U_0603_6.3V6M

Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	QCLA4 LA-8861P M/B	0.2

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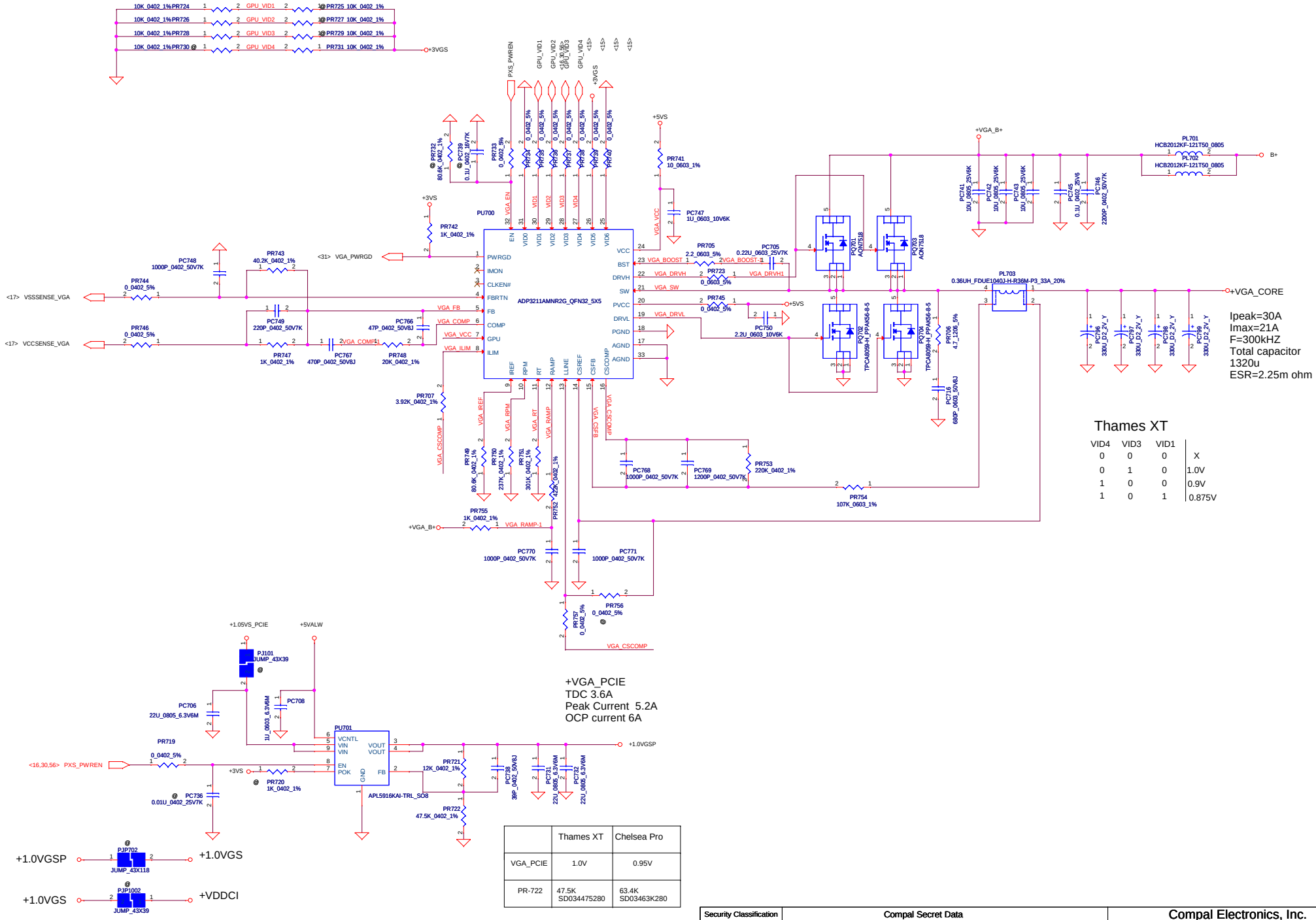


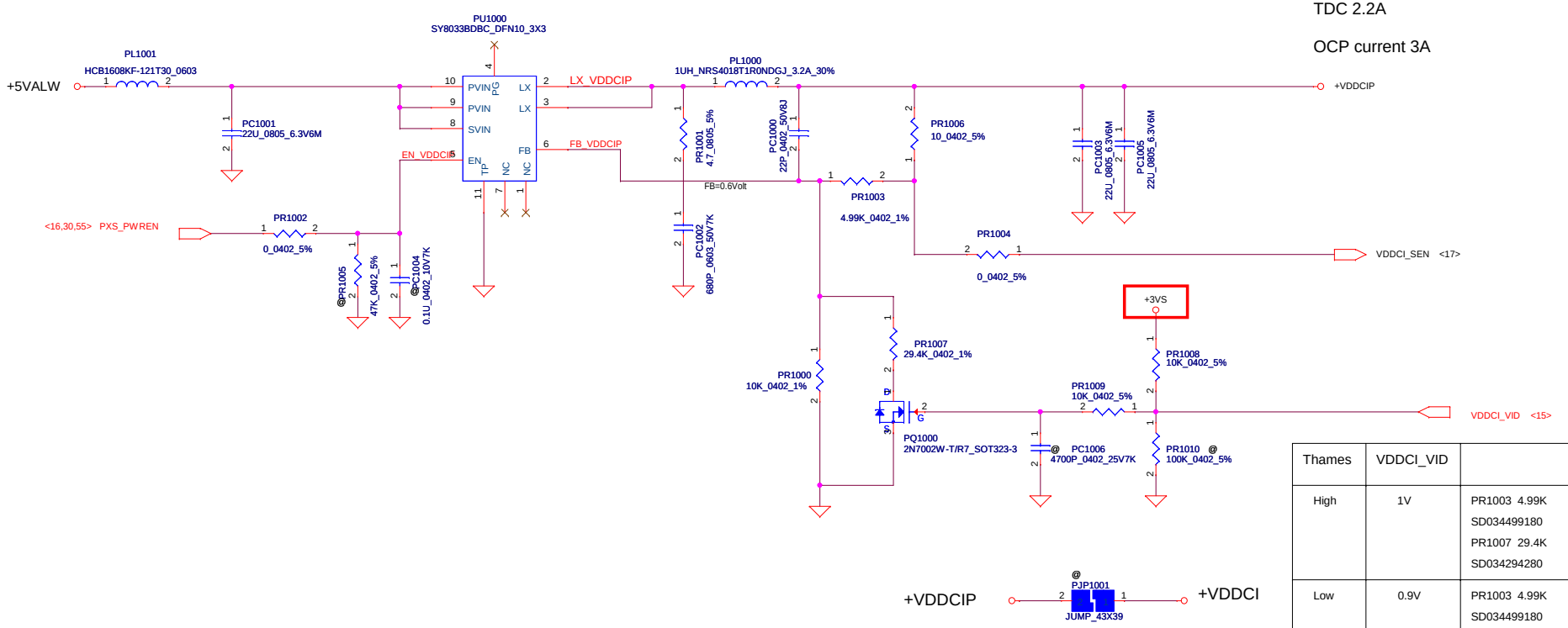
	Thames XT	Chelsea Pro
VGA_PCIE	1.0V	0.95V
PR-722	47.5K SD034475280	63.4K SD03463K280

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Title	+VGA_COREP / +VGA_PCIE(+1.0VGS)		
Size	Document Number		Rev
	QCLA4 LA-8861P M/B		0.2
Date:	Tuesday, February 14, 2012	Sheet	55 of 58

+VDDCI
TDC 2.2A

OCP current 3A



Thames	VDDCI_VID	
High	1V	PR1003 4.99K SD034499180 PR1007 29.4K SD034294280
Low	0.9V	PR1003 4.99K SD034499180

Chelsea	VDDCI_VID	
High	0.95V	PR1003 5.23K SD034523180 PR1007 86.6K SD034866280
Low	0.91V	PR1003 5.23K SD034523180

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: +VDDCIP

Size | Document Number: QCLA4 LA-8861P M/B | Rev: 0.2

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1.	2011/09/29	P51-PWR_+3VALWP/+5VALWP		Change PU330 to RT8205L	Change source
2.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16V	SP	Change PU400 to RT8237C	Change source
3.	2011/09/29	P54-PWR_+VCCSAP/1.8VSP		Change PU450 to SY8037B	Change source
4.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change HMOS to MDV1525	Change source
5.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16V	SP	Change HMOS to MDV1525	Change source
6.	2011/09/29	P49-PWR_BATTERY CONN / OTP		Change PD5,PD6 to SCA00001G00	ESD team request
7.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PR589 from 348 to 8.06k	FAE suggestion
8.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PR590 from 3.65k to 806	FAE suggestion
10.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PC574 from 680P to 0.033u	FAE suggestion
11.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PC577 from 4700P to 0.033u	FAE suggestion
12.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PR548 from 1.21k to 8.06k	FAE suggestion
13.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PR550 from 10.7k to 806	FAE suggestion
14.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PC547 from 680P to 0.033u	FAE suggestion
15.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Change PC551 from 4700P to 0.033u	FAE suggestion
16.	2011/09/29	P57-PWR +CPU_CORE DECOUPLI	NG	Add snubber and boost resistor	For 3x3 H-MOS solution
17.	2011/09/29	P49-PWR_BATTERY CONN / OTP		Add PR22 120k,PR27 100k, PR32 0 Ohm	For 120W adapter protect(9012)
18.	2011/09/29	P58-PWR_VGA_CORE		Remove PC803, PC804 add PC806 47u	For Nvidia suggestion
19.	2011/09/29	P51-PWR_+3VALWP/+5VALWP		Change PC360 to SE000006R80	Change source
20.	2011/09/29	P58-PWR_VGA_CORE		Change PC702 to SE00000H180	Change source
21.	2011/09/29	P49-PWR_BATTERY CONN / OTP		Add PR17 14k, PR33 0 Ohm	For CPU temperature protect(9012)
22.	2011/09/29	P51-PWR_+3VALWP/+5VALWP		Add PR373 0 Ohm	For 3/5 V always power on(9012)

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HW PIR (Product Improve Record)

QCLA4 LA-8861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST		PURPOSE	
1.	02/01	16	Remove PX_MODE and BACO components		No support PX4.0 by K99's request	
2.	02/01	18	Remove PX_EN and RV125		No support PX4.0 by K99's request	
3.	02/01	12	Change RD9.2 to GND		Correct the DDR SPD address	
4.	02/01	13	Change RD15.1 to +3VS		Correct the DDR SPD address	
5.	02/01	26	Stuff BIOS 2M ROM:UH4,RH267,RH269,	CH100,RH271,RH69,CH21	For win8 common design	
6.	02/01	27	Change JTP footprint to ACES_50504	-0120N-001_12P	Follow connector list	
7.	02/01	40	Add JMIC ACES_50271-0020N-001_2P		From K99's request to change AMIC	
8.	02/01	36	Change JWLAN footprint to ACES_889	11-5204_52P	Follow connector list	
9.	02/01	38	Remove INT_MIC from JCRIO.1		From K99's request to change AMIC	
10.	02/01	37	Reserve PJ31 from +3VALW_PCH to +3	V_LAN	To save power consumption	
11.	02/06	38	Swap LR9		For layout smoothly	
12.	02/06	36	Add UM5,RM21;Reserve RM19,PJ33,Lin	k AOAC_WLAN_PWR_EN# to +3V_WLAN	For WLAN ON/OFF feature	
13.	02/06	43	Connect AOAC_WLAN_PWR_EN# to EC pi	n38; Connect WLAN_RST# to EC pin91	For WLAN ON/OFF feature	
14.	02/06	38	Change JCRIO.1 netname to NBA_PLUG	and change JCRIO.2 to MIC_SENSE	Remove AMic solution on sub/B	
15.	02/06	40	Remove CA64 and add RA32,RA33 to l	ink SENSE_A to UA1.13	Remove AMic solution on sub/B	
16.	02/09	37	Add TL1 on UL1.37		Reserved from vendor's suggestion	
17.	02/09	31	Change UH1.T7 from HDMI_HPD to CHP	3_SERDBG and add RH216 PH 1Kohm	For Serial POST debugger feature	
18.	02/09	24	Delete T66 and link CHP3_SERDBG to	JCRT.4	For Serial POST debugger feature	
19.	02/09	10	Remove CC58		To prevent from short with thermal	
19.	02/09	25	Add D94,D95,D96 on HDMI signal		For ESD request	
20.	02/09	24	DEL D3~D5 and add D97,D98 on CRT s	ignal	For ESD request	
21.	02/09	37	Add D99,D100 on LAN signal		For ESD request	
22.	02/09	35	Add R1000~R1003 between JODD and J	ODDB	Reserve for reducing SATA signal refle	ction
23.	02/09	08	Reserve DRAMRST_CNTRL_EC to QC3		Reserved for DS3 feature	
24.	02/09	41	Reserve DRAMRST_CNTRL_EC to EC pin	89	Reserved for DS3 feature	

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